

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

SWITCHING  
 N- AND P-CANNEL POWER MOS FET

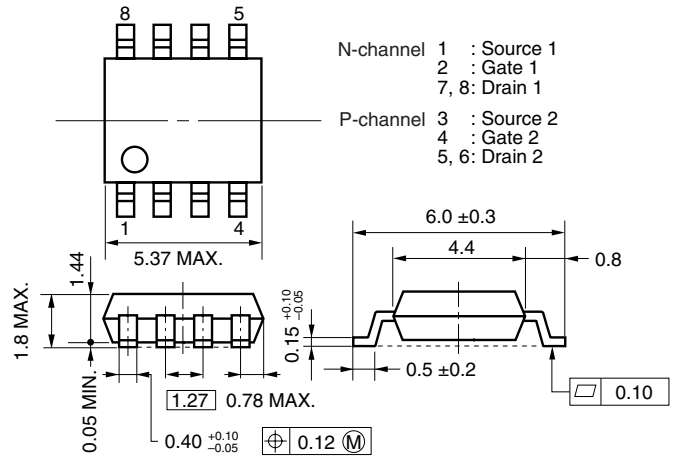
DESCRIPTION

The  $\mu$ PA2794AGR is N- and P-channel MOS Field Effect Transistors designed for Motor Drive application.

FEATURES

- Low on-state resistance  
 N-channel  $R_{DS(on)1} = 25 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 2.8 \text{ A}$ )  
 $R_{DS(on)2} = 33 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = 4.5 \text{ V}$ ,  $I_D = 2.8 \text{ A}$ )  
 P-channel  $R_{DS(on)1} = 43 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = -10 \text{ V}$ ,  $I_D = -2.8 \text{ A}$ )  
 $R_{DS(on)2} = 54 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = -4.5 \text{ V}$ ,  $I_D = -2.8 \text{ A}$ )
- Low input capacitance  
 N-channel  $C_{iss} = 2200 \text{ pF TYP.}$   
 P-channel  $C_{iss} = 2200 \text{ pF TYP.}$
- Built-in gate protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit: mm)

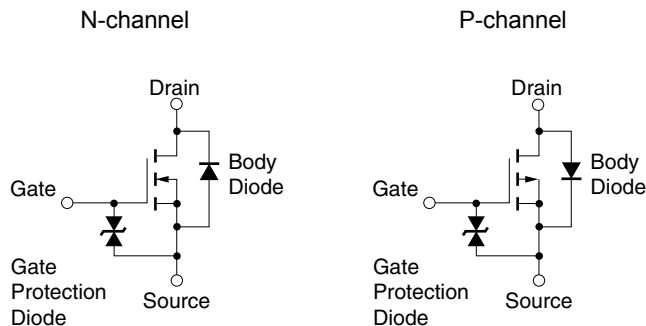


ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
$\mu$ PA2794AGR-E1-AT <sup>Note</sup>	Pure Sn	Tape 2500 p/reel	Power SOP8
$\mu$ PA2794AGR-E2-AT <sup>Note</sup>			

**Note** Pb-free (This product does not contain Pb in external electrode and other parts.)

EQUIVALENT CIRCUITS



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C. All terminals are connected.)**

PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	60	-60	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	∓20	V
Drain Current (DC)	I <sub>D(DC)</sub>	±5.5	∓5.5	A
Drain Current (pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	±22	∓22	A
Total Power Dissipation (1 unit) <sup>Note2</sup>	P <sub>T1</sub>	1.7		W
Total Power Dissipation (2 units) <sup>Note2</sup>	P <sub>T2</sub>	2.0		W
Channel Temperature	T <sub>ch</sub>	150		°C
Storage Temperature	T <sub>stg</sub>	-55 to +150		°C
Single Avalanche Current <sup>Note3</sup>	I <sub>AS</sub>	5.5	-5.5	A
Single Avalanche Energy <sup>Note3</sup>	E <sub>AS</sub>	3.03		mJ

**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1%

**2.** Mounted on ceramic substrate of 2000 mm<sup>2</sup> x 1.6 mm

**3.** Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = 30 V, R<sub>G</sub> = 25 Ω, L = 100 μH, V<sub>GS</sub> = 20 → 0 V

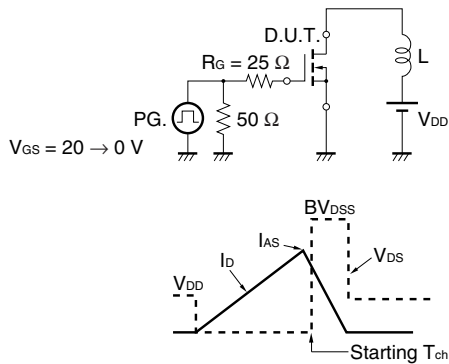
**ELECTRICAL CHARACTERISTICS (TA = 25°C. All terminals are connected.)**

**N-channel**

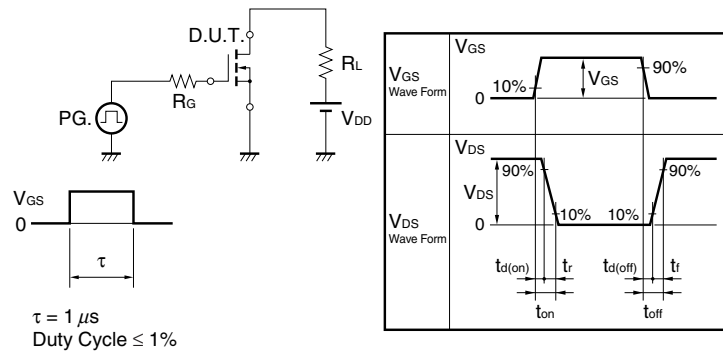
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$			10	μA
Gate Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			±10	μA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	1.5	2.0	2.5	V
Forward Transfer Admittance <sup>Note</sup>	$ y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 2.8\text{ A}$	4	7.6		S
Drain to Source On-state Resistance <sup>Note</sup>	$R_{DS(on)1}$	$V_{GS} = 10\text{ V}, I_D = 2.8\text{ A}$		19.5	25	mΩ
	$R_{DS(on)2}$	$V_{GS} = 4.5\text{ V}, I_D = 2.8\text{ A}$		23	33	mΩ
Input Capacitance	$C_{iss}$	$V_{DS} = 10\text{ V},$		2200		pF
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V},$		245		pF
Reverse Transfer Capacitance	$C_{rss}$	$f = 1\text{ MHz}$		136		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, I_D = 2.8\text{ A},$		10		ns
Rise Time	$t_r$	$V_{GS} = 10\text{ V},$		16		ns
Turn-off Delay Time	$t_{d(off)}$	$R_G = 0\ \Omega$		58		ns
Fall Time	$t_f$			7.5		ns
Total Gate Charge	$Q_G$	$I_D = 5.5\text{ A},$		41		nC
Gate to Source Charge	$Q_{GS}$	$V_{DD} = 48\text{ V},$		6.3		nC
Gate to Drain Charge	$Q_{GD}$	$V_{GS} = 10\text{ V}$		11		nC
Body Diode Forward Voltage <sup>Note</sup>	$V_{F(S-D)}$	$I_F = 5.5\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = 5.5\text{ A}, V_{GS} = 0\text{ V},$		28		ns
Reverse Recovery Charge	$Q_{rr}$	$di/dt = 100\text{ A}/\mu\text{s}$		29		nC

**Note** Pulsed

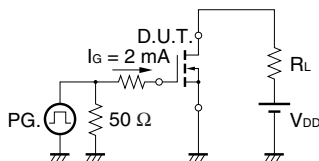
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**



**TEST CIRCUIT 3 GATE CHARGE**

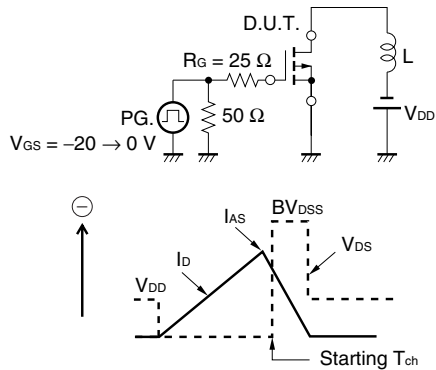


**P-channel**

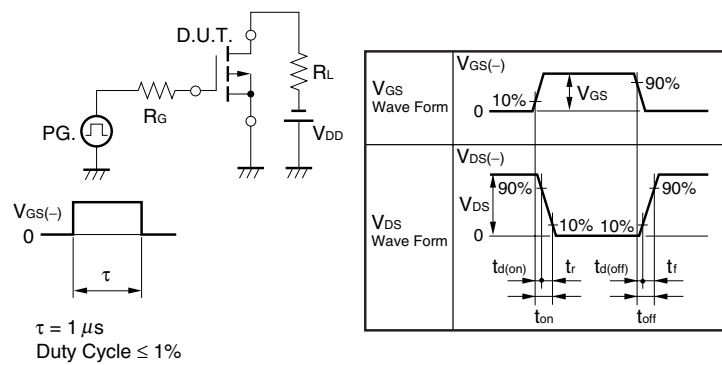
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}$			-10	$\mu\text{A}$
Gate Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\mp 10$	$\mu\text{A}$
Gate to Source Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = -10\text{ V}, I_D = -1\text{ mA}$	-1.0	-1.7	-2.5	V
Forward Transfer Admittance <sup>Note</sup>	$ y_{fs} $	$V_{DS} = -10\text{ V}, I_D = -2.8\text{ A}$	5	10		S
Drain to Source On-state Resistance <sup>Note</sup>	$R_{DS(on)1}$	$V_{GS} = -10\text{ V}, I_D = -2.8\text{ A}$		33	43	$\text{m}\Omega$
	$R_{DS(on)2}$	$V_{GS} = -4.5\text{ V}, I_D = -2.8\text{ A}$		36	54	$\text{m}\Omega$
Input Capacitance	$C_{iss}$	$V_{DS} = -10\text{ V},$		2200		pF
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V},$		270		pF
Reverse Transfer Capacitance	$C_{rss}$	$f = 1\text{ MHz}$		200		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -30\text{ V}, I_D = -2.8\text{ A},$		10		ns
Rise Time	$t_r$	$V_{GS} = -10\text{ V},$		22		ns
Turn-off Delay Time	$t_{d(off)}$	$R_G = 0\ \Omega$		150		ns
Fall Time	$t_f$			23		ns
Total Gate Charge	$Q_G$	$I_D = -5.5\text{ A},$		45		nC
Gate to Source Charge	$Q_{GS}$	$V_{DD} = -48\text{ V},$		4.3		nC
Gate to Drain Charge	$Q_{GD}$	$V_{GS} = -10\text{ V}$		13		nC
Body Diode Forward Voltage <sup>Note</sup>	$V_{F(S-D)}$	$I_F = 5.5\text{ A}, V_{GS} = 0\text{ V}$	0.83	1.5		V
Reverse Recovery Time	$t_{rr}$	$I_F = -5.5\text{ A}, V_{GS} = 0\text{ V},$		46		ns
Reverse Recovery Charge	$Q_{rr}$	$di/dt = -50\text{ A}/\mu\text{s}$		29		nC

**Note** Pulsed

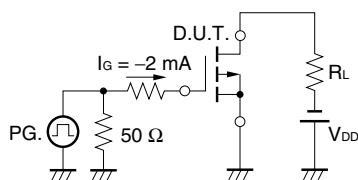
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

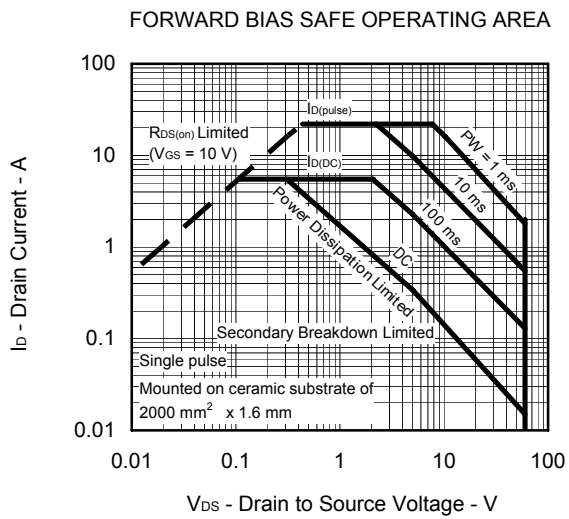
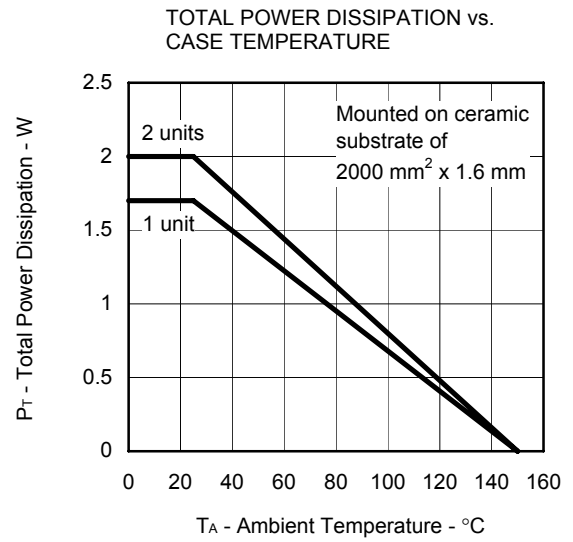
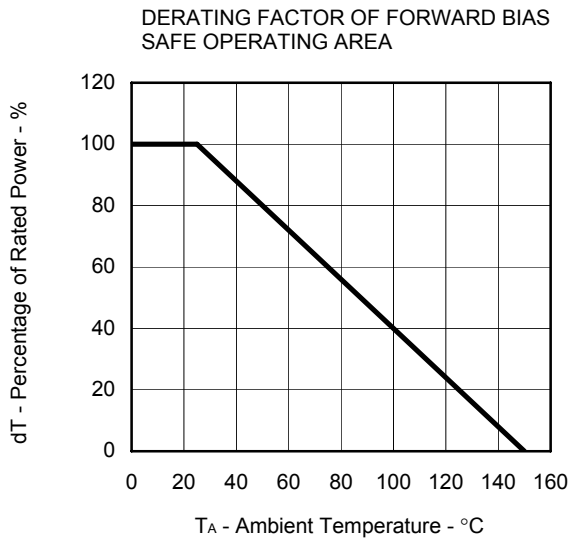


**TEST CIRCUIT 3 GATE CHARGE**

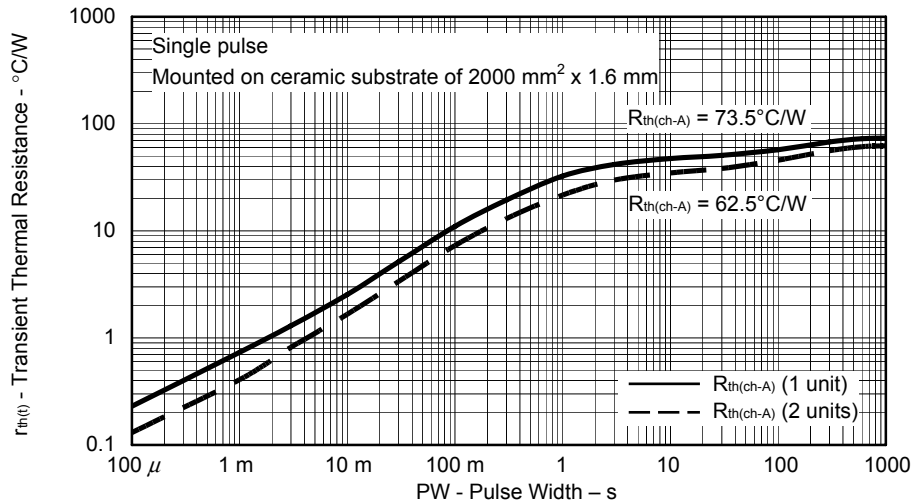


TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

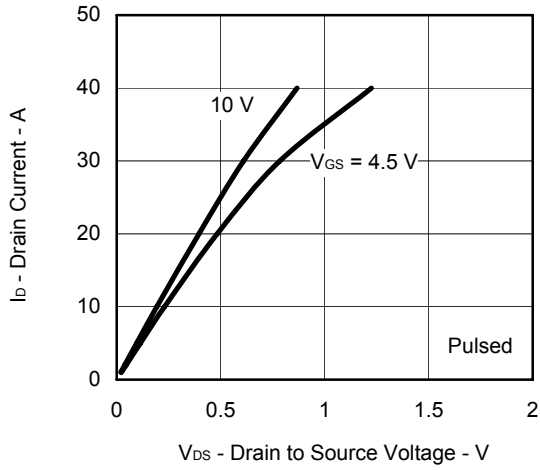
(1) N-channel



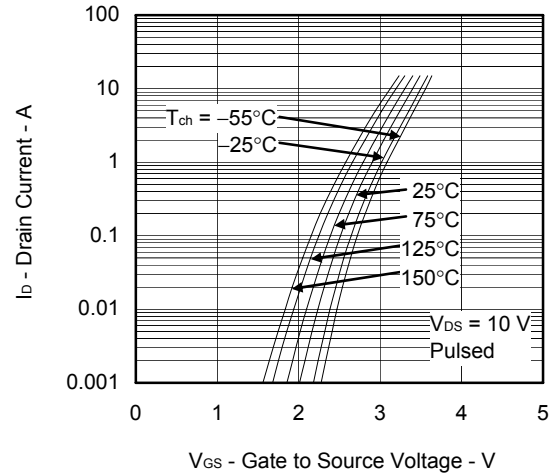
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



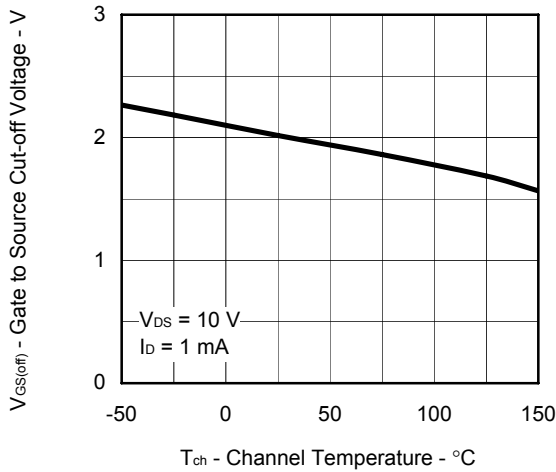
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



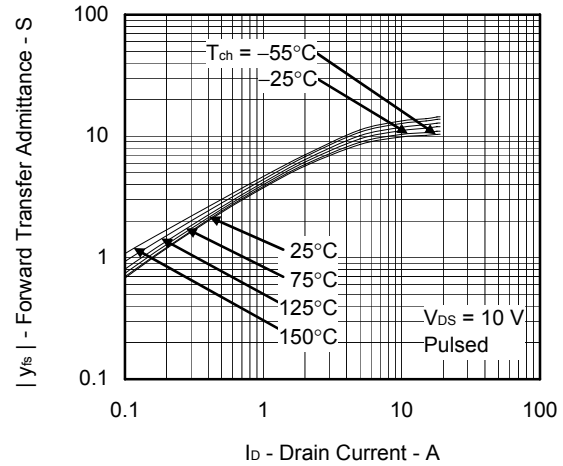
FORWARD TRANSFER CHARACTERISTICS



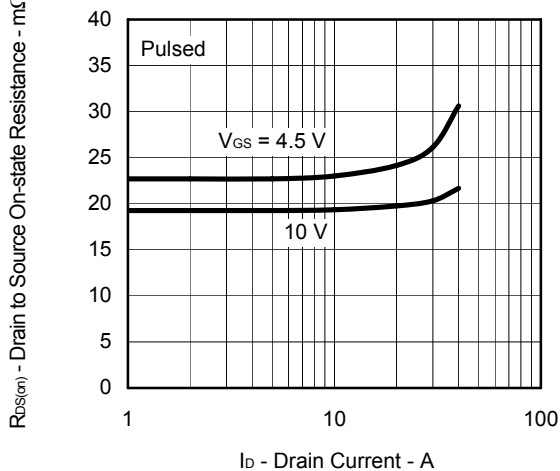
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



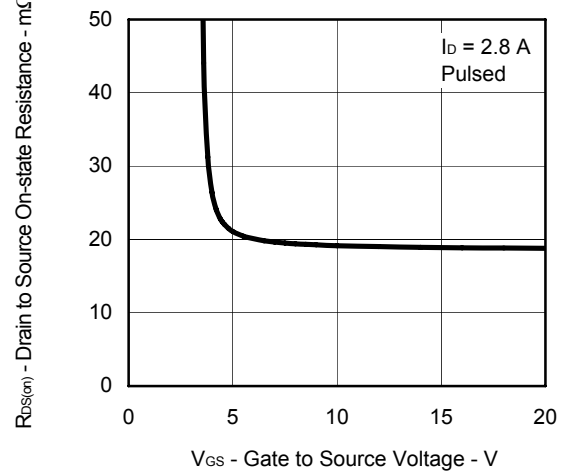
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

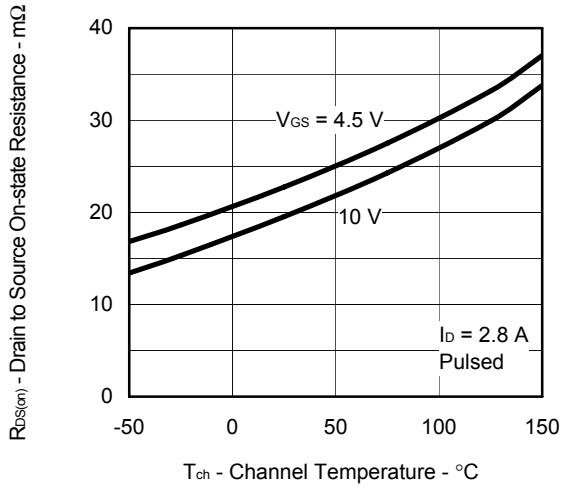


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

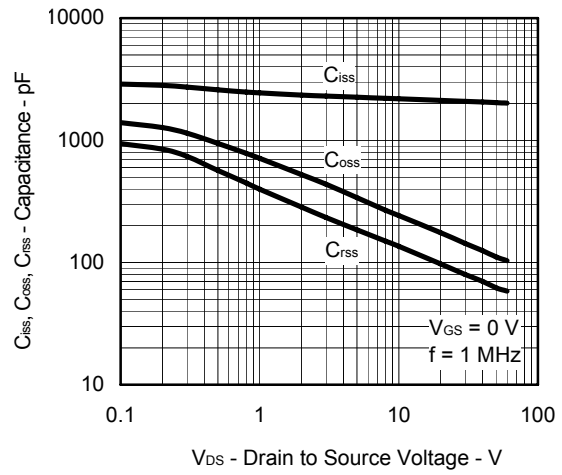




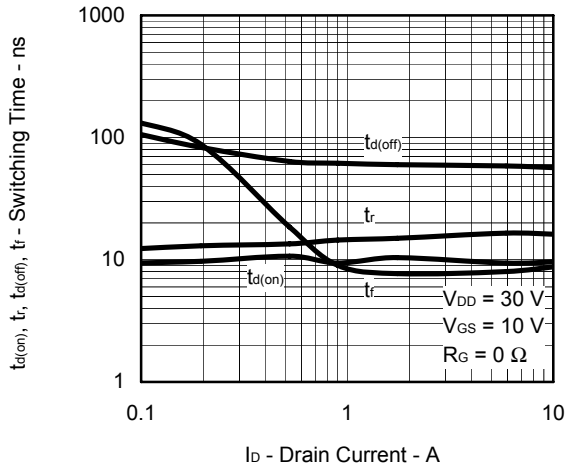
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



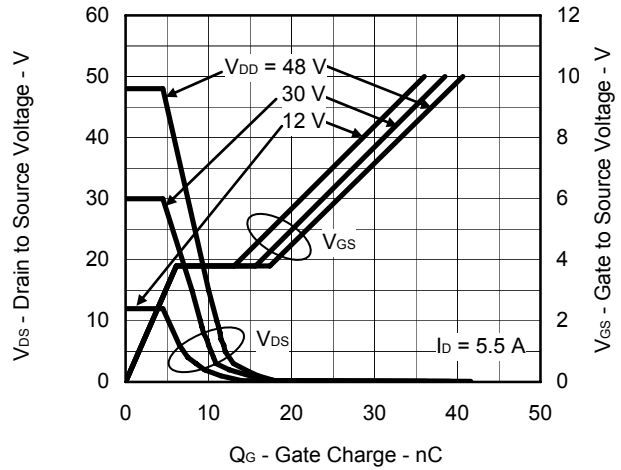
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



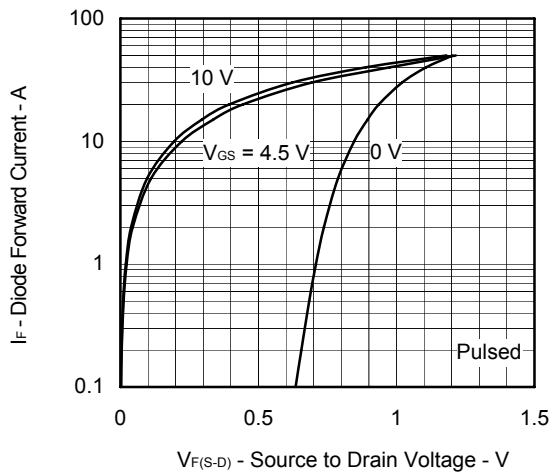
SWITCHING CHARACTERISTICS



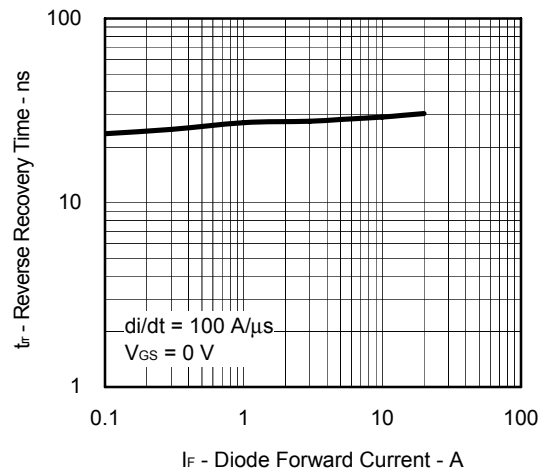
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

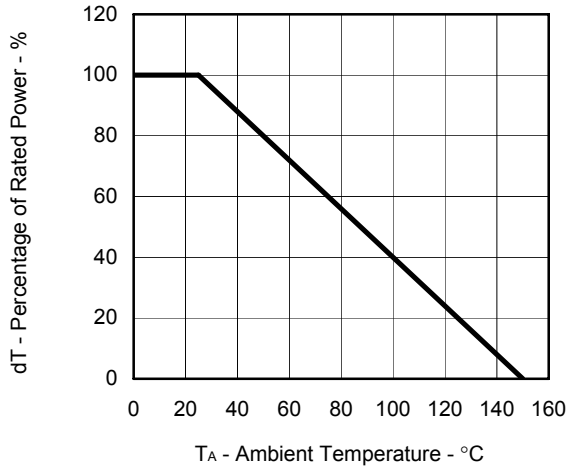


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

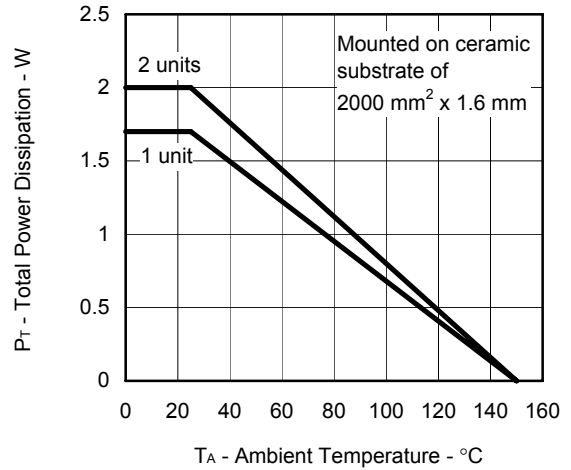


(2) P-channel

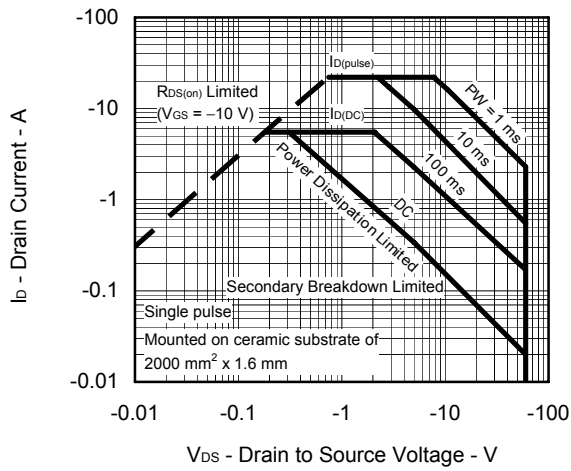
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



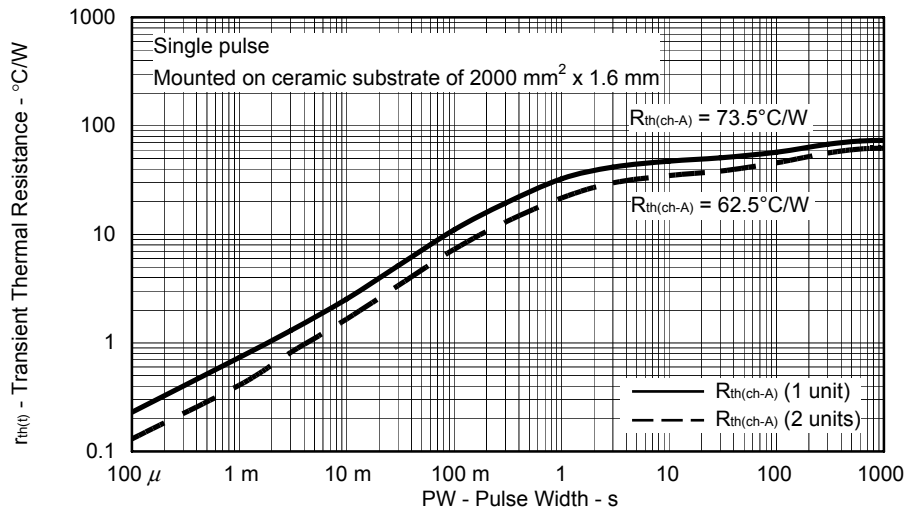
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



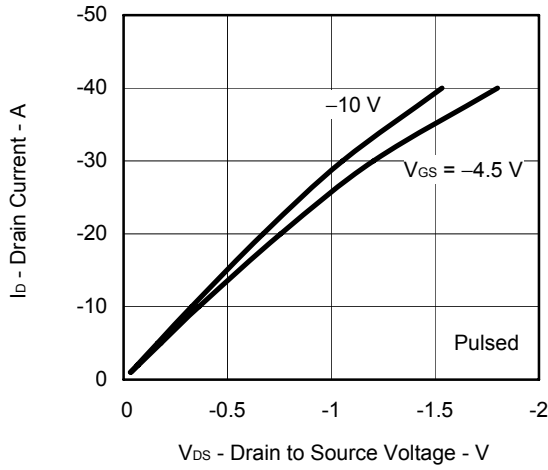
FORWARD BIAS SAFE OPERATING AREA



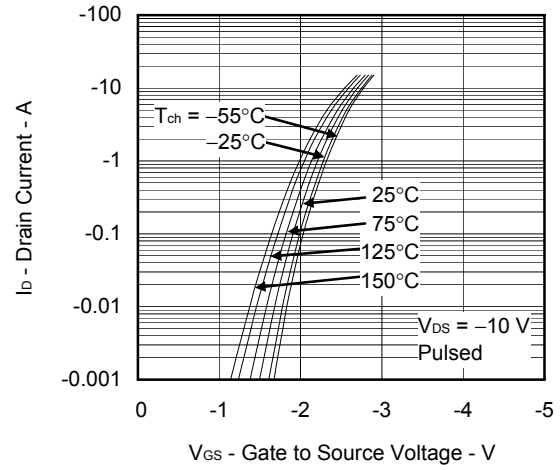
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



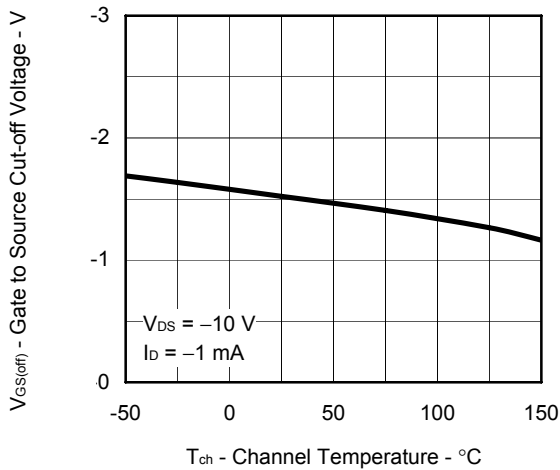
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



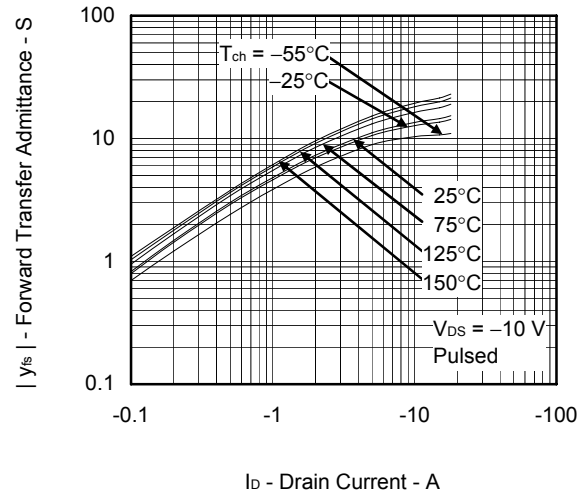
FORWARD TRANSFER CHARACTERISTICS



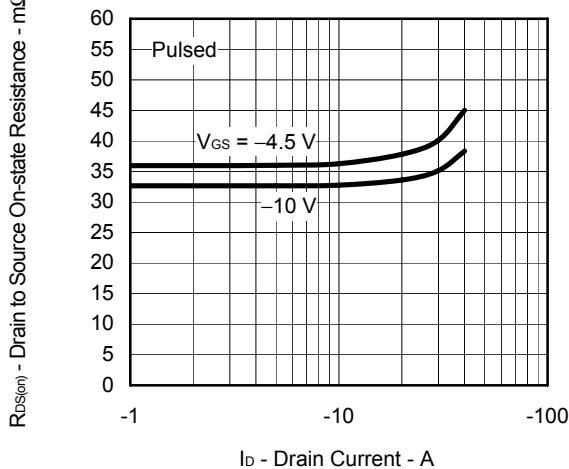
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



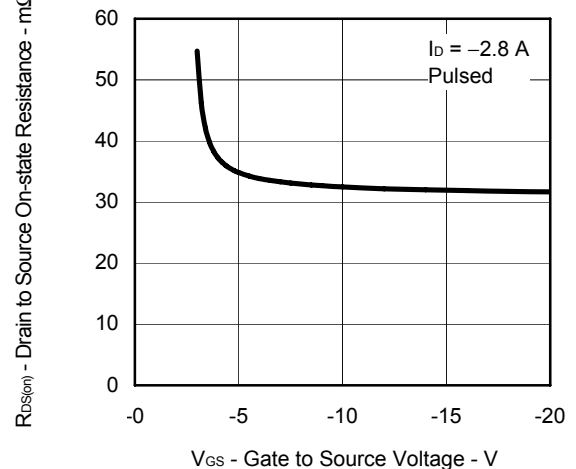
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



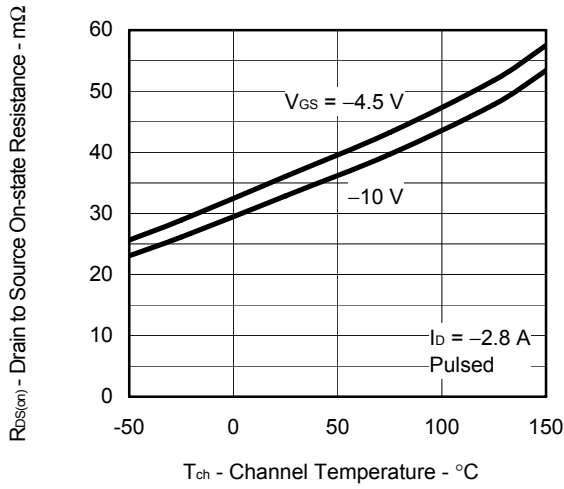
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



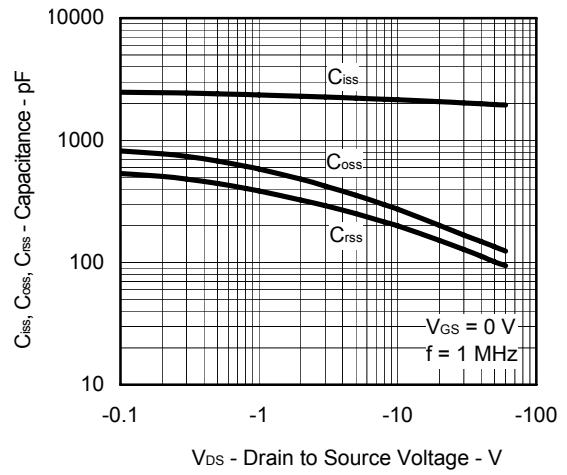
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



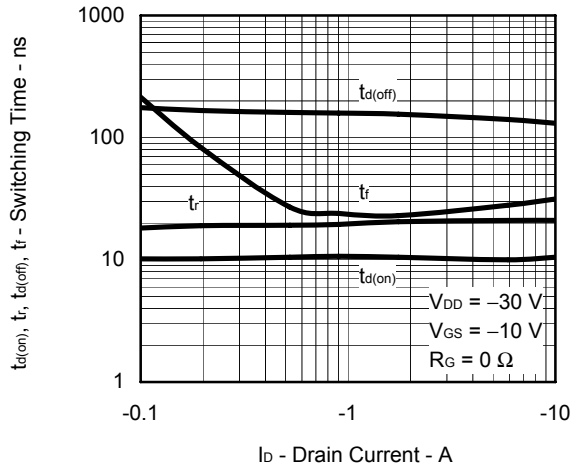
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



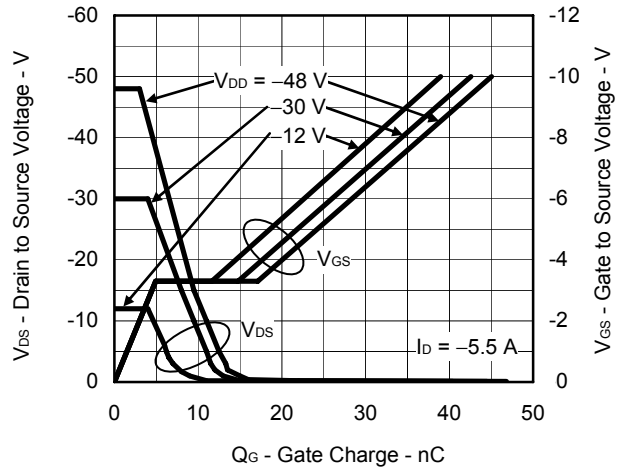
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



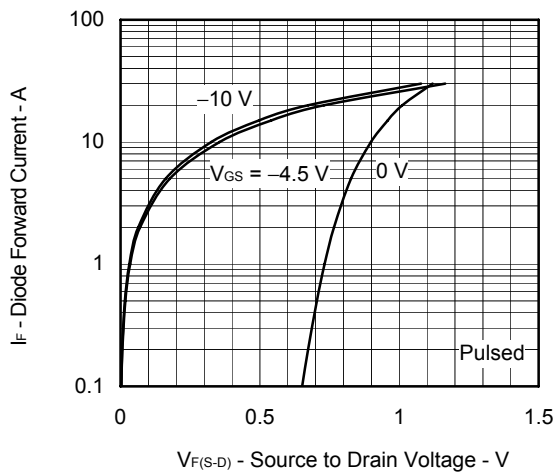
SWITCHING CHARACTERISTICS



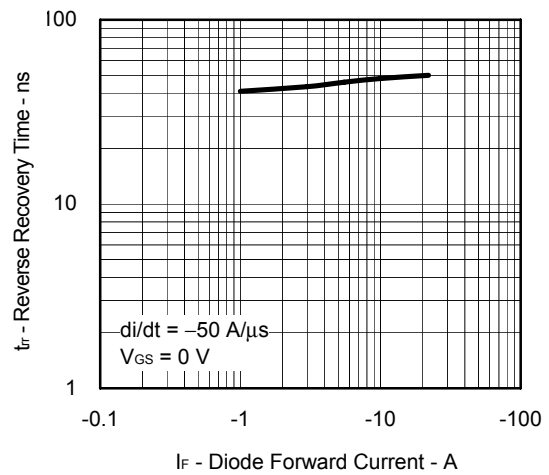
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

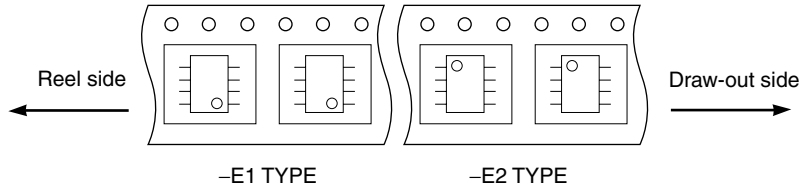


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

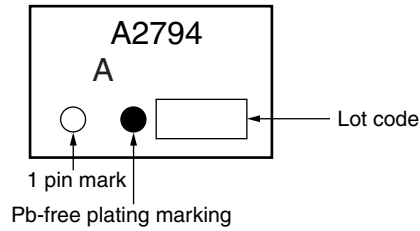


**TAPE INFORMATION**

There are two types (-E1, -E2) of taping depending on the direction of the device.



**MARKING INFORMATION**



**RECOMMENDED SOLDERING CONDITIONS**

The μPA2794AGR should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Maximum temperature (Package's surface temperature): 260°C or below Time at maximum temperature: 10 seconds or less Time of temperature higher than 220°C: 60 seconds or less Preheating time at 160 to 180°C: 60 to 120 seconds Maximum number of reflow processes: 3 times Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	IR60-00-3
Partial heating	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350

**Caution Do not use different soldering methods together (except for partial heating).**

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