N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ZVNL120C

ISSUE 2 – MARCH 94

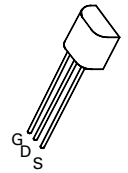
FEATURES

* 200 Volt V_{DS}
* $R_{DS(on)}$=10Ω
* Low threshold

APPLICATIONS

* Telephone handsets

REFER TO ZVNL120A FOR GRAPHS



E-Line
TO92 Compatible

ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	200	V
Continuous Drain Current at T_{amb}=25°C	I_D	180	mA
Pulsed Drain Current	I_{DM}	2	A
Gate Source Voltage	V_{GS}	± 20	V
Power Dissipation at T_{amb}=25°C	P_{tot}	700	mW
Operating and Storage Temperature Range	T_j:T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise stated).

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	200		V	I_D=1mA, V_{GS}=0V
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.5	1.5	V	ID=1mA, V_{DS}= V_{GS}
Gate-Body Leakage	I_{GSS}		100	nA	V_{GS}=± 20V, V_{DS}=0V
Zero Gate Voltage Drain Current	I_{DSS}		10 100	µA µA	V_{DS}=200 V, V_{GS}=0 V_{DS}=160 V, V_{GS}=0V, T=125°C(2)
On-State Drain Current(1)	$I_{D(on)}$	500		mA	V_{DS}=25 V, V_{GS}=5V
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		10 10	Ω Ω	V_{GS}=5V,I_D=250mA V_{GS}=3V, I_D=125mA
Forward Transconductance (1)(2)	g_{fs}	200		mS	V_{DS}=25V,I_D=250mA
Input Capacitance (2)	C_{iss}		85	pF	V_{DS}=25 V, V_{GS}=0V, f=1MHz
Common Source Output Capacitance (2)	C_{oss}		20	pF	
Reverse Transfer Capacitance (2)	C_{rss}		7	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		8	ns	V_{DD}≈25V, I_D=250mA
Rise Time (2)(3)	t_r		8	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		20	ns	
Fall Time (2)(3)	t_f		12	ns	

(1) Measured under pulsed conditions. Width=300µs. Duty cycle ≤2%
(2) Sample test.

3) Switching times measured with 50Ω source impedance and <5ns rise time on a pulse generator