

# PMR670UPE

20 V, 480 mA P-channel Trench MOSFET

Rev. 1 — 13 September 2011

Product data sheet

## 1. Product profile

### 1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT416 (SC-75) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

### 1.2 Features and benefits

- Very fast switching
- Trench MOSFET technology
- ESD protection up to 2 kV
- AEC-Q101 qualified

### 1.3 Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

### 1.4 Quick reference data

Table 1. Quick reference data

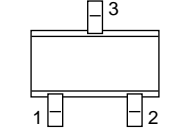
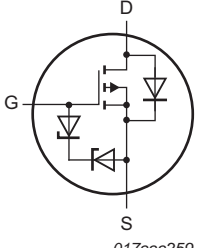
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-20	V
$V_{GS}$	gate-source voltage		-8	-	8	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-480	mA
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -400\text{ mA}; T_j = 25\text{ °C}$	-	0.67	0.85	$\Omega$

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.



## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p><b>SOT416 (SC-75)</b></p>	 <p>017aaa259</p>
2	S	source		
3	D	drain		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
PMR670UPE	SC-75	plastic surface-mounted package; 3 leads	SOT416

## 4. Marking

**Table 4. Marking codes**

Type number	Marking code
PMR670UPE	AD

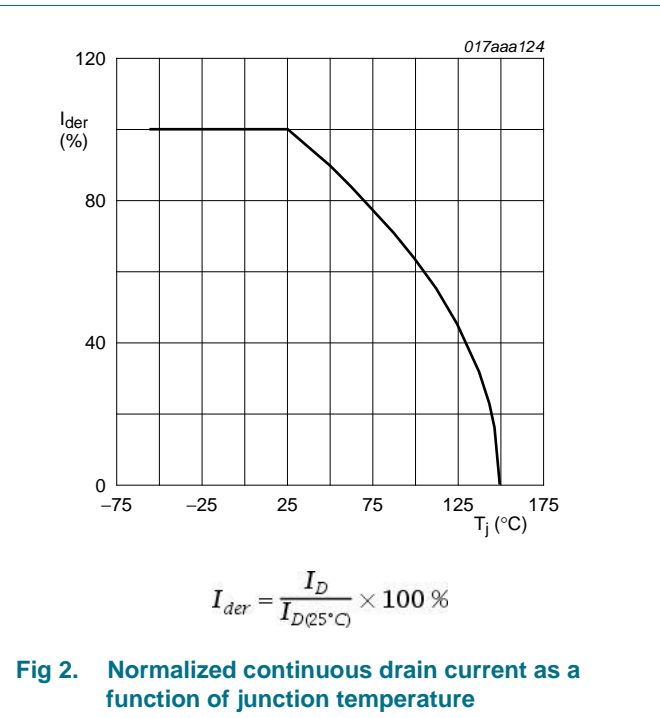
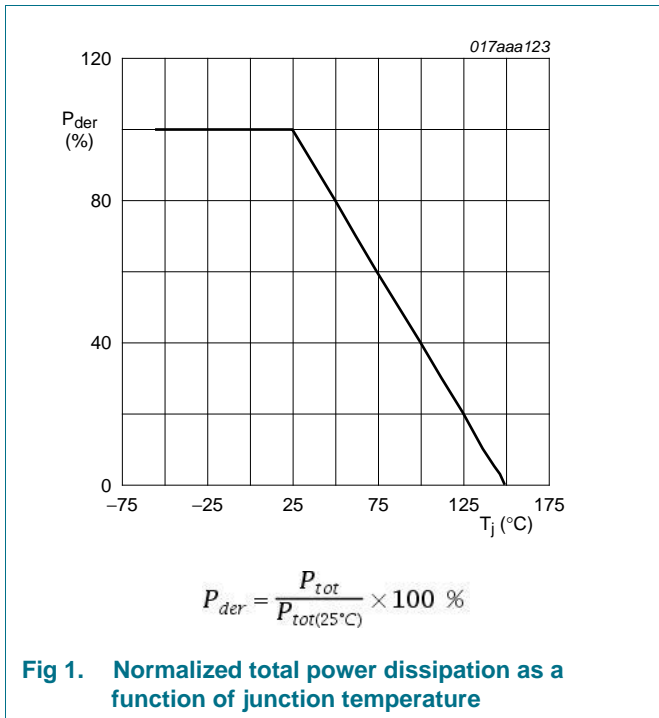
## 5. Limiting values

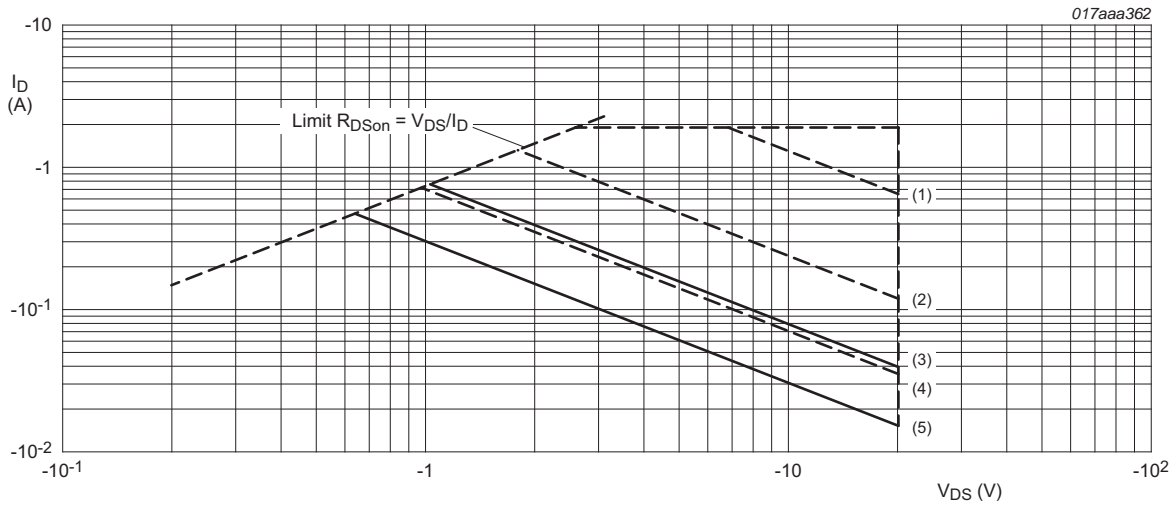
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C	-	-20	V	
V <sub>GS</sub>	gate-source voltage		-8	8	V	
I <sub>D</sub>	drain current	V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 25 °C	[1]	-	-480	mA
		V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 100 °C	[1]	-	-300	mA
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs	-	-1.9	A	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	250	mW
			[1]	-	300	mW
		T <sub>sp</sub> = 25 °C		-	770	mW
T <sub>j</sub>	junction temperature		-55	150	°C	
T <sub>amb</sub>	ambient temperature		-55	150	°C	
T <sub>stg</sub>	storage temperature		-65	150	°C	
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	-300	mA
<b>ESD maximum rating</b>						
V <sub>ESD</sub>	electrostatic discharge voltage	HBM	[3]	-	2000	V

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [3] Measured between all pins.





$I_{DM}$  = single pulse

(1)  $t_p = 1$  ms

(2)  $t_p = 10$  ms

(3) DC;  $T_{sp} = 25$  °C

(4)  $t_p = 100$  ms

(5) DC;  $T_{amb} = 25$  °C; drain mounting pad  $1$  cm<sup>2</sup>

**Fig 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage**

## 6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	440	510	K/W
			[2]	360	415	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	160	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.

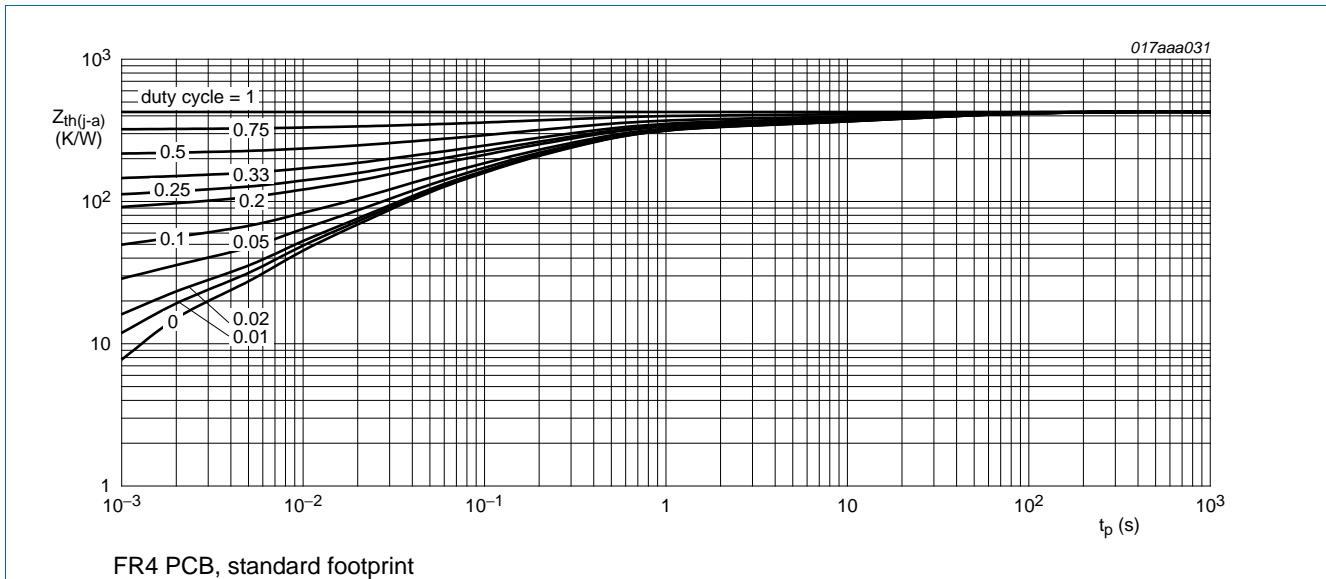


Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

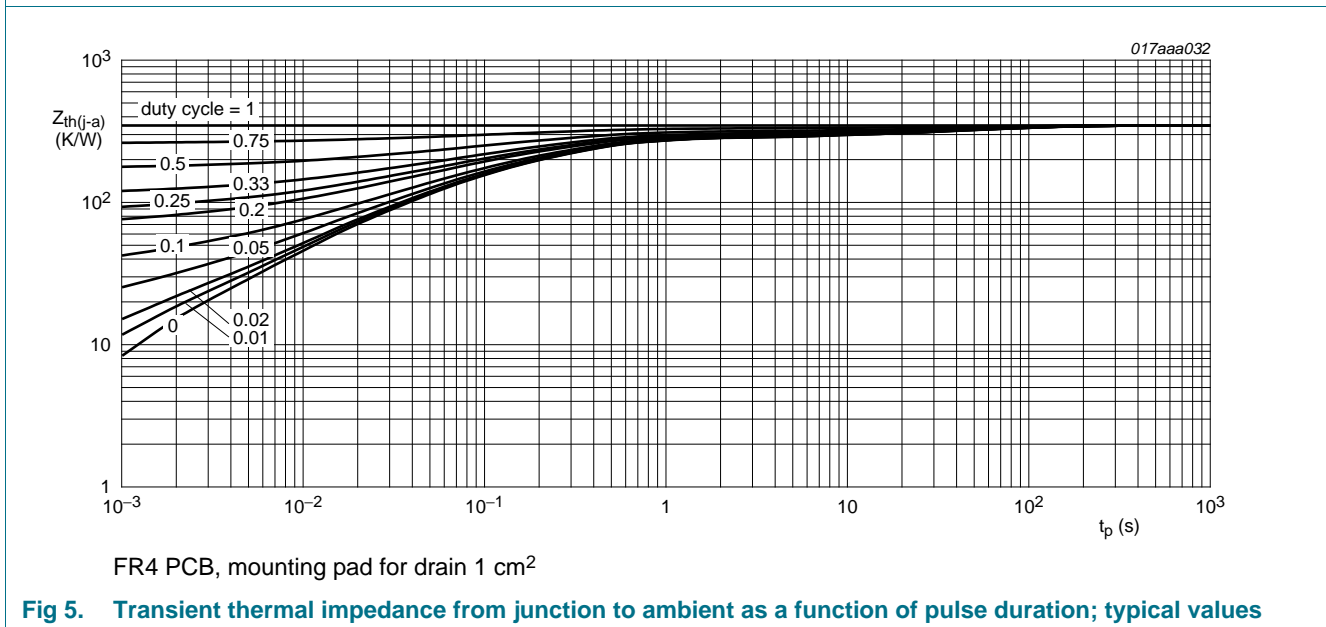


Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 7. Characteristics

**Table 7. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu\text{A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-20	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu\text{A}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-0.5	-0.8	-1.3	V
$I_{DSS}$	drain leakage current	$V_{DS} = -20 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	$\mu\text{A}$
		$V_{DS} = -20 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	-	-10	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 8 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-2	$\mu\text{A}$
		$V_{GS} = -8 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-2	$\mu\text{A}$
		$V_{GS} = 4.5 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-0.5	$\mu\text{A}$
		$V_{GS} = -4.5 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-0.5	$\mu\text{A}$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}$ ; $I_D = -400 \text{ mA}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	0.67	0.85	$\Omega$
		$V_{GS} = -4.5 \text{ V}$ ; $I_D = -400 \text{ mA}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	1.1	1.4	$\Omega$
		$V_{GS} = -2.5 \text{ V}$ ; $I_D = -200 \text{ mA}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	1.2	1.5	$\Omega$
		$V_{GS} = -1.8 \text{ V}$ ; $I_D = -10 \text{ mA}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	1.8	2.8	$\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -10 \text{ V}$ ; $I_D = -200 \text{ mA}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	610	-	mS
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 \text{ V}$ ; $I_D = -400 \text{ mA}$ ; $V_{GS} = -4.5 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	0.76	1.14	nC
$Q_{GS}$	gate-source charge		-	0.28	-	nC
$Q_{GD}$	gate-drain charge		-	0.18	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -10 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	58	87	pF
$C_{oss}$	output capacitance		-	21	-	pF
$C_{rss}$	reverse transfer capacitance		-	12	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10 \text{ V}$ ; $R_L = 250 \Omega$ ; $V_{GS} = -4.5 \text{ V}$ ; $R_{G(ext)} = 6 \Omega$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	18	36	ns
$t_r$	rise time		-	30	-	ns
$t_{d(off)}$	turn-off delay time		-	80	160	ns
$t_f$	fall time		-	72	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = -300 \text{ mA}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-0.48	-0.84	-1.2	V

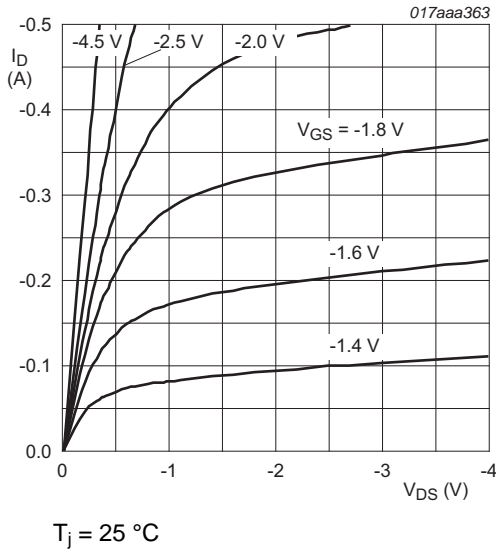


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

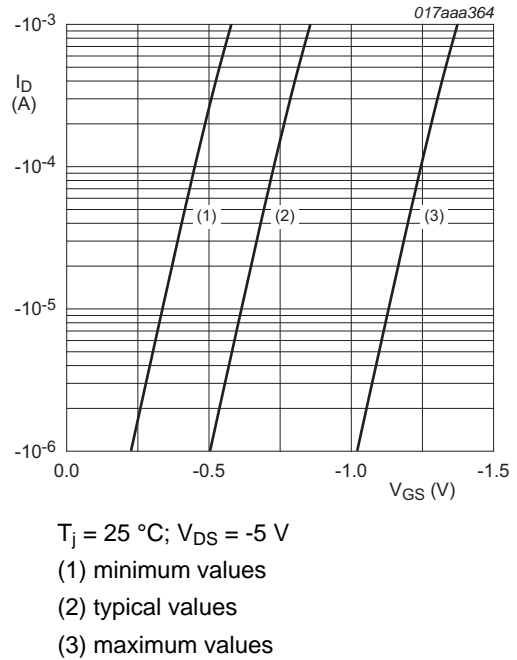


Fig 7. Sub-threshold drain current as a function of gate-source voltage

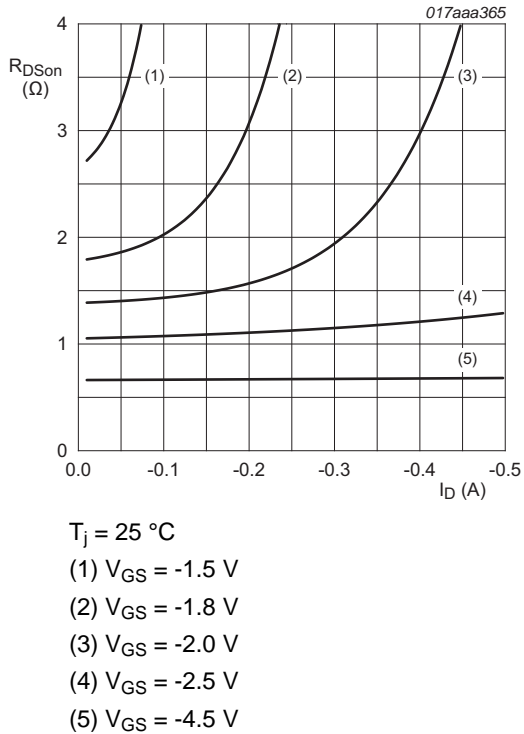


Fig 8. Drain-source on-state resistance as a function of drain current; typical values

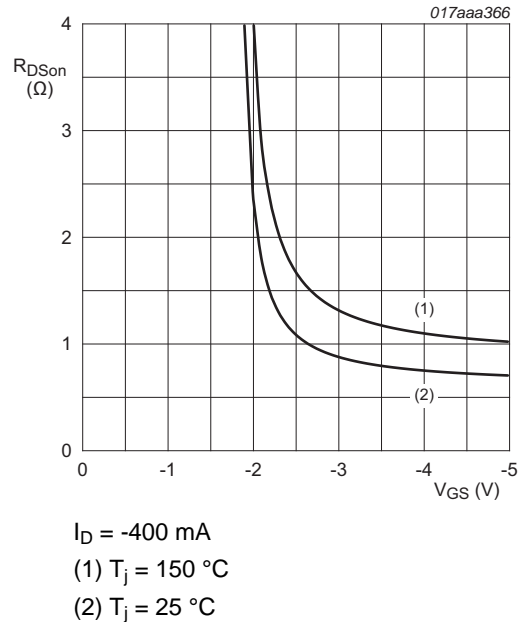
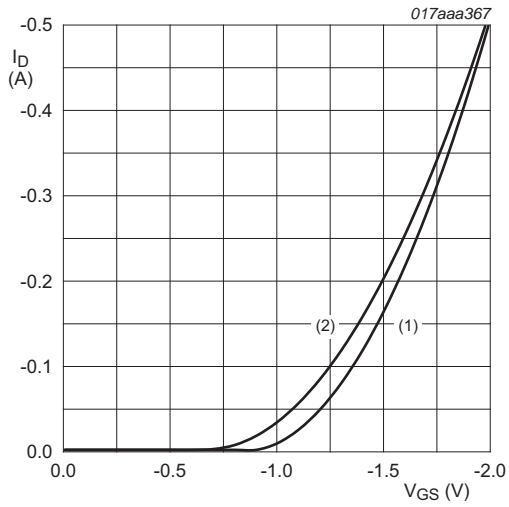
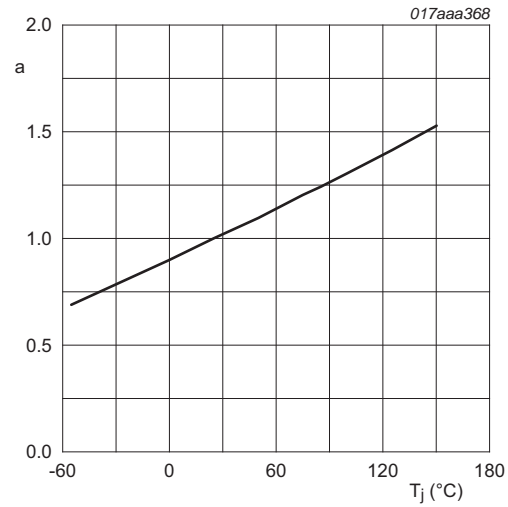


Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



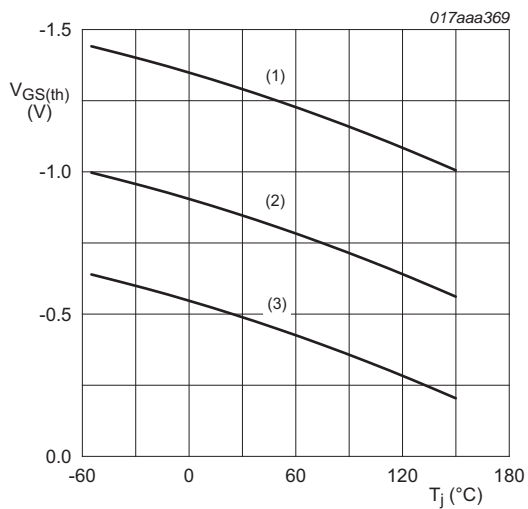
$V_{DS} > I_D \times R_{DS(on)}$   
 (1)  $T_j = 25\text{ °C}$   
 (2)  $T_j = 150\text{ °C}$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



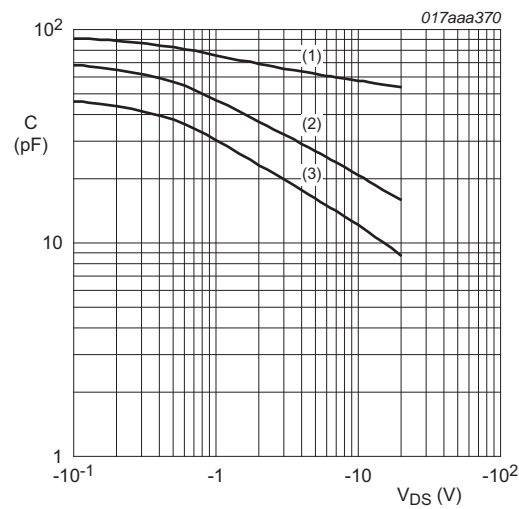
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ °C})}}$$

Fig 11. Normalized drain-source on-state resistance as a function of ambient temperature; typical values



$I_D = -0.25\text{ mA}; V_{DS} = V_{GS}$   
 (1) maximum values  
 (2) typical values  
 (3) minimum values

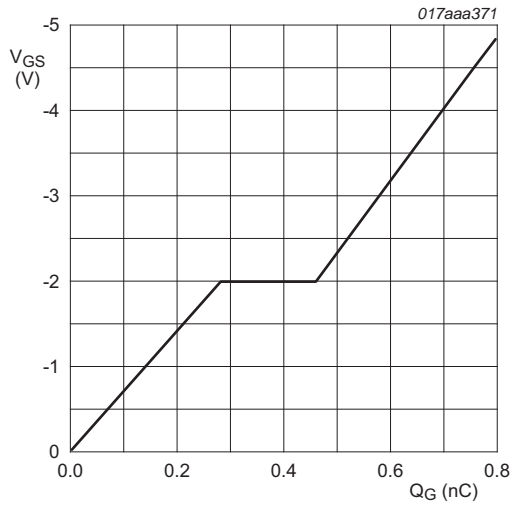
Fig 12. Gate-source threshold voltage as a function of junction temperature



$f = 1\text{ MHz}; V_{GS} = 0\text{ V}$   
 (1)  $C_{iss}$   
 (2)  $C_{oss}$   
 (3)  $C_{rss}$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values





$I_D = -0.4 \text{ A}; V_{DD} = -10 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig 14. Gate-source voltage as a function of gate charge; typical values

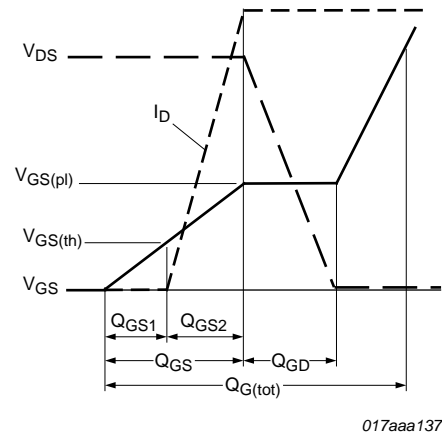
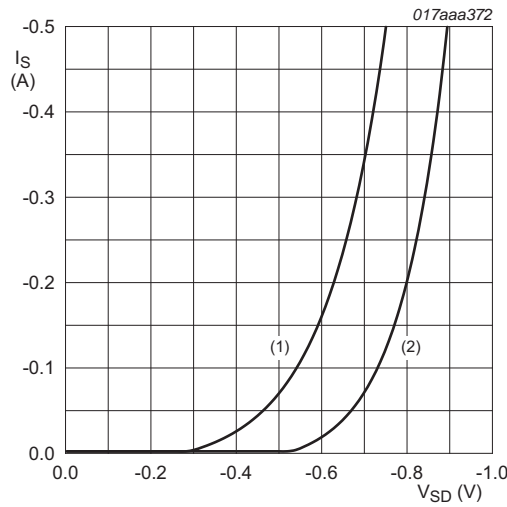


Fig 15. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$   
 (1)  $T_{amb} = 150 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$

Fig 16. Source current as a function of source-drain voltage; typical values

## 8. Test information

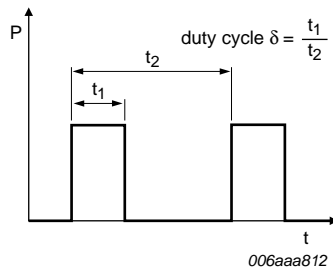


Fig 17. Duty cycle definition

### 8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

9. Package outline

Plastic surface-mounted package; 3 leads

SOT416

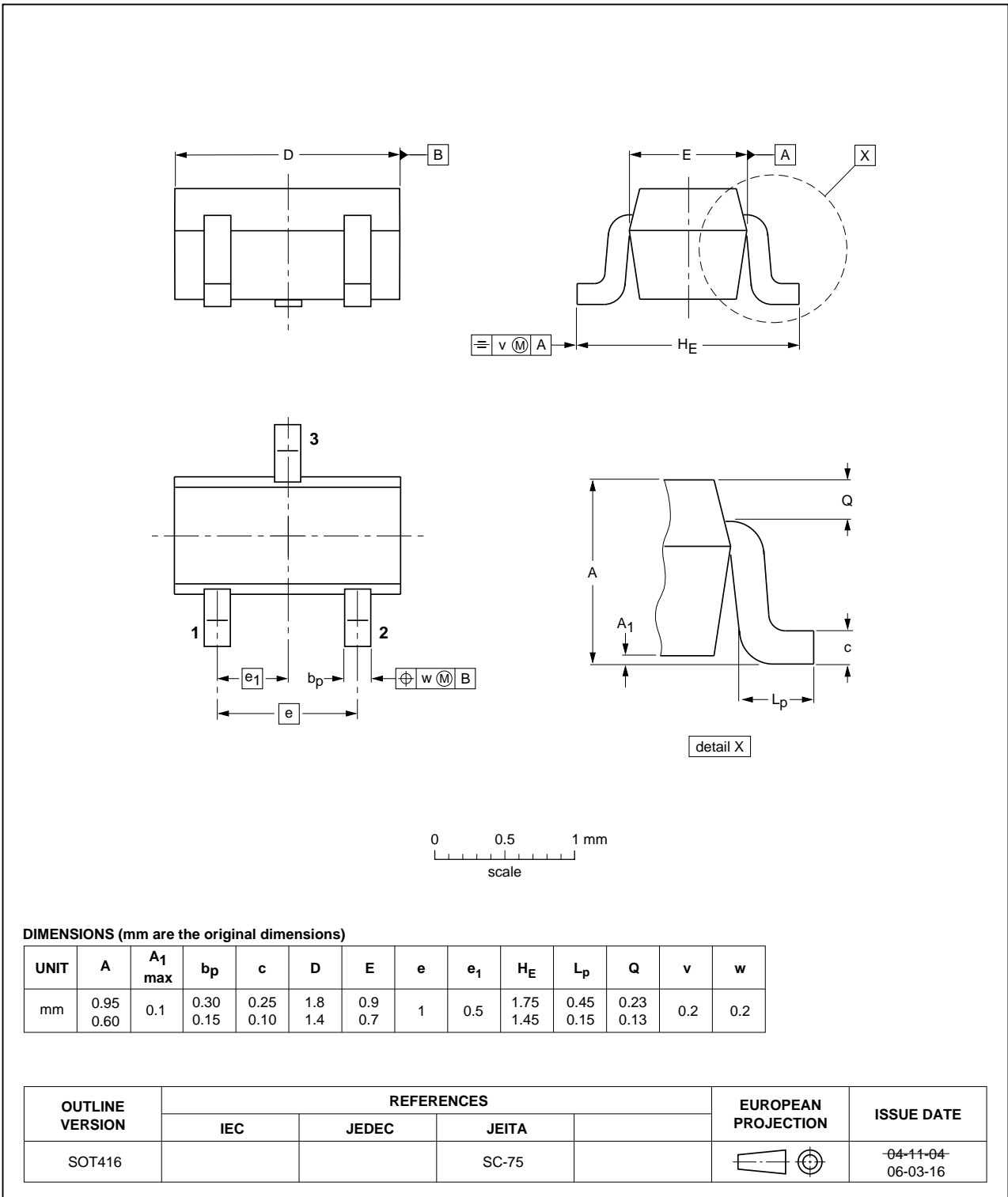


Fig 18. Package outline SOT416 (SC-75)

10. Soldering

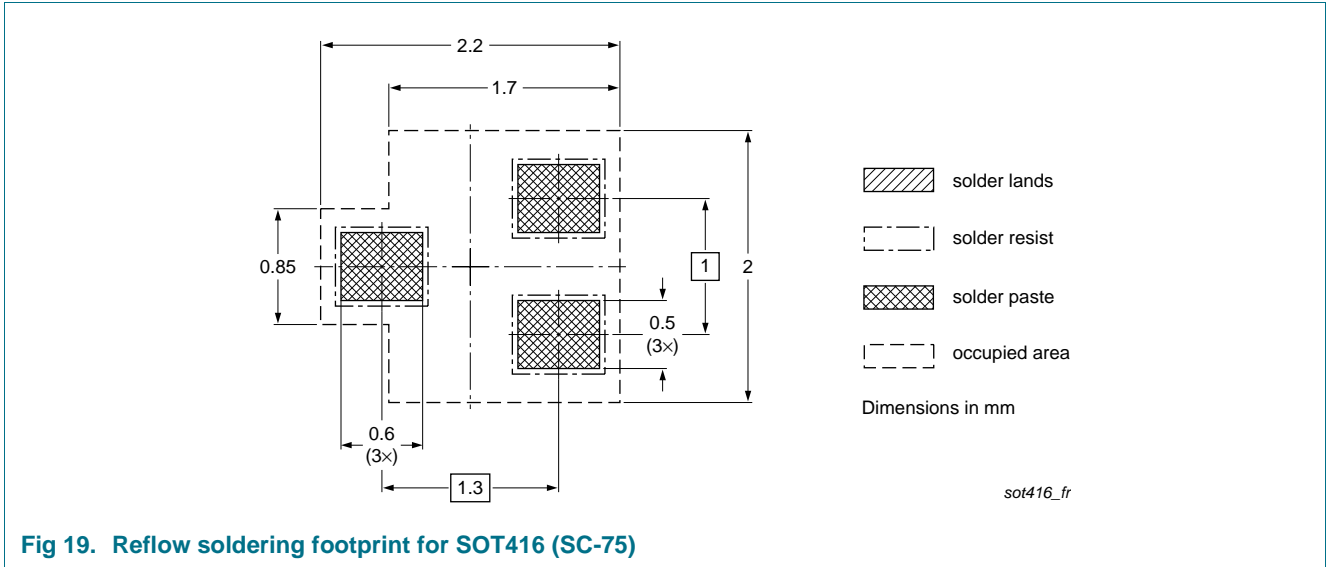


Fig 19. Reflow soldering footprint for SOT416 (SC-75)

## 11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMR670UPE v.1	20110913	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <a href="#">[1]</a> <a href="#">[2]</a>	Product status <a href="#">[3]</a>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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