

**MJ423**

# High-Voltage NPN Silicon Transistor

... designed for medium-to-high voltage inverters, converters, regulators and switching circuits.

- High Voltage —  $V_{CEX} = 400$  Vdc
- Gain Specified to 3.5 Amp
- High Frequency Response to 2.5 MHz

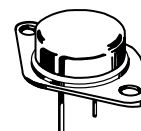
**10 AMPERE  
POWER TRANSISTOR  
NPN SILICON  
400 VOLTS  
125 WATTS**

## MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEX}$	400	Vdc
Collector-Base Voltage	$V_{CB}$	400	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current — Continuous	$I_C$	10	Adc
Base Current	$I_B$	2.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	125 1.0	Watts W/ $^\circ\text{C}$
Operating Junction Temperature Range	$T_J$	-65 to +150	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +200	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	1.0	$^\circ\text{C}/\text{W}$



**CASE 1-07  
TO-204AA  
(TO-3)**

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage* (1) ( $I_C = 100$ mAdc, $I_B = 0$ )	$V_{(BR)CEO(sus)}$	325	—	Vdc
Collector Cutoff Current ( $V_{CE} = 400$ Vdc, $V_{EB(off)} = 1.5$ Vdc) ( $V_{CE} = 400$ Vdc, $V_{EB(off)} = 1.5$ Vdc, $T_C = 125^\circ\text{C}$ )	$I_{CEX}$	— —	0.25 0.5	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0$ Vdc, $I_C = 0$ )	$I_{EBO}$	—	5.0	mAdc

### ON CHARACTERISTICS

DC Current Gain(1) ( $I_C = 1.0$ Adc, $V_{CE} = 5.0$ Vdc) ( $I_C = 2.5$ Adc, $V_{CE} = 5.0$ Vdc)	$h_{FE}$	30 10	90 —	—
Collector-Emitter Saturation Voltage (1) ( $I_C = 1.0$ Adc, $I_B = 0.10$ Adc)	$V_{CE(sat)}$	—	0.8	Vdc
Base-Emitter Saturation Voltage ( $I_C = 1.0$ Adc, $I_B = 0.1$ Adc)	$V_{BE(sat)}$	—	1.25	Vdc

### DYNAMIC CHARACTERISTICS

Current-Gain — Bandwidth Product ( $I_C = 200$ mAdc, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)	$f_T$	2.5	—	MHz
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(1)  $PW \leq 300$   $\mu\text{s}$  Duty Cycle  $\leq 2.0\%$ .

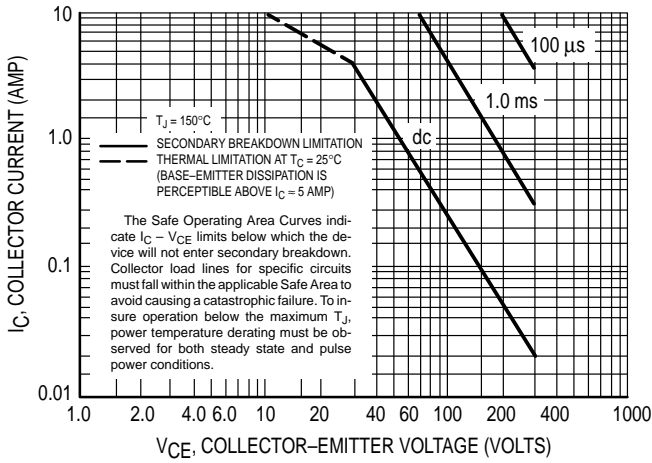


Figure 1. Active-Region Safe-Operating Area

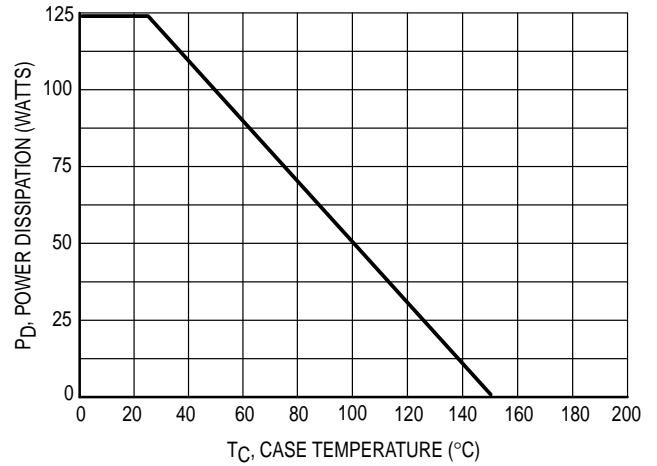


Figure 2. Power-Temperature Derating Curve

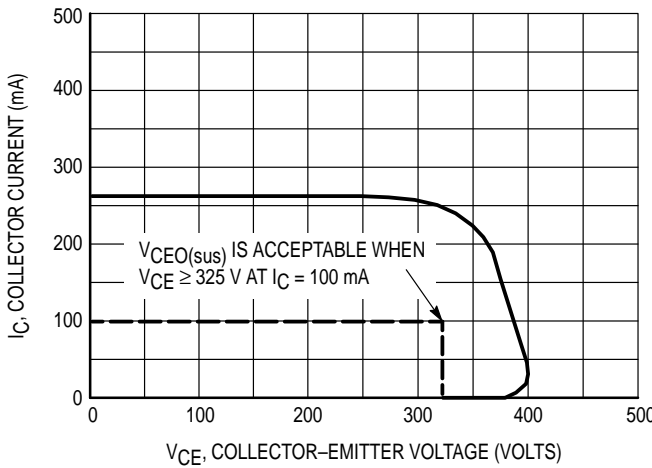


Figure 3. Sustaining Voltage Test Load Line

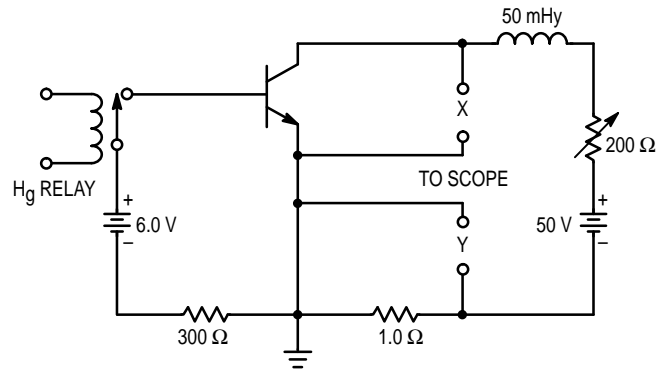


Figure 4. Sustaining Voltage Test Circuit

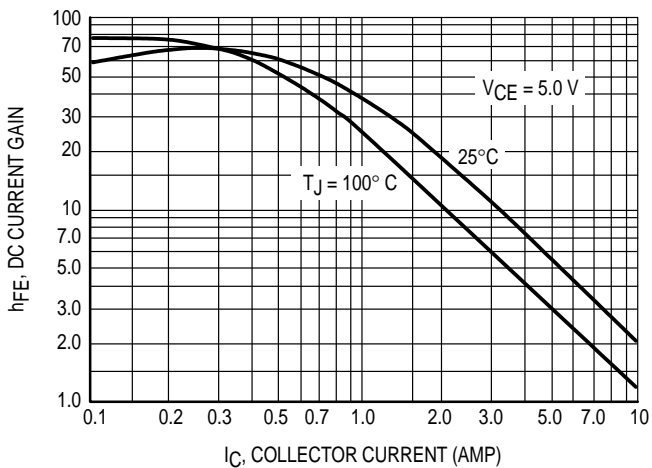


Figure 5. Current Gain

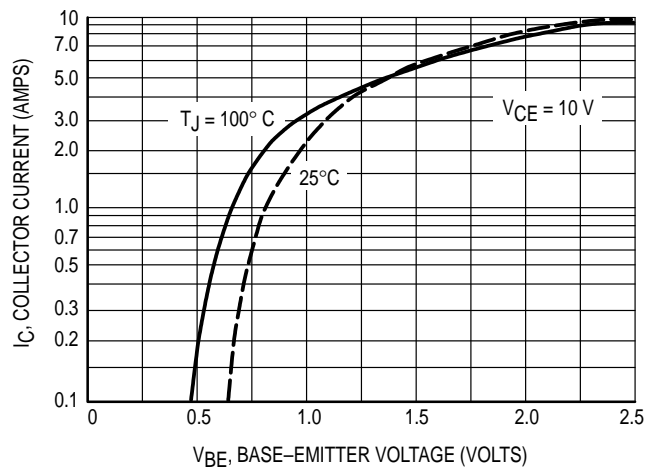
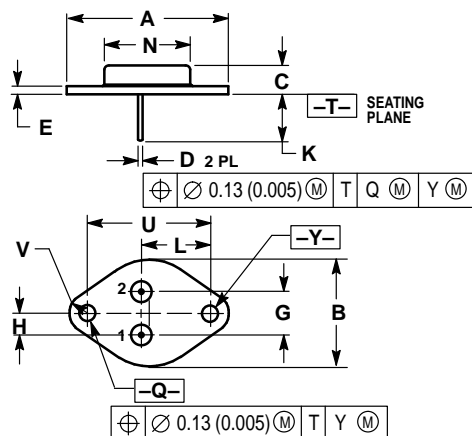


Figure 6. Transconductance

PACKAGE DIMENSIONS




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:  
 PIN 1. BASE  
 2. EMITTER  
 CASE: COLLECTOR

CASE 1-07  
 TO-204AA (TO-3)  
 ISSUE Z

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