MJD44H11, NJVMJD44H11 (NPN) MJD45H11, NJVMJD45H11 (PNP)

Complementary Power Transistors

DPAK For Surface Mount Applications

Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, converters, and power amplifiers.

Features

- Lead Formed for Surface Mount Application in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“−1” Suffix)
- Electrically Similar to Popular D44H/D45H Series
- Low Collector Emitter Saturation Voltage − $V_{CE(sat)}$ = 1.0 Volt Max @ 8.0 A
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs
- Epoxy Meets UL 94 V−0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V
- AEC−Q101 Qualified and PPAP Capable − NJVMJD44H11, NJVMJD45H11
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- These are Pb−Free Packages

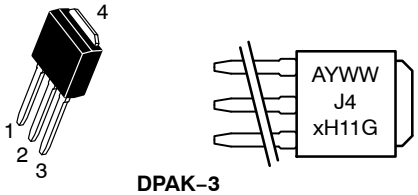
ON Semiconductor®

http://onsemi.com

SILICON
POWER TRANSISTORS
8 AMPERES
80 VOLTS, 20 WATTS

MARKING DIAGRAMS

DPAK
CASE 369C
STYLE 1



DPAK−3
CASE 369D
STYLE 1

A	=	Assembly Location
Y	=	Year
WW	=	Work Week
J4xH11	=	Device Code x = 4 or 5
G	=	Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Emitter Voltage	V_{CEO}	80	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
Collector Current − Continuous − Peak	I_C	8 16	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 20 0.16	W W/°C
Total Power Dissipation (Note 1) @ T_A = 25°C Derate above 25°C	P_D	 1.75 0.014	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction−to−Ambient (Note 1)	$R_{\theta JA}$	71.4	°C/W
Lead Temperature for Soldering	T_L	260	°C

1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage (I_C = 30 mA, I_B = 0)		$V_{CEO(sus)}$	80			Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)		I_{CES}			1.0	μA
Emitter Cutoff Current (V_{EB} = 5 Vdc)		I_{EBO}			1.0	μA
ON CHARACTERISTICS						
Collector−Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.4 Adc)		$V_{CE(sat)}$			1	Vdc
Base−Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc)		$V_{BE(sat)}$			1.5	Vdc
DC Current Gain (V_{CE} = 1 Vdc, I_C = 2 Adc)		h_{FE}	60			–
DC Current Gain (V_{CE} = 1 Vdc, I_C = 4 Adc)			40			
DYNAMIC CHARACTERISTICS						
Collector Capacitance (V_{CB} = 10 Vdc, f_{test} = 1 MHz)	MJD44H11, NJVMJD44H11G,/T4G/RLG MJD45H11, NJVMJD45H11T4G/RLG	C_{cb}		45 130		pF
Gain Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 20 MHz)	MJD44H11, NJVMJD44H11G,/T4G/RLG MJD45H11, NJVMJD45H11T4G/RLG	f_T		85 90		MHz
SWITCHING TIMES						
Delay and Rise Times (I_C = 5 Adc, I_{B1} = 0.5 Adc)	MJD44H11, NJVMJD44H11G,/T4G/RLG MJD45H11, NJVMJD45H11T4G/RLG	$t_d + t_r$		300 135		ns
Storage Time (I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	MJD44H11, NJVMJD44H11G,/T4G/RLG MJD45H11, NJVMJD45H11T4G/RLG	t_s		500 500		ns
Fall Time (I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc	MJD44H11, NJVMJD44H11G,/T4G/RLG MJD45H11, NJVMJD45H11T4G/RLG	t_f		140 100		ns

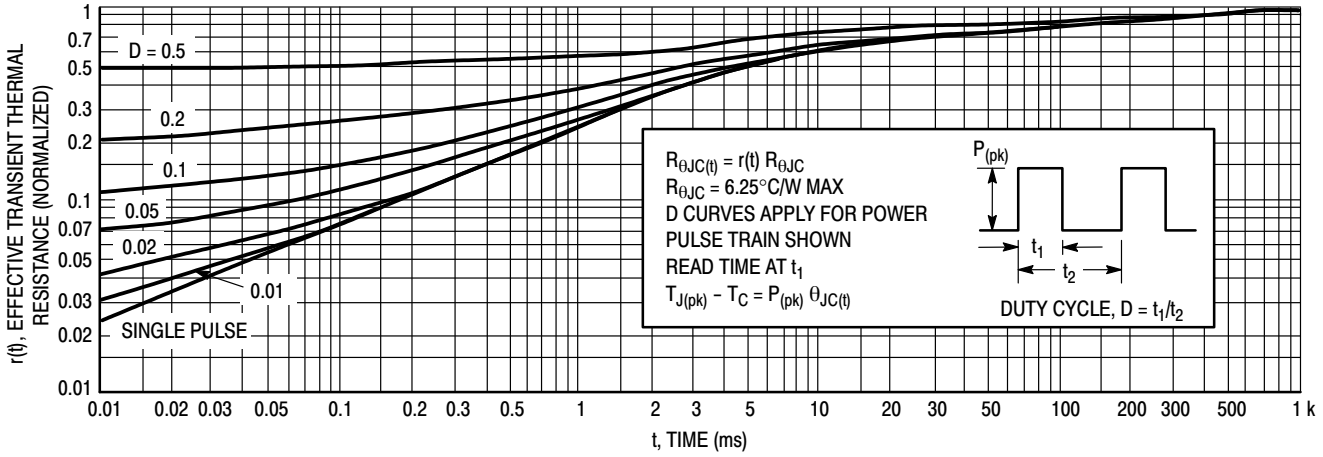


Figure 1. Thermal Response

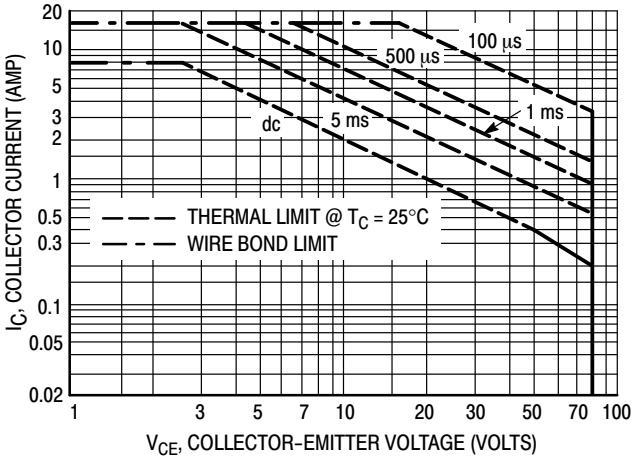


Figure 2. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

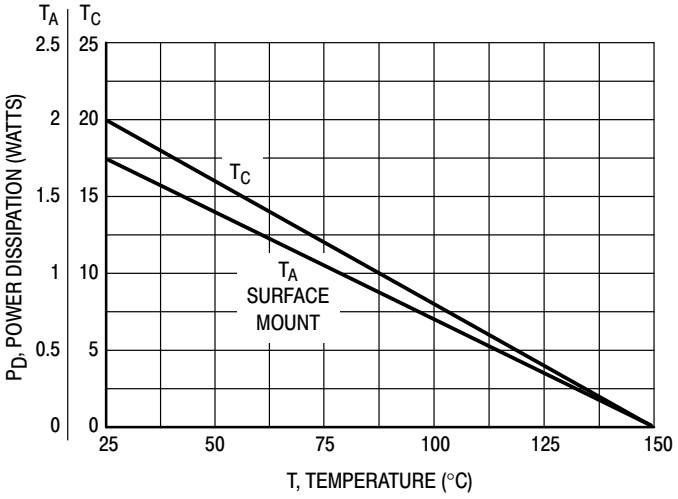


Figure 3. Power Derating

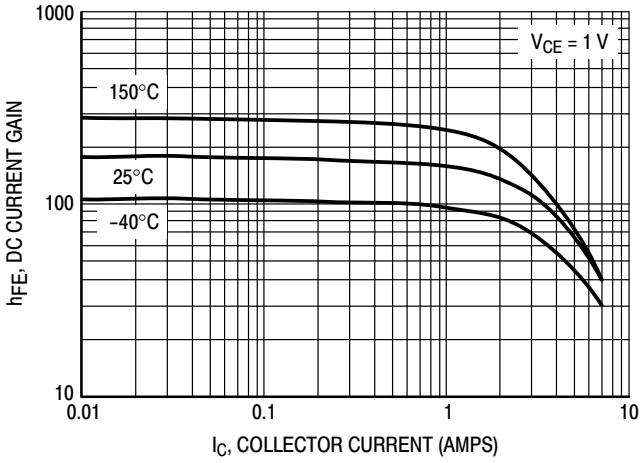


Figure 4. MJD44H11 DC Current Gain

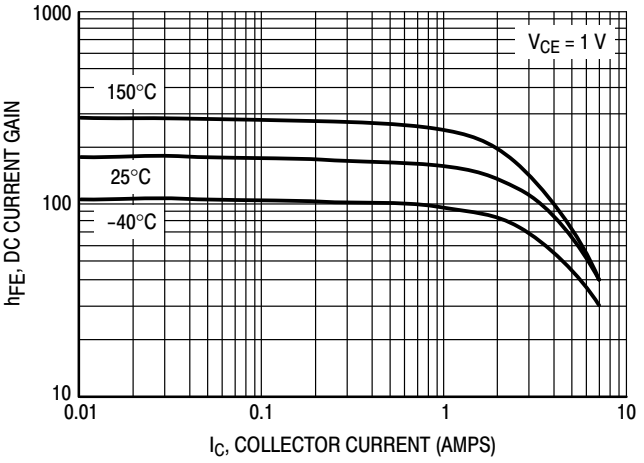


Figure 5. MJD45H11 DC Current Gain

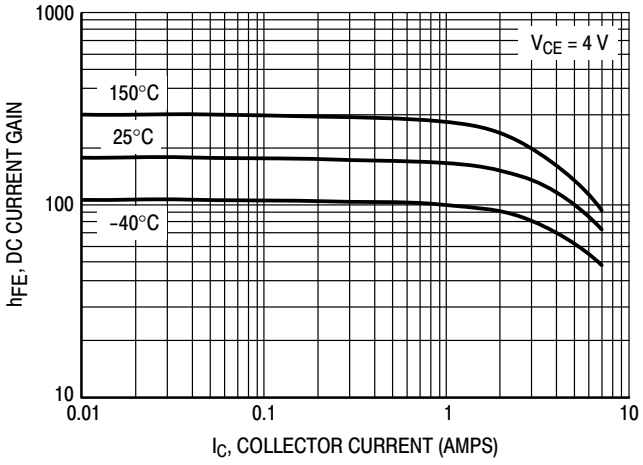


Figure 6. MJD44H11 DC Current Gain

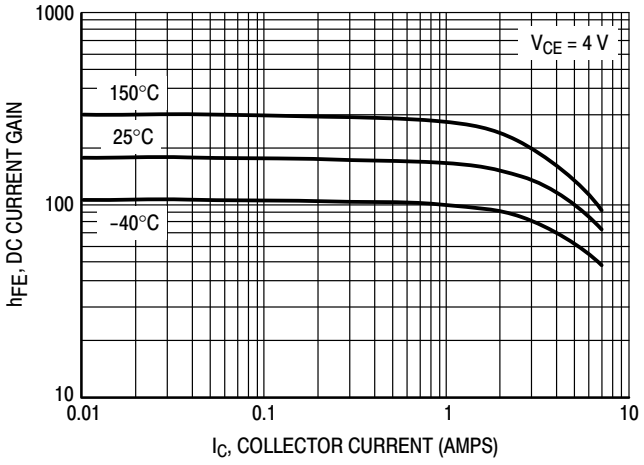


Figure 7. MJD45H11 DC Current Gain

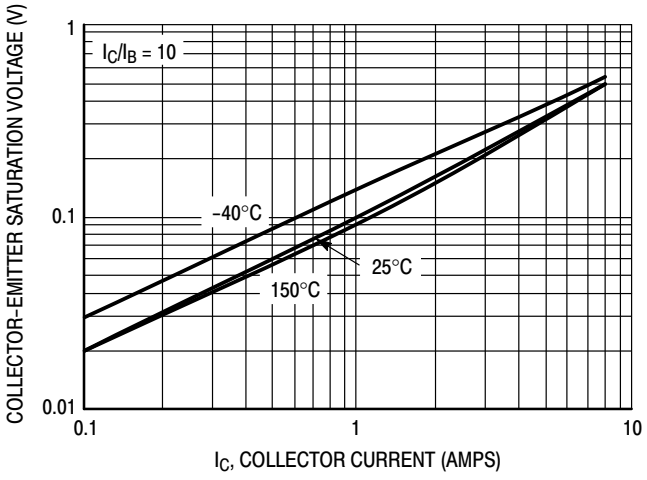


Figure 8. MJD44H11 Saturation Voltage $V_{CE(sat)}$

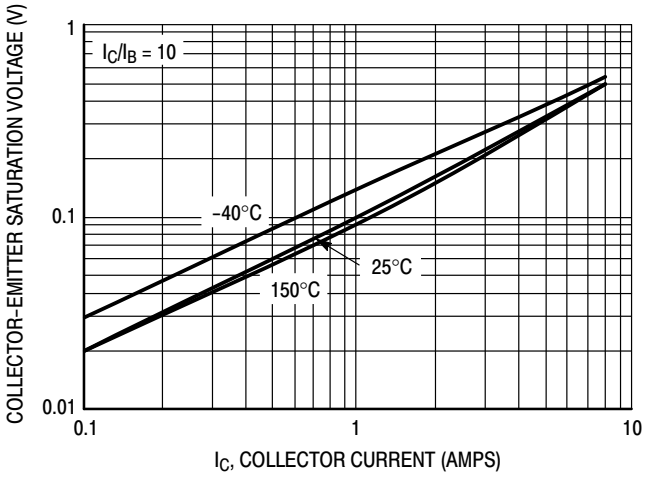


Figure 9. MJD45H11 Saturation Voltage $V_{CE(sat)}$

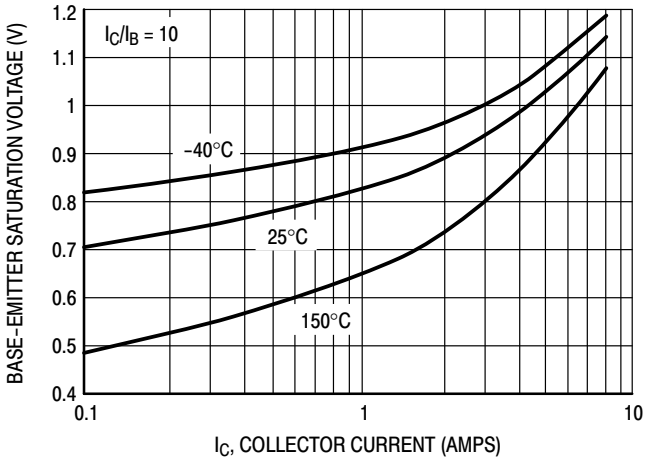


Figure 10. MJD44H11 Saturation Voltage $V_{BE(sat)}$

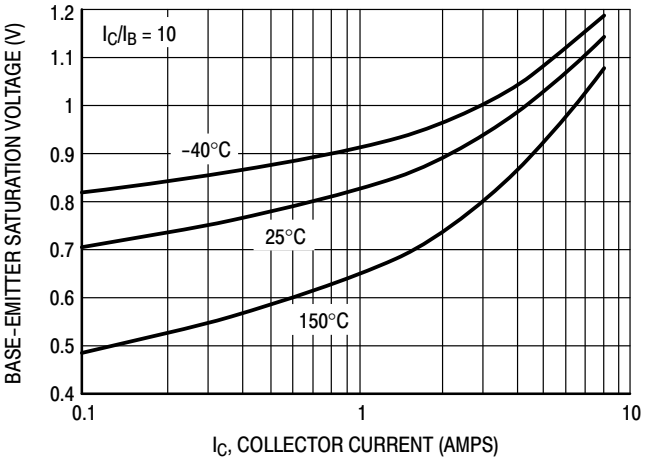


Figure 11. MJD45H11 Saturation Voltage $V_{BE(sat)}$

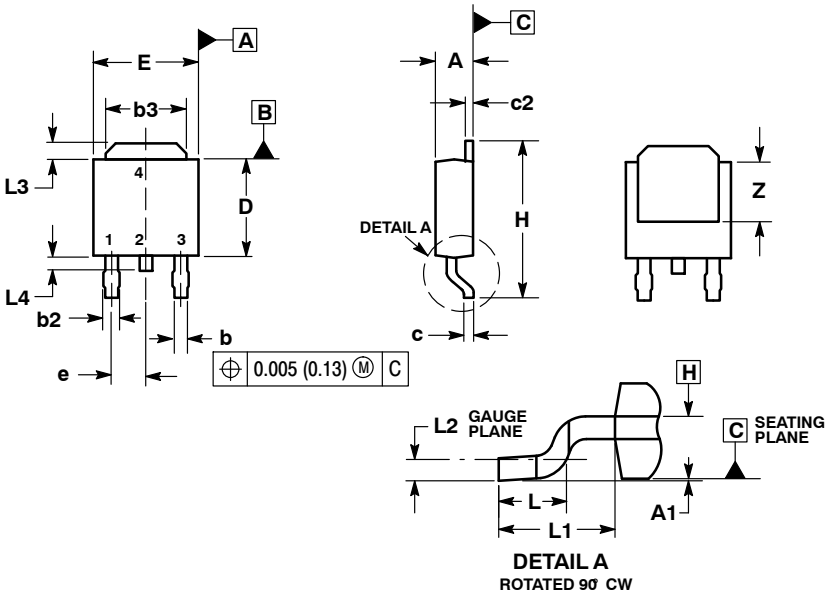
ORDERING INFORMATION

Device	Package Type	Package	Shipping†
MJD44H11G	DPAK (Pb−Free)	369C	75 Units / Rail
NJVMJD44H11G	DPAK (Pb−Free)		
MJD44H11−1G	DPAK−3 (Pb−Free)	369D	
MJD44H11RLG	DPAK (Pb−Free)	369C	1800 / Tape & Reel
NJVMJD44H11RLG	DPAK (Pb−Free)		
MJD44H11T4G	DPAK (Pb−Free)		2500 / Tape & Reel
NJVMJD44H11T4G	DPAK (Pb−Free)		
MJD44H11T5G	DPAK (Pb−Free)		
MJD45H11G	DPAK (Pb−Free)		75 Units / Rail
MJD45H11−1G	DPAK−3 (Pb−Free)	369D	
MJD45H11RLG	DPAK (Pb−Free)	369C	1800 / Tape & Reel
NJVMJD45H11RLG	DPAK (Pb−Free)		
MJD45H11T4	DPAK		2500 / Tape & Reel
MJD45H11T4G	DPAK (Pb−Free)		2500 / Tape & Reel
NJVMJD45H11T4G	DPAK (Pb−Free)		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

DPAK
CASE 369C−01
ISSUE D

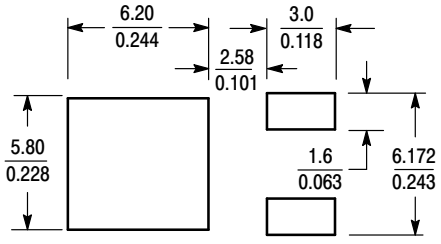


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	−−−	0.040	−−−	1.01
Z	0.155	−−−	3.93	−−−

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*

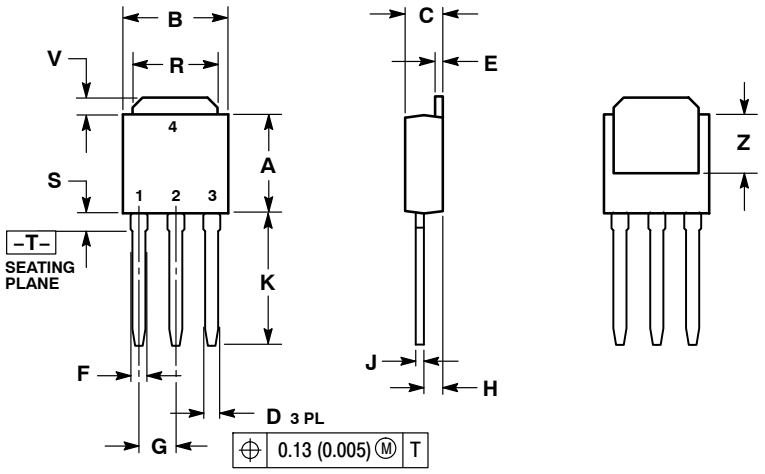


SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

IPAK
CASE 369D−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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Japan Customer Focus Center
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MJD44H11/D