MJD47, NJVMJD47T4G, MJD50

High Voltage Power Transistors

DPAK For Surface Mount Applications

Designed for line operated audio output amplifier, switchmode supply drivers and other switching applications.

Features

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Electrically Similar to Popular TIP47, and TIP50
- 250 and 400 V (Min) − $V_{CEO(sus)}$
- 1 A Rated Collector Current
- Epoxy Meets UL 94 V−0 @ 0.125 in
- ESD Ratings:
  - Human Body Model, 3B > 8000 V
  - Machine Model, C > 400 V
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These are Pb−Free Packages*

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Emitter Voltage MJD47, NJVMJD47T4G MJD50	V_{CEO}	 250 400	Vdc
Collector−Base Voltage MJD47, NJVMJD47T4G MJD50	V_{CB}	 350 500	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
Collector Current Continuous Peak	I_C	 1 2	Adc
Base Current	I_B	0.6	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 15 0.12	 W W/°C
Total Power Dissipation (Note 1) @ T_A = 25°C Derate above 25°C	P_D	 1.56 0.0125	 W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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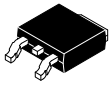
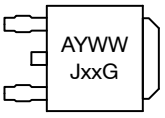
NPN SILICON POWER TRANSISTORS
1 AMPERE
250, 400 VOLTS, 15 WATTS



DPAK
CASE 369C
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
Jxx = Device Code
xx = 47 or 50
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
MJD47G	369C (Pb−Free)	75 Units/Rail
MJD47T4G	369C (Pb−Free)	2,500/Tape & Reel
NJVMJD47T4G	369C (Pb−Free)	2,500/Tape & Reel
MJD50G	369C (Pb−Free)	75 Units/Rail
MJD50T4G	369C (Pb−Free)	2,500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction−to−Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance Junction−to−Ambient (Note 2)	$R_{\theta JA}$	80	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 3) (I_C = 30 mAdc, I_B = 0)	MJD47, NJVMJD47T4G MJD50	$V_{CEO(sus)}$	 250 400	 − −	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 300 Vdc, I_B = 0)	 MJD47, NJVMJD47T4G MJD50	I_{CEO}	 − −	 0.2 0.2	mAdc
Collector Cutoff Current (V_{CE} = 350 Vdc, V_{BE} = 0) (V_{CE} = 500 Vdc, V_{BE} = 0)	 MJD47, NJVMJD47T4G MJD50	I_{CES}	 − −	 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	 −	 1	mAdc
ON CHARACTERISTICS (Note 3)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 10 Vdc) (I_C = 1 Adc, V_{CE} = 10 Vdc)		h_{FE}	 30 10	 150 −	−
Collector−Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)		$V_{CE(sat)}$	 −	 1	Vdc
Base−Emitter On Voltage (I_C = 1 Adc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	 −	 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 2 MHz)		f_T	 10	 −	MHz
Small−Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		h_{fe}	 25	 −	−

3. Pulse Test: Pulse Width $\leq$ 300 μs, Duty Cycle $\leq$ 2%.

TYPICAL CHARACTERISTICS

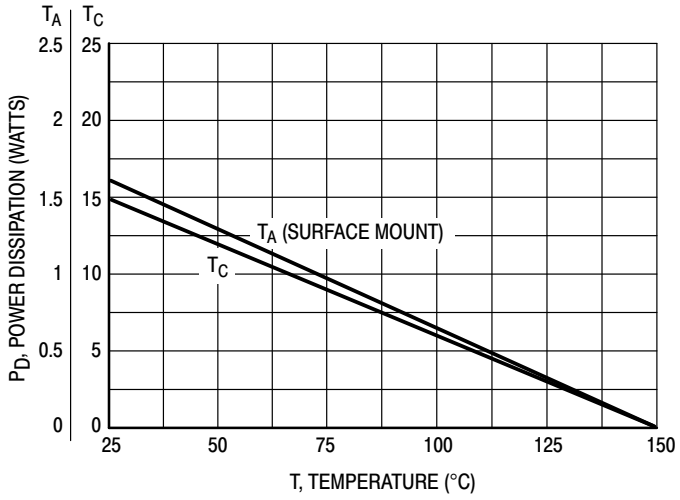


Figure 1. Power Derating

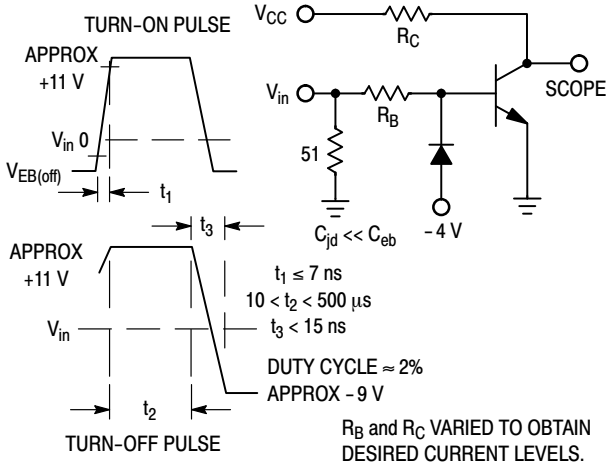


Figure 2. Switching Time Equivalent Circuit

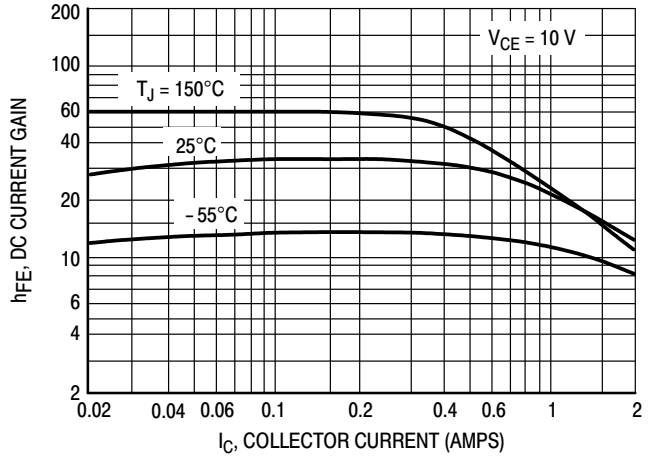


Figure 3. DC Current Gain

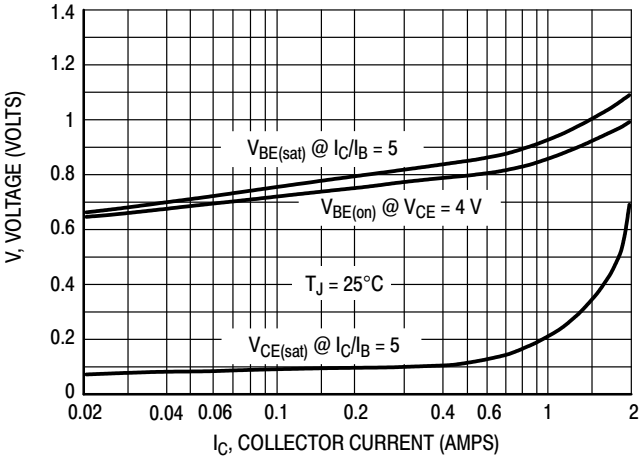


Figure 4. "On" Voltages

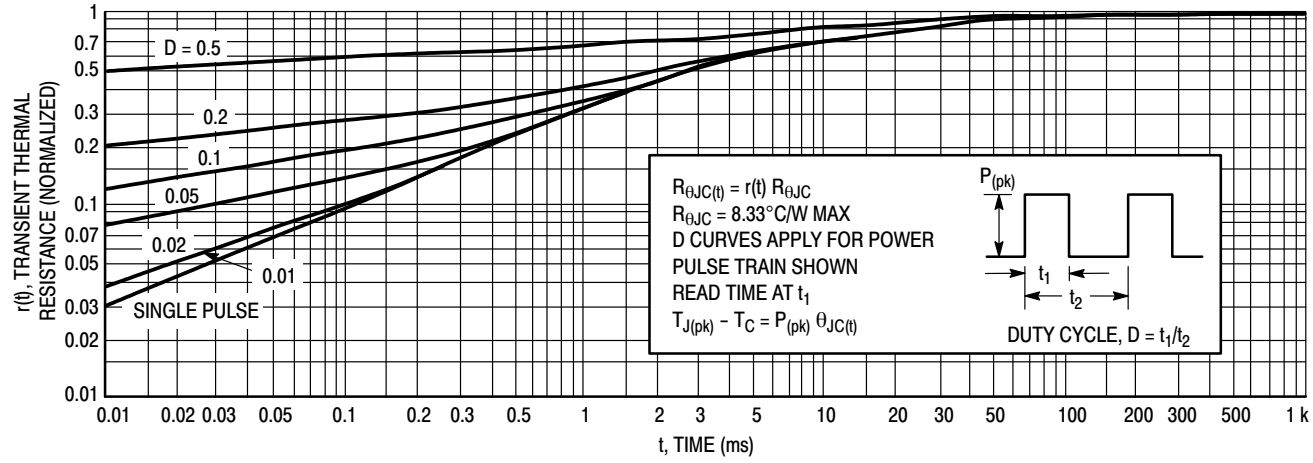


Figure 5. Thermal Response

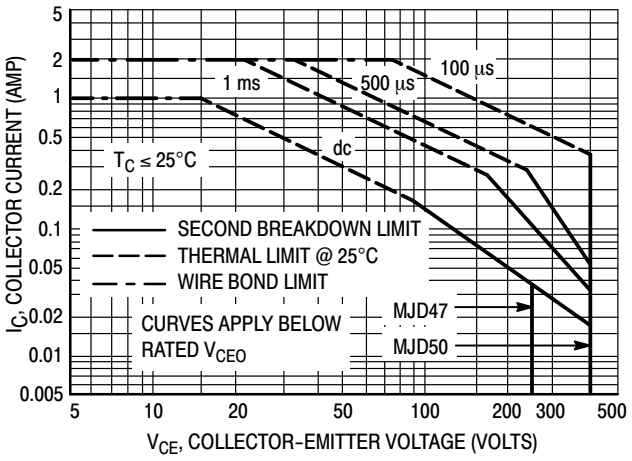


Figure 6. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \le 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

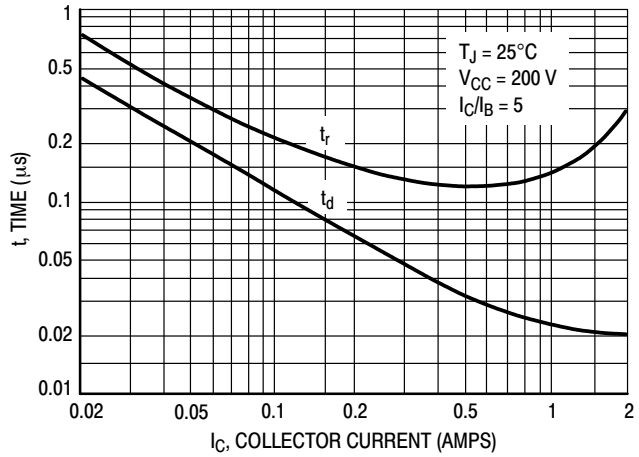


Figure 7. Turn−On Time

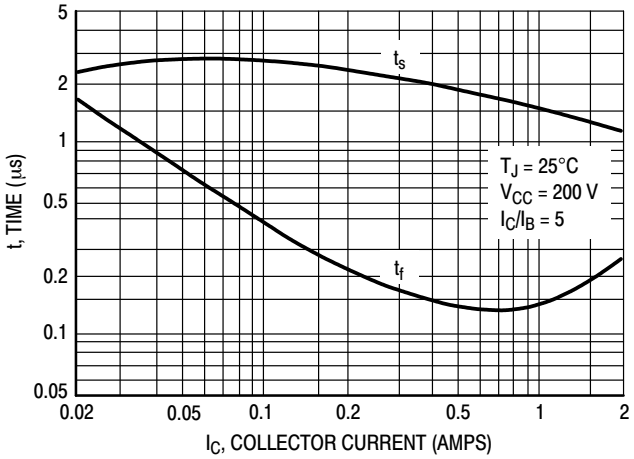
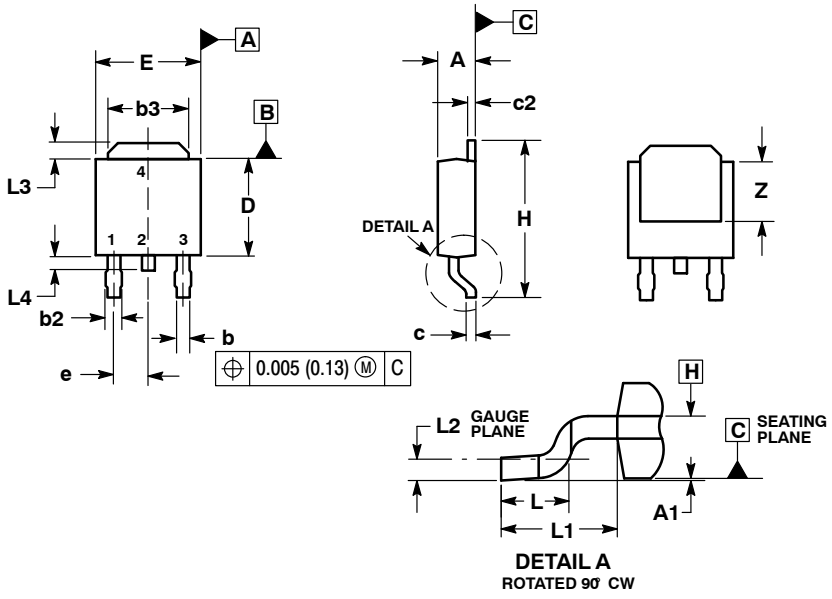


Figure 8. Turn-Off Time

PACKAGE DIMENSIONS

DPAK
CASE 369C
ISSUE D

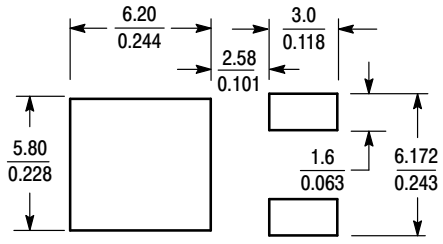


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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Email: orderlit@onsemi.com

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