IXYS

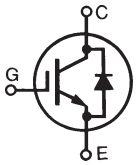
Preliminary Technical Information

High Voltage, High Gain BIMOSFET™ Monolithic Bipolar MOS Transistor

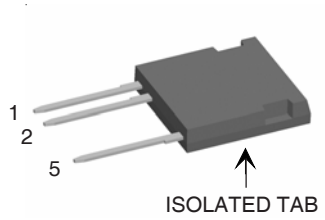
IXBF12N300

V_{CES} = 3000V
I_{C90} = 12A
$V_{CE(sat)} \leq$ 3.2V

(Electrically Isolated Tab)



ISOPLUS i4-Pak™



1 = Gate 5 = Collector
2 = Emitter

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_C = 25°C to 150°C	3000	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	3000	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	T_C = 25°C	22	A
I_{C90}	T_C = 90°C	12	A
I_{CM}	T_C = 25°C, 1ms	100	A
SSOA (RBSOA)	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 30Ω Clamped Inductive Load	I_{CM} = 30 $V_{CES} \leq$ 2400	A V
P_C	T_C = 25°C	100	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6mm (0.062 in.) from Case for 10s	300	°C
T_{SOLD}	Plastic Body for 10 seconds	260	°C
F_C	Mounting Force	20..120 / 4.5..27	Nm/lb.in.
V_{ISOL}	50/60Hz, 1 Minute	3000	V
Weight		5	g

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 250μA, V_{GE} = 0V	3000			V
$V_{GE(th)}$	I_C = 250μA, V_{CE} = V_{GE}	3.0		5.0	V
I_{CES}	V_{CE} = 0.8 • V_{CES}, V_{GE} = 0V			25	μA
	T_J = 125°C			1	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ± 20V			±100	nA
$V_{CE(sat)}$	I_C = 12A, V_{GE} = 15V, Note 1		2.8	3.2	V
	T_J = 125°C		3.5		V

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 3000V Electrical Isolation
- High Blocking Voltage
- Anti-Parallel Diode
- International Standard Package
- Low Conduction Losses

Advantages

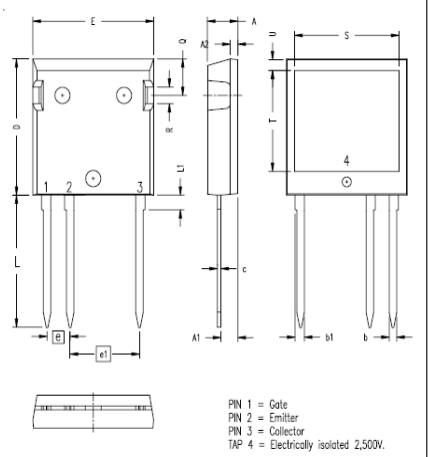
- Low Gate Drive Requirement
- High Power Density

Applications:

- Switched-Mode and Resonant-Mode Power Supplies
- Uninterruptible Power Supplies (UPS)
- Laser Generators
- Capacitor Discharge Circuits
- AC Switches

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	I_C = 12A, V_{CE} = 10V, Note 1	6.5	10.8		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		1290		pF
C_{oes}			56		pF
C_{res}			19		pF
Q_g	I_C = 12A, V_{GE} = 15V, V_{CE} = 1000V		62		nC
Q_{ge}			13		nC
Q_{gc}			8.5		nC
$t_{d(on)}$	**Resistive Switching Times, T_J = 25°C**		64		ns
t_r	I_C = 12A, V_{GE} = 15V		140		ns
$t_{d(off)}$	V_{CE} = 1250V, R_G = 10Ω		180		ns
t_f			540		ns
$t_{d(on)}$	**Resistive Switching Times, T_J = 125°C**		65		ns
t_r	I_C = 12A, V_{GE} = 15V		395		ns
$t_{d(off)}$	V_{CE} = 1250V, R_G = 10Ω		175		ns
t_f			530		ns
R_{thJC}				1.25	°C/W
R_{thCS}	(TO-247)		0.15		°C/W

ISOPLUS i4-Pak™ (HV) (IXBF) Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.102	.118	2.59	3.00
A2	.046	.085	1.17	2.16
b	.045	.055	1.14	1.40
b1	.058	.068	1.47	1.73
C	.020	.029	0.51	0.74
D	.819	.840	20.80	21.34
E	.770	.799	19.56	20.29
e	.150 BSC		3.81 BSC	
e1	.450 BSC		11.43 BSC	
L	.780	.840	19.81	21.34
L1	.083	.102	2.11	2.59
Q	.210	.244	5.33	6.20
R	.100	.180	2.54	4.57
S	.660	.690	16.76	17.53
T	.590	.620	14.99	15.75
U	.065	.080	1.65	2.03

Reverse Diode

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
V_F	I_F = 12A, V_{GE} = 0V			2.1	V
t_{rr}	I_F = 6A, V_{GE} = 0V, -di_F/dt = 100A/μs		1.4		μs
I_{RM}	V_R = 100V, V_{GE} = 0V		21		A

Note 1: Pulse Test, t ≤ 300μs, Duty Cycle, d ≤ 2%.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

Fig. 1. Output Characteristics @ 25ºC

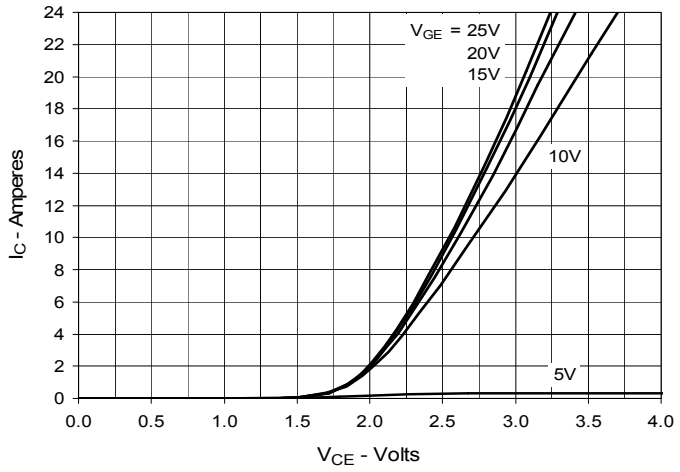


Fig. 2. Extended Output Characteristics @ 25ºC

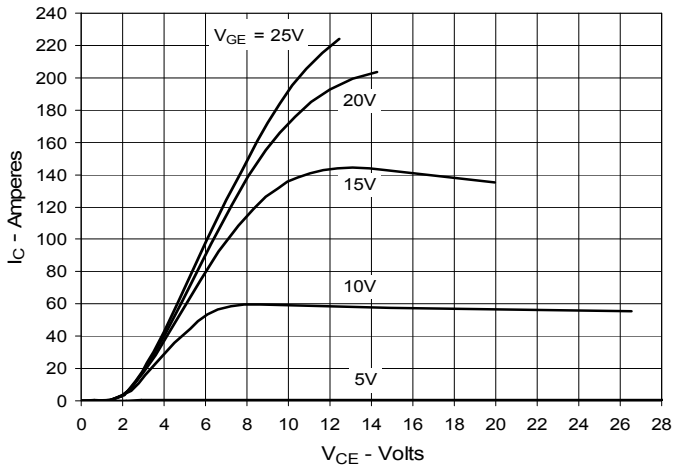


Fig. 3. Output Characteristics @ 125ºC

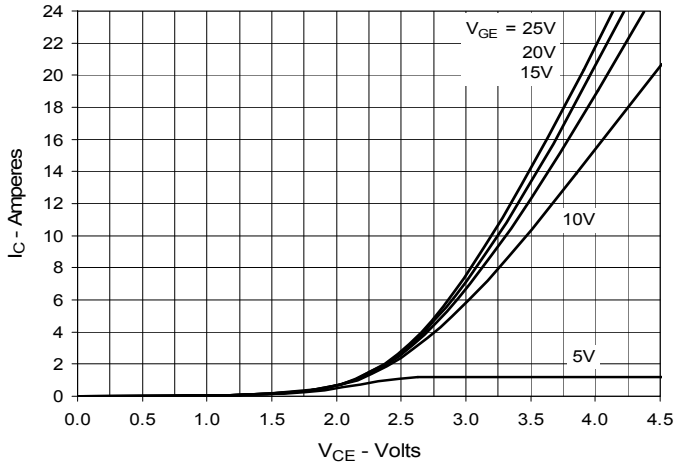


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

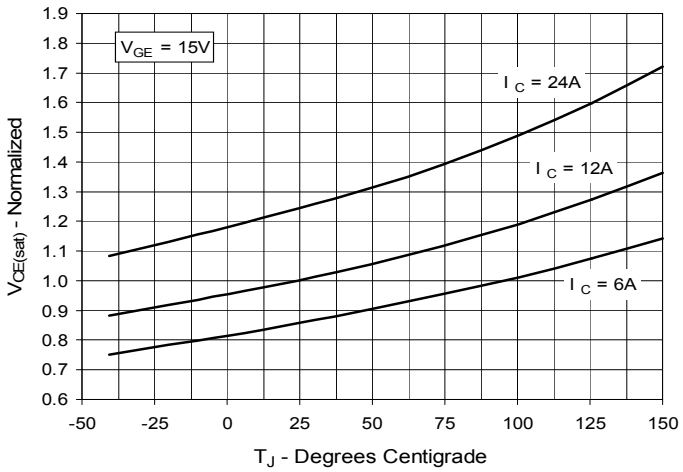


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

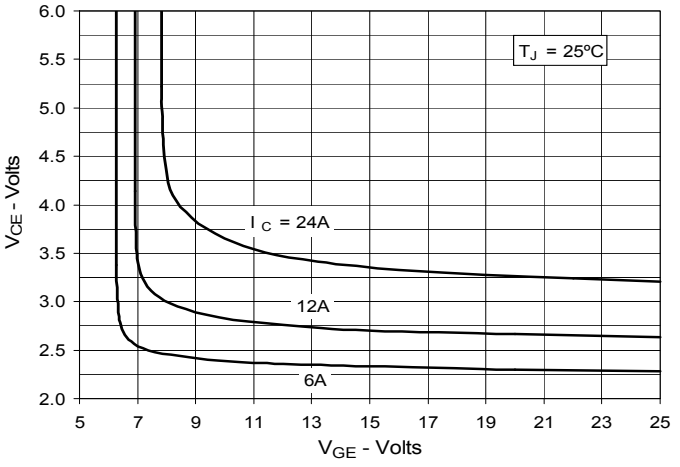


Fig. 6. Input Admittance

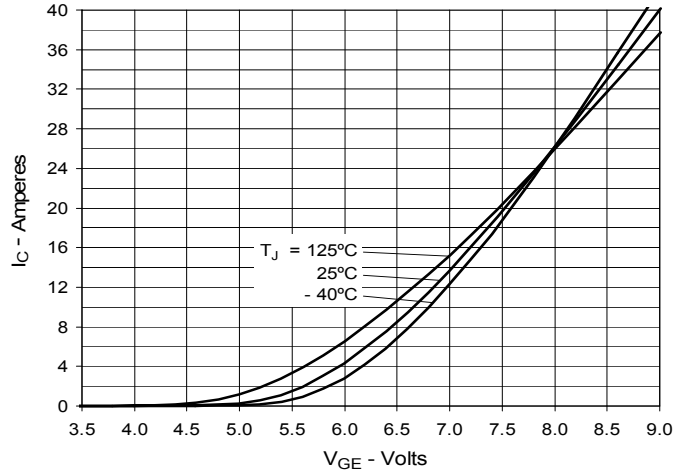


Fig. 7. Transconductance

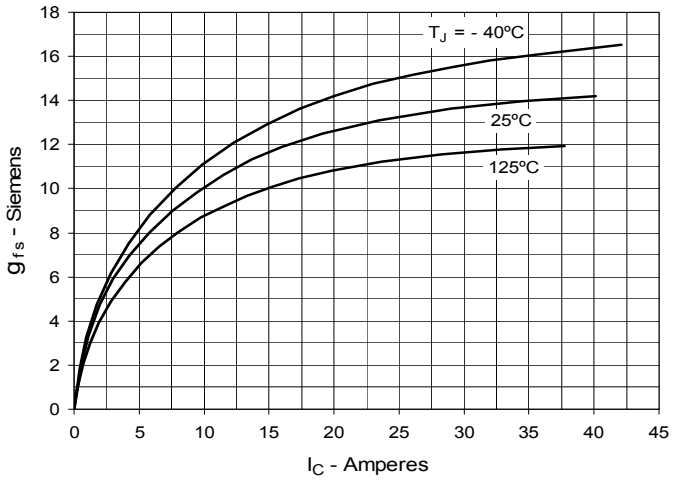


Fig. 8. Forward Voltage Drop of Intrinsic Diode

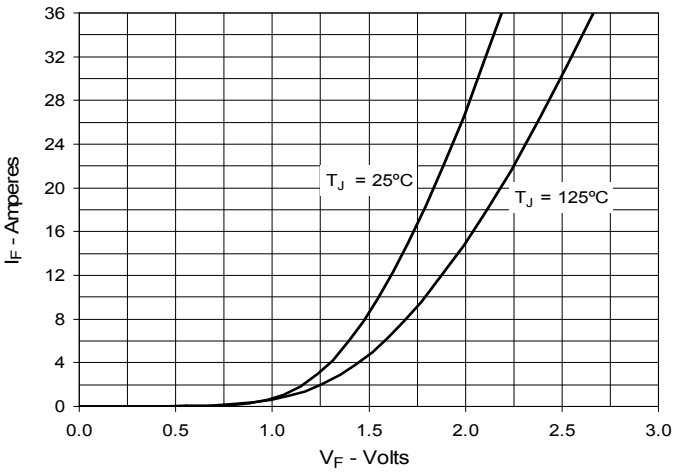


Fig. 9. Gate Charge

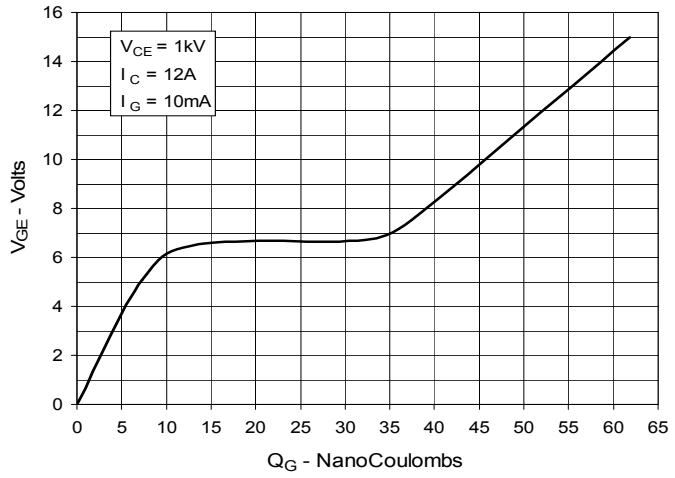


Fig. 10. Capacitance

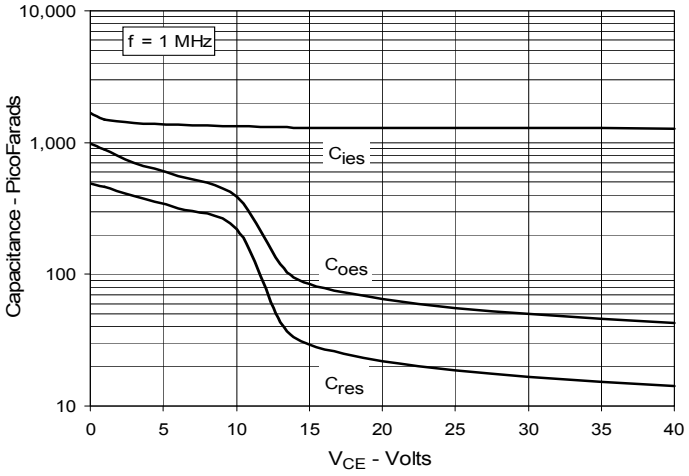


Fig. 11. Reverse-Bias Safe Operating Area

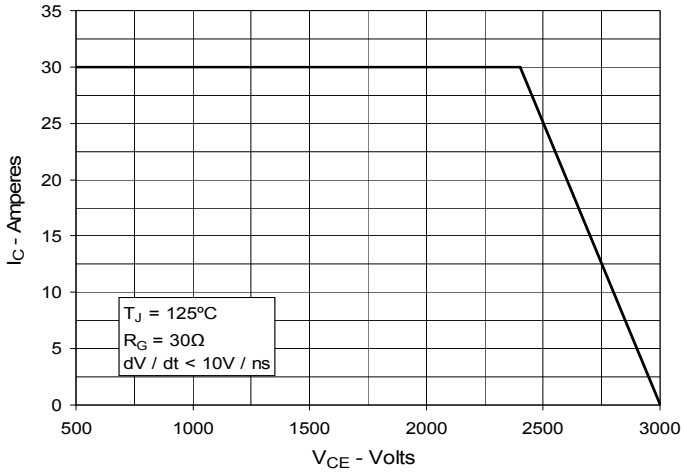


Fig. 12. Maximum Transient Thermal Impedance

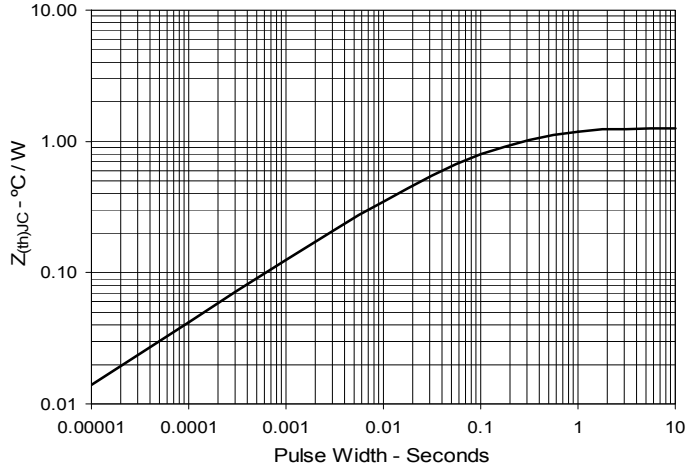


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

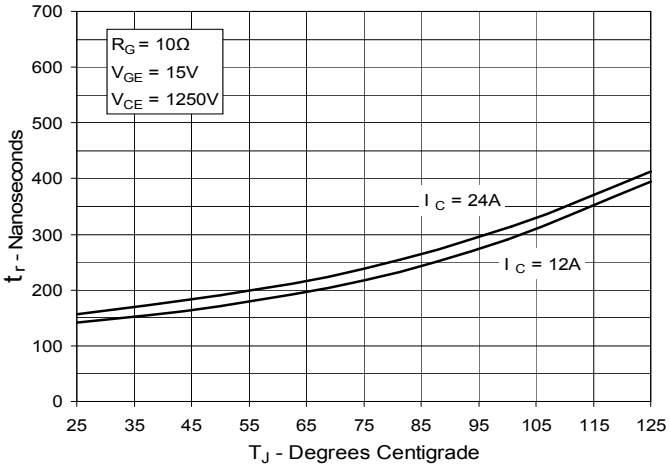


Fig. 14. Resistive Turn-on Rise Time vs. Collector Current

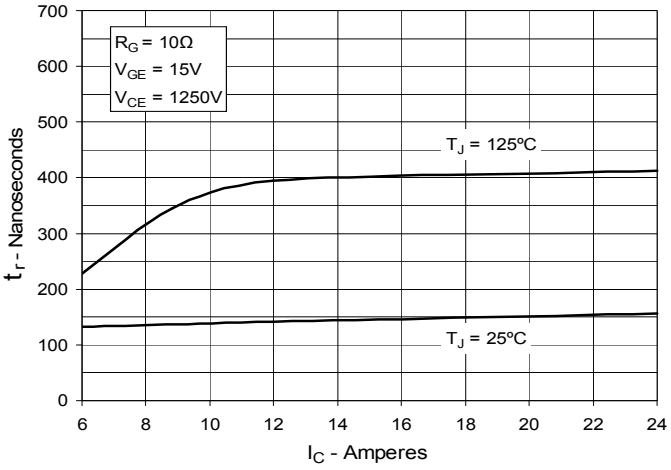


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

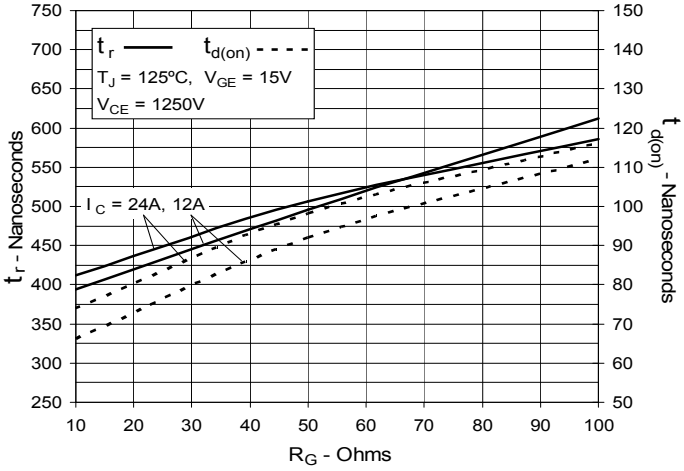


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

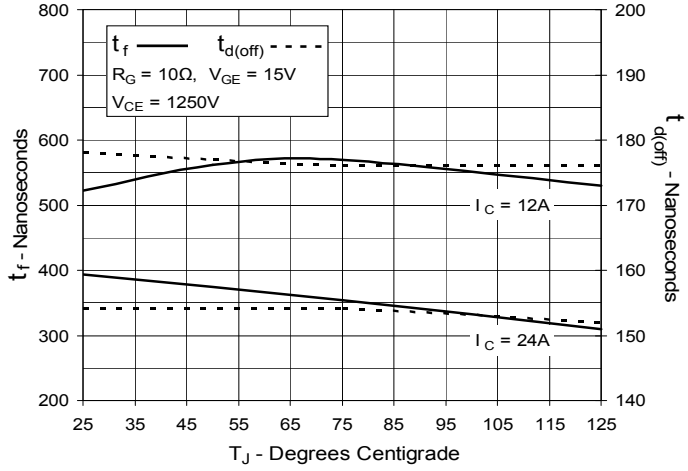


Fig. 17. Resistive Turn-off Switching Times vs. Collector Current

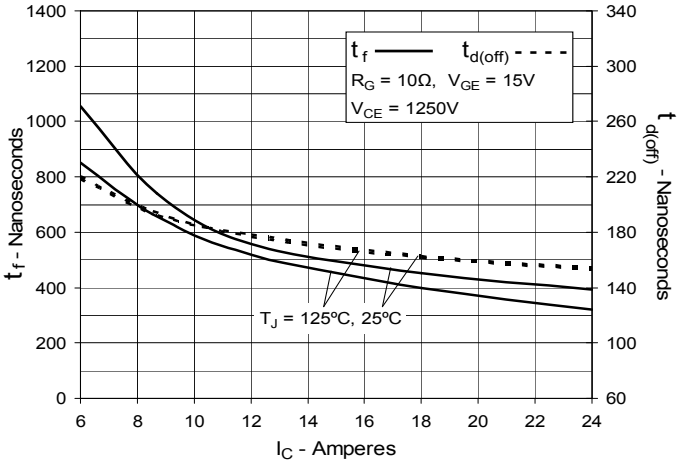


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance