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P1 98.2

# MOS FIELD EFFECT POWER TRANSISTOR 2SK1760

## SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

### DESCRIPTION

The 2SK1760 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

### FEATURES

- Low On-state Resistance  
 $R_{DS(on)} \leq 4.0 \Omega$  ( $V_{GS} = 10 V, I_D = 3 A$ )
- Low  $C_{iss}$   $C_{iss} = 790 pF$  TYP.
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

### QUALITY GRADE

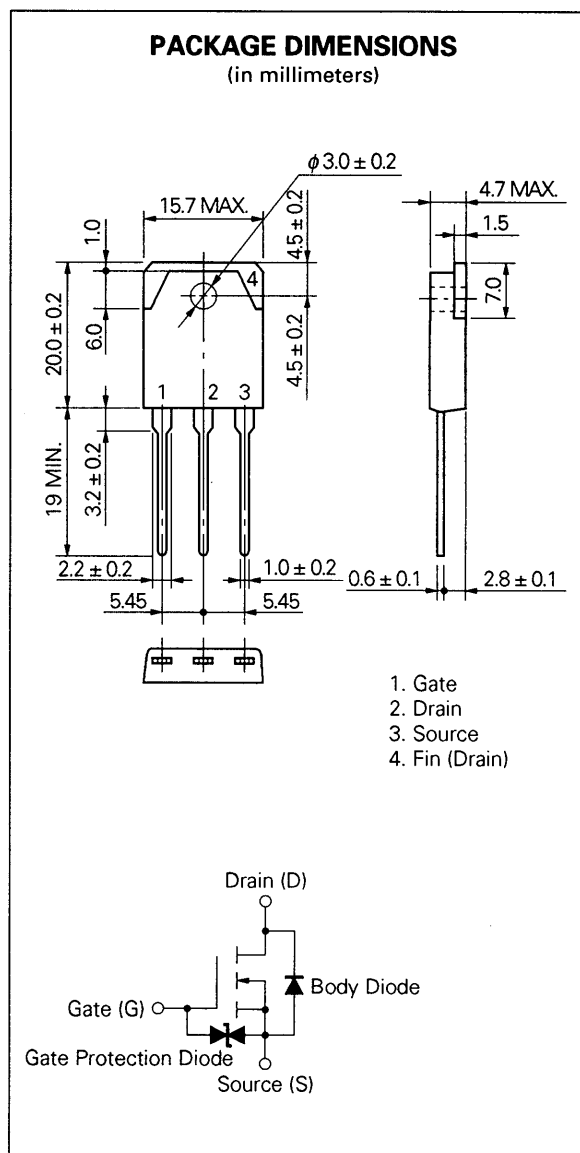
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

### ABSOLUTE MAXIMUM RATINGS ( $T_a = 25^\circ C$ )

Drain to Source Voltage	$V_{DSS}$	900	V
Gate to Source Voltage	$V_{GSS}$	$\pm 30$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 5.0$	A
Drain Current (pulse)	$I_{D(pulse)^*}$	$\pm 10$	A
Total Power Dissipation ( $T_c = 25^\circ C$ )	$P_T$	100	W
Channel Temperature	$T_{ch}$	150	$^\circ C$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ C$

\*  $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1\%$

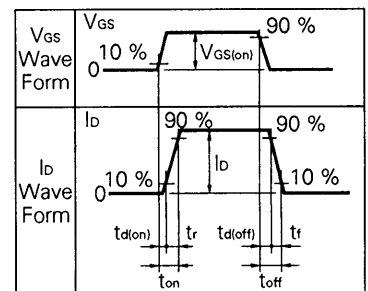
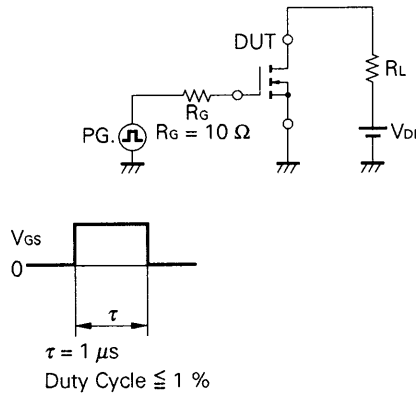
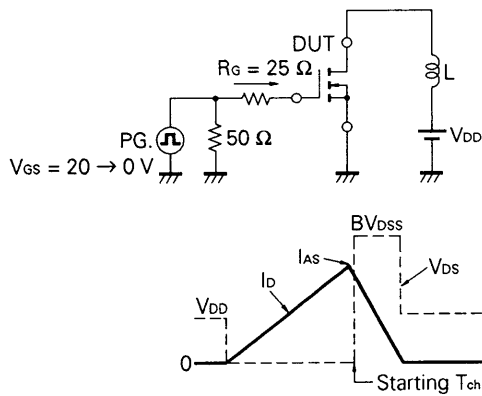


**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

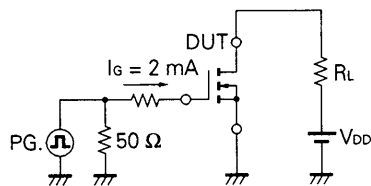
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		3.1	4.0	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	2.5		3.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	1.0	3.1		S	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 3 A
Drain Leakage Current	I <sub>DSS</sub>			100	μA	V <sub>DS</sub> = 900 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		790		pF	V <sub>DS</sub> = 10 V V <sub>GS</sub> = 0 f = 1 MHz
Output Capacitance	C <sub>oss</sub>		150		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>		60		pF	
Turn-On Delay Time	t <sub>d(on)</sub>		15		ns	V <sub>GS</sub> = 10 V V <sub>DD</sub> = 150 V I <sub>D</sub> = 3 A, R <sub>G</sub> = 10 Ω R <sub>L</sub> = 50 Ω
Rise Time	t <sub>r</sub>		30		ns	
Turn-Off Delay Time	t <sub>d(off)</sub>		80		ns	
Fall Time	t <sub>f</sub>		25		ns	
Total Gate Charge	Q <sub>G</sub>		34		nC	V <sub>GS</sub> = 10 V I <sub>D</sub> = 5 A V <sub>DD</sub> = 450 V
Gate to Source Charge	Q <sub>GS</sub>		6		nC	
Gate to Drain Charge	Q <sub>GD</sub>		18		nC	
Diode Forward Voltage	V <sub>F(S-D)</sub>		0.9		V	I <sub>F</sub> = 5 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		660		ns	I <sub>F</sub> = 5 A, V <sub>GS</sub> = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Q <sub>rr</sub>		4.5		μC	
Single Avalanche Current	I <sub>AS</sub>			5.0	A	V <sub>DD</sub> = 150 V, L = 100 μH R <sub>G</sub> = 25 Ω, V <sub>GS</sub> = 20 V → 0 Unclamped Starting T <sub>ch</sub> = 25 °C

**Test Circuit 1: Avalanche Capability**

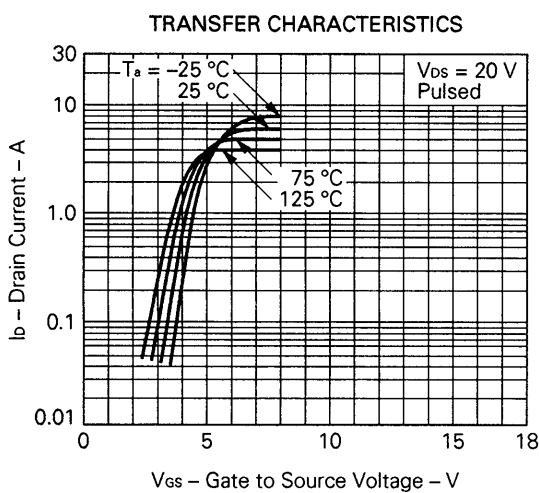
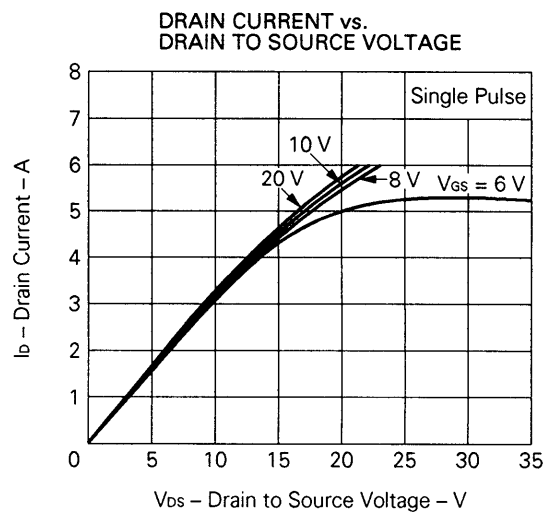
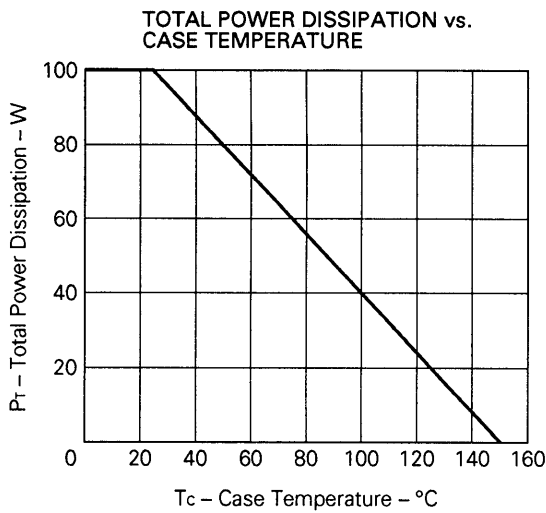
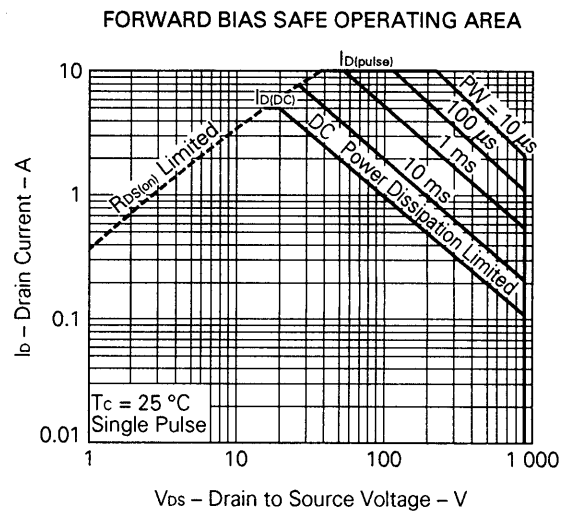
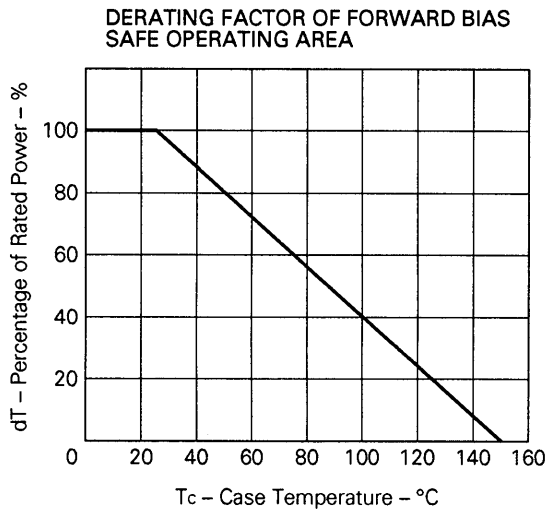
**Test Circuit 2: Switching Time**

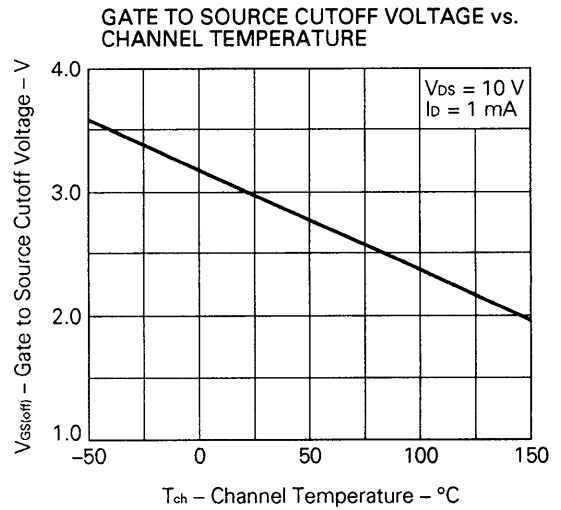
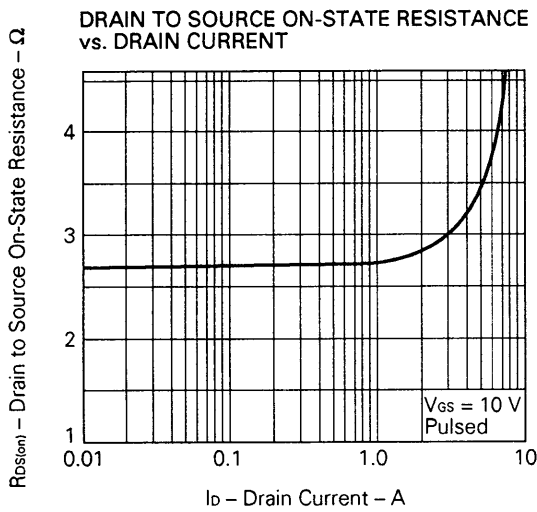
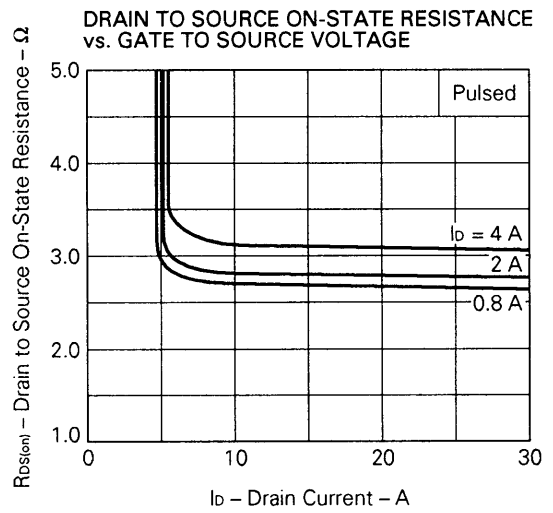
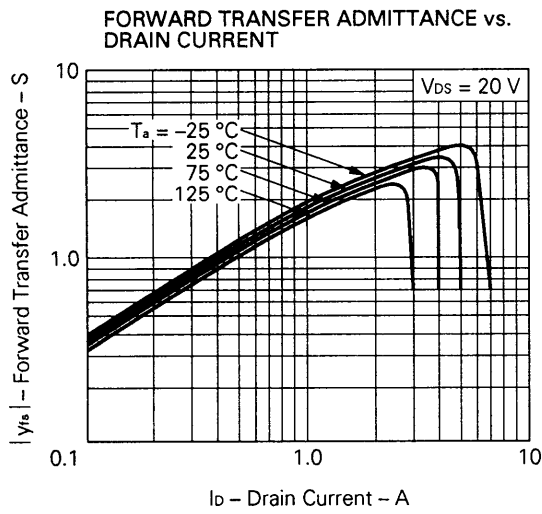
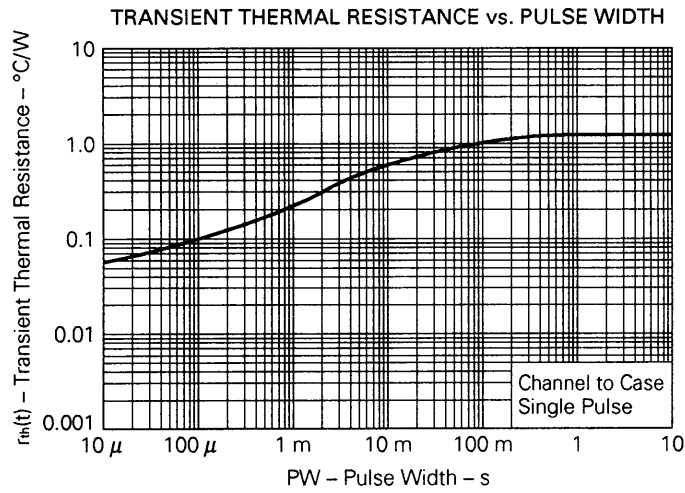


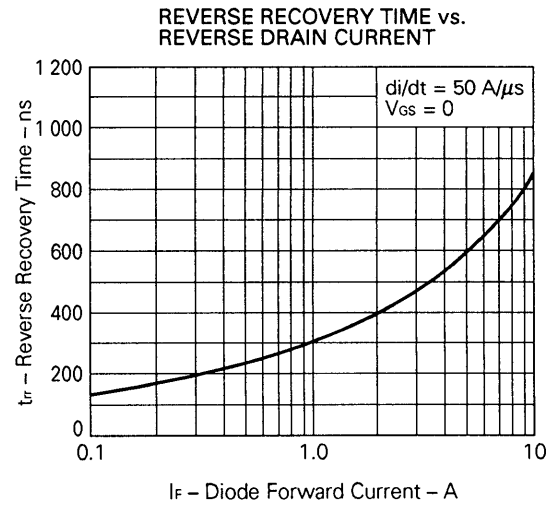
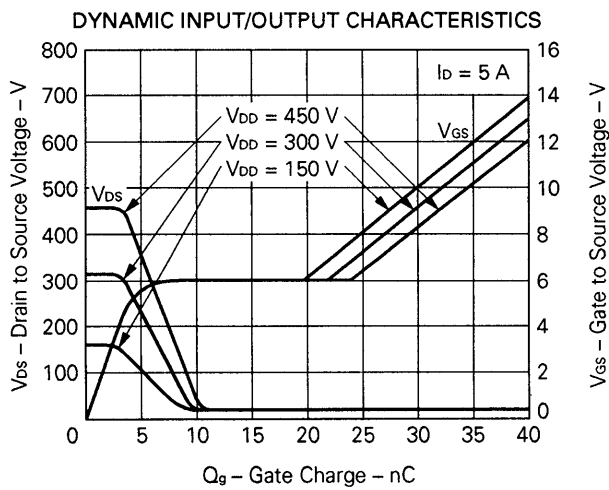
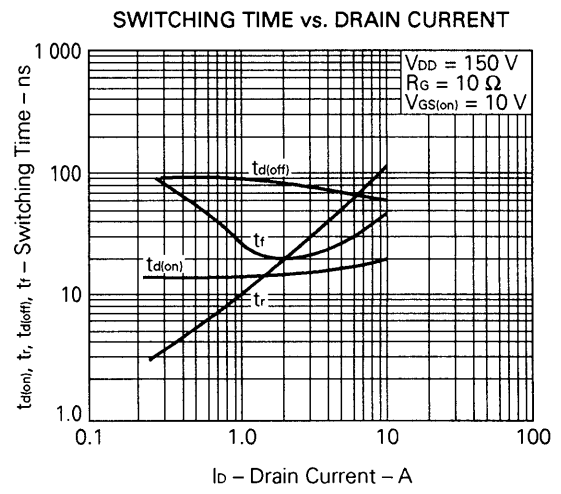
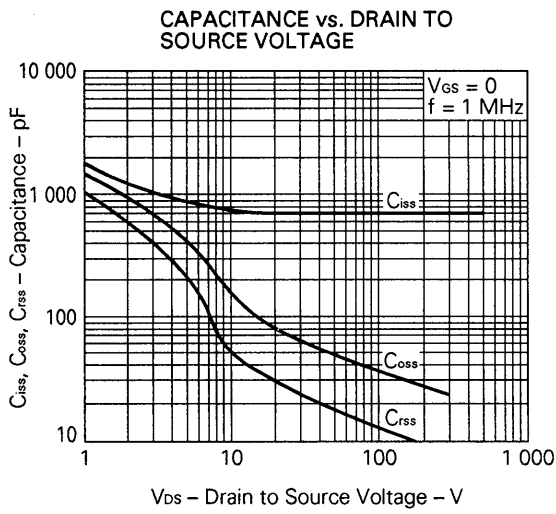
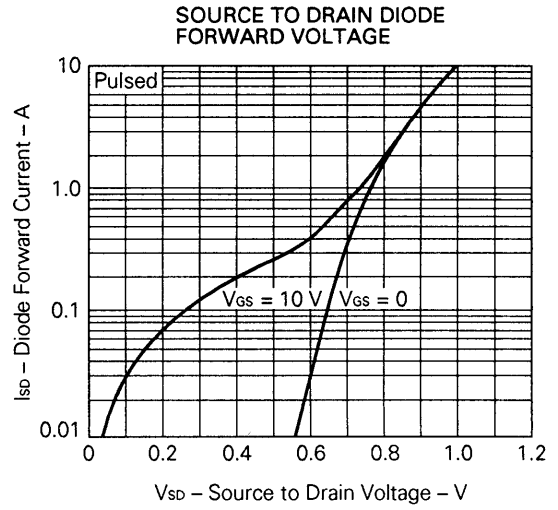
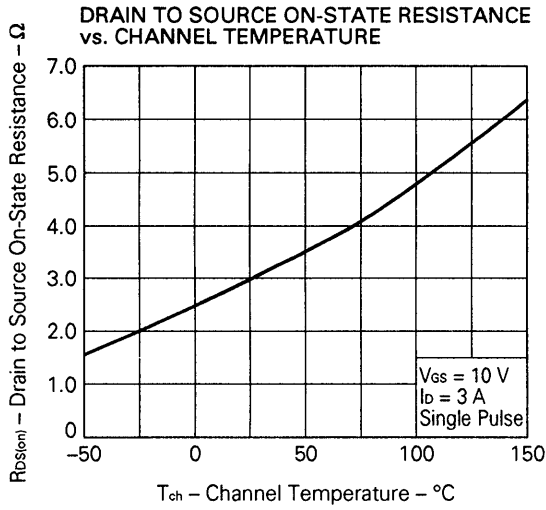
**Test Circuit 3: Gate Charge**



TYPICAL CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ )







**Reference**

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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