



## N-Channel Enhancement-Mode Vertical DMOS FETs

### Ordering Information

BV <sub>DSS</sub> / BV <sub>DGS</sub>	R <sub>DS(ON)</sub> (max)	I <sub>D(ON)</sub> (min)	Order Number / Package			
			TO-3	TO-39	TO-220	Dice†
350V	2.5Ω	3A	VN0335N1	VN0335N2	VN0335N5	VN0335ND
400V	2.5Ω	3A	VN0340N1	VN0340N2	VN0340N5	VN0340ND

† MIL visual screening available

### High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

### Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C<sub>ISS</sub> and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

### Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

### Absolute Maximum Ratings

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

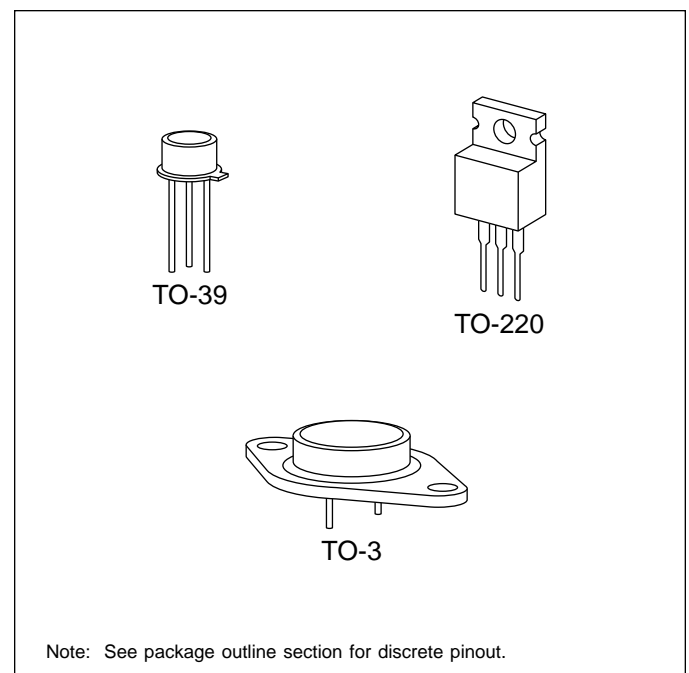
\* Distance of 1.6 mm from case for 10 seconds.

### Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Package Options



## Thermal Characteristics

Package	$I_D$ (continuous)*	$I_D$ (pulsed)	Power Dissipation @ $T_C = 25^\circ\text{C}$	$\theta_{ja}$ $^\circ\text{C/W}$	$\theta_{jc}$ $^\circ\text{C/W}$	$I_{DR}^*$	$I_{DRM}$
TO-3	3.5A	8.0A	100W	30	1.25	3.5A	8.0A
TO-39	1.0A	7.0A	6W	125	20.8	1.0A	7.0A
TO-220	2.1A	8.0A	50W	40	2.5	2.1A	8.0A

\*  $I_D$  (continuous) is limited by max rated  $T_j$ .

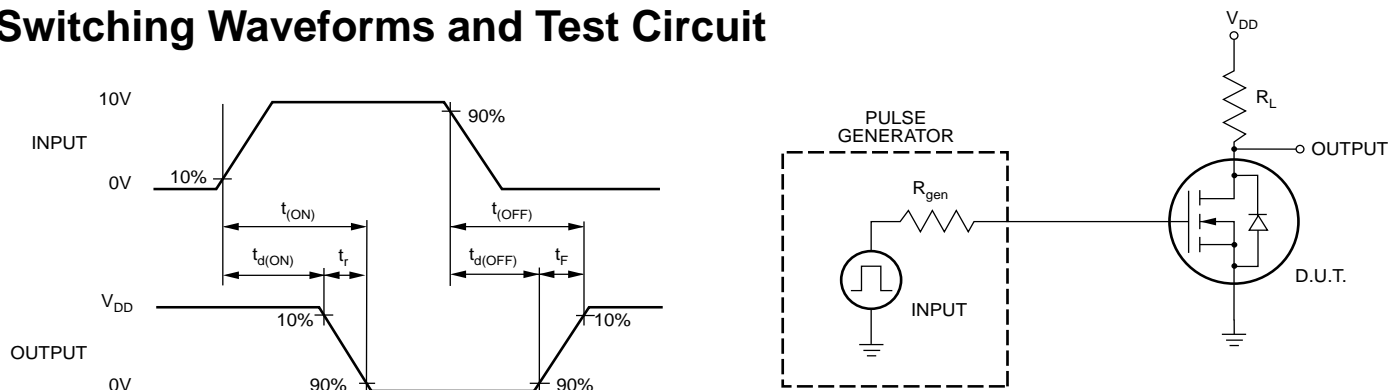
## Electrical Characteristics (@ $25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	VN0340	400			$V_{GS} = 0, I_D = 10\text{mA}$
		VN0335	350			
$V_{GS(th)}$	Gate Threshold Voltage	2		4	V	$V_{GS} = V_{DS}, I_D = 10\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-4.8	-6.0	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 10\text{mA}$
$I_{GSS}$	Gate Body Leakage			100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0$
$I_{DSS}$	Zero Gate Voltage Drain Current			100	$\mu\text{A}$	$V_{GS} = 0, V_{DS} = \text{Max Rating}$
				2.0	mA	$V_{GS} = 0, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current		5.0		A	$V_{GS} = 5\text{V}, V_{DS} = 25\text{V}$
		3.0	6.0	$V_{GS} = 10\text{V}, V_{DS} = 25\text{V}$		
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		2.2		$\Omega$	$V_{GS} = 5\text{V}, I_D = 0.5\text{A}$
			1.8	2.5		$V_{GS} = 10\text{V}, I_D = 1\text{A}$
$\Delta R_{DS(th)}$	Change in $R_{DS(th)}$ with Temperature		1	2	%/ $^\circ\text{C}$	$V_{GS} = 10\text{V}, I_D = 1\text{A}$
$G_{FS}$	Forward Transconductance	1	1.25		$\text{S}$	$V_{DS} = 25\text{V}, I_D = 1\text{A}$
$C_{ISS}$	Input Capacitance		550	650	pF	$V_{GS} = 0, V_{DS} = 25\text{V}$ $f = 1 \text{ MHz}$
$C_{OSS}$	Common Source Output Capacitance		75	125		
$C_{RSS}$	Reverse Transfer Capacitance		25	50		
$t_{d(ON)}$	Turn-ON Delay Time		12	20	ns	$V_{DD} = 25\text{V},$ $I_D = 1\text{A},$ $R_{GEN} = 10\Omega$
$t_r$	Rise Time		12	20		
$t_{d(OFF)}$	Turn-OFF Delay Time		65	100		
$t_f$	Fall Time		20	30		
$V_{SD}$	Diode Forward Voltage Drop		1.1	1.5		
$t_{rr}$	Reverse Recovery Time		450		ns	$V_{GS} = 0, I_{SD} = 1\text{A}$

### Notes:

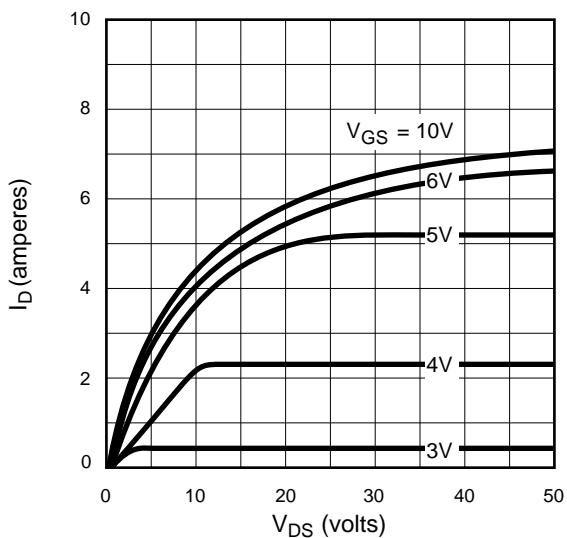
- All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test:  $300\mu\text{s}$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit

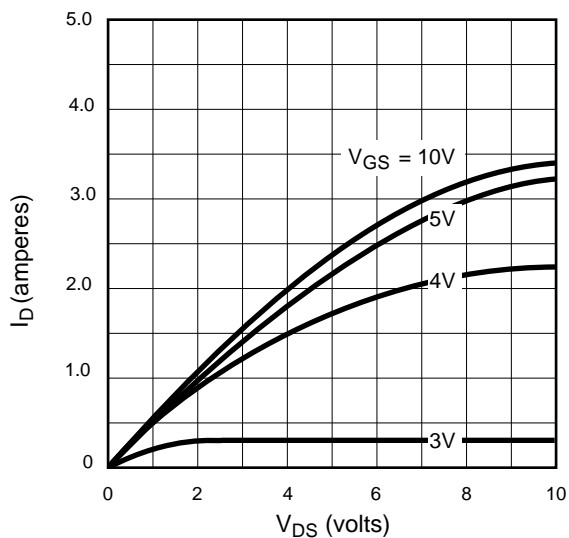


# Typical Performance Curves

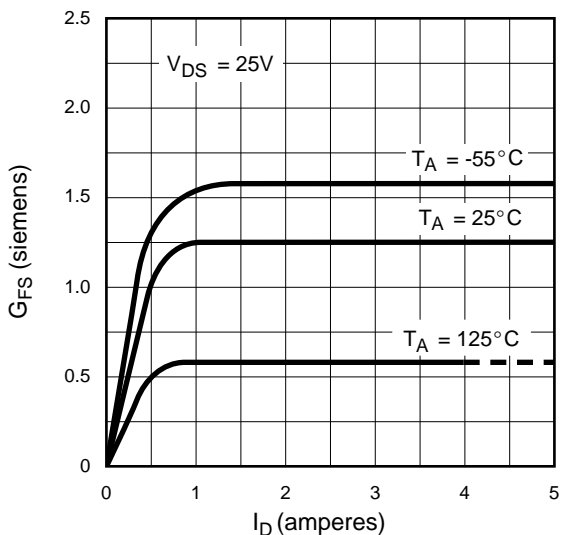
Output Characteristics



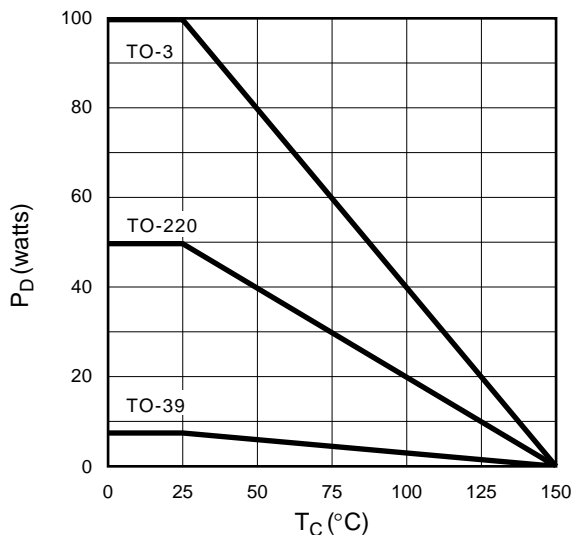
Saturation Characteristics



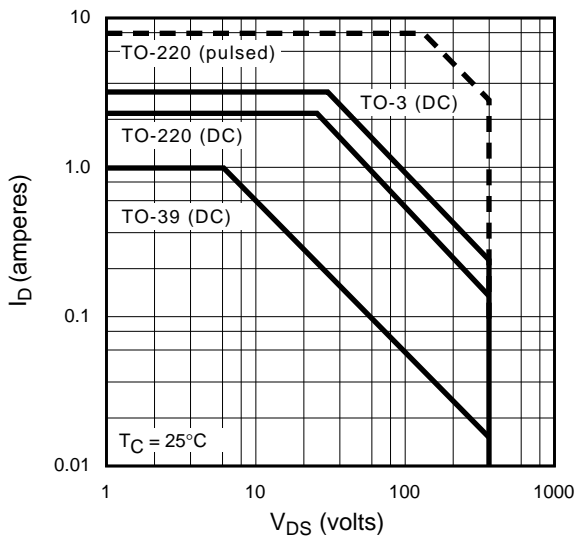
Transconductance vs. Drain Current



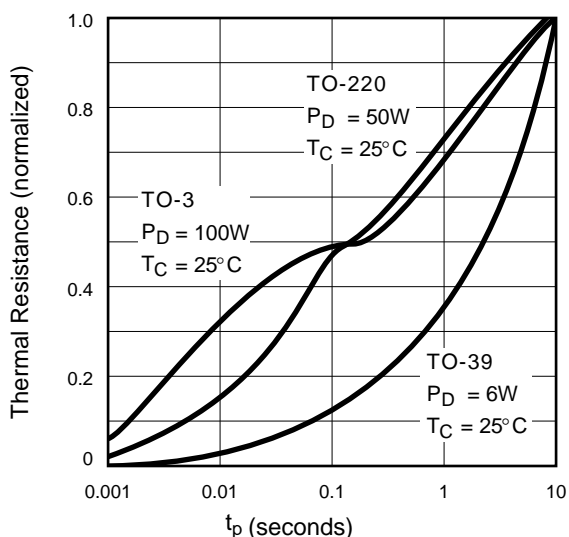
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

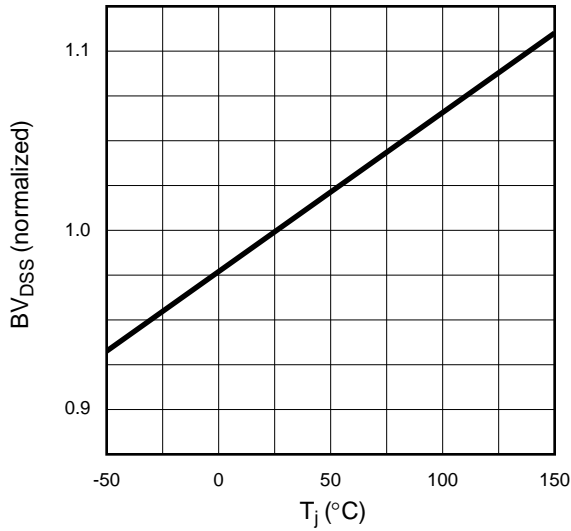


Thermal Response Characteristics

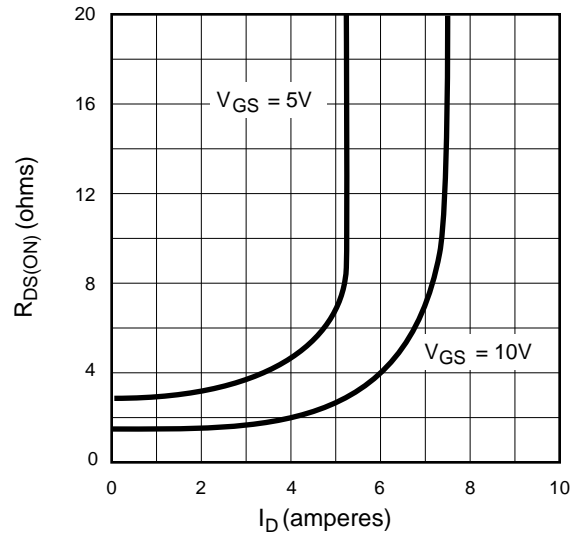


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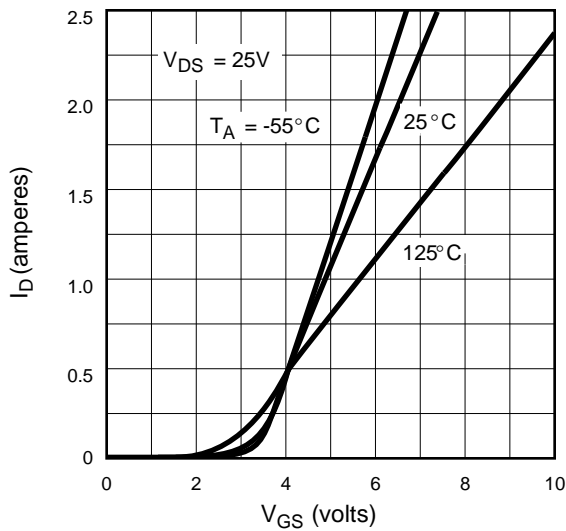
BV<sub>DSS</sub> Variation with Temperature



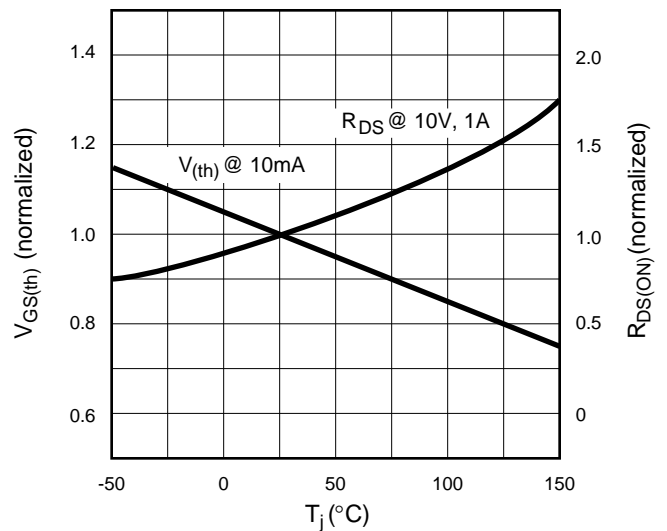
On-Resistance vs. Drain Current



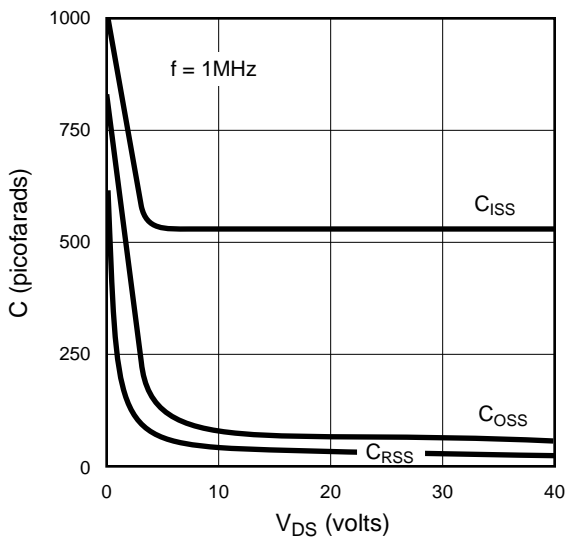
Transfer Characteristics



V<sub>(th)</sub> and R<sub>DS</sub> Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

