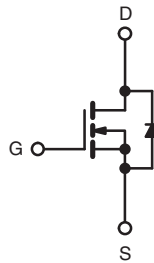
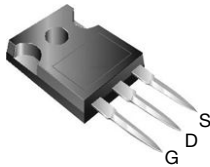


## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	600
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$   0.21
$Q_g$ (Max.) (nC)	180
$Q_{gs}$ (nC)	61
$Q_{gd}$ (nC)	85
Configuration	Single

TO-247AC



N-Channel MOSFET

### FEATURES

- Superfast Body Diode Eliminates the Need for External Diodes in ZVS Applications
- Lower Gate Charge Results in Simpler Drive Requirements
- Enhanced  $dV/dt$  Capabilities Offer Improved Ruggedness
- Higher Gate Voltage Threshold Offers Improved Noise Immunity
- Compliant to RoHS Directive 2002/95/EC



RoHS\*  
COMPLIANT

### APPLICATIONS

- Zero Voltage Switching (SMPS)
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control Applications

ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	IRFP26N60LPbF
	SiHFP26N60L-E3
SnPb	IRFP26N60L
	SiHFP26N60L


ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	600	V	
Gate-Source Voltage	$V_{GS}$	$\pm 30$		
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A	
		$T_C = 100\text{ }^\circ\text{C}$		
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	100		
Linear Derating Factor		3.8	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	570	mJ	
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	26	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	47	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	470	W
Peak Diode Recovery $dV/dt$ <sup>c</sup>		$dV/dt$	21	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$		- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw		10	lbf · in
			1.1	N · m

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1.7\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 26\text{ A}$ ,  $dV/dt = 21\text{ V/ns}$  (see fig. 12).
- $I_{SD} \leq 26\text{ A}$ ,  $dI/dt \leq 480\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.24	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.27	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$	-	0.33	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	-	5.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	50	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	2.0	mA
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 16\text{ A}^b$	-	0.21	0.25	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 16\text{ A}$	13	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}, \text{ see fig. 5}$	-	5020	-	pF
Output Capacitance	$C_{oss}$		-	450	-	
Reverse Transfer Capacitance	$C_{rss}$		-	34	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$		-	230	-	
Effective Output Capacitance (Energy Related)	$C_{oss\text{ eff. (ER)}}$		$V_{GS} = 0\text{ V}$	-	170	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 26\text{ A}, V_{DS} = 480\text{ V}, \text{ see fig. 7 and 15}^b$	-	-	180	nC
Gate-Source Charge	$Q_{gs}$		-	-	61	
Gate-Drain Charge	$Q_{gd}$		-	-	85	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 26\text{ A}, R_g = 4.3\text{ }\Omega, V_{GS} = 10\text{ V}, \text{ see fig. 11a and 11b}^b$	-	31	-	ns
Rise Time	$t_r$		-	110	-	
Turn-Off Delay Time	$t_{d(off)}$		-	47	-	
Fall Time	$t_f$		-	42	-	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	26	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	100	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 26\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 26\text{ A}$	-	170	250	ns
		$T_J = 125\text{ }^\circ\text{C}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	210	320	
Body Diode Reverse Recovery Charge	$Q_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 26\text{ A}, V_{GS} = 0\text{ V}^b$	-	670	1000	nC
		$T_J = 125\text{ }^\circ\text{C}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	1050	1570	
Reverse Recovery Current	$I_{RRM}$	$T_J = 25\text{ }^\circ\text{C}$	-	7.3	11	A
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .  
 $C_{oss\text{ eff. (ER)}}$  is a fixed capacitance that stores the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

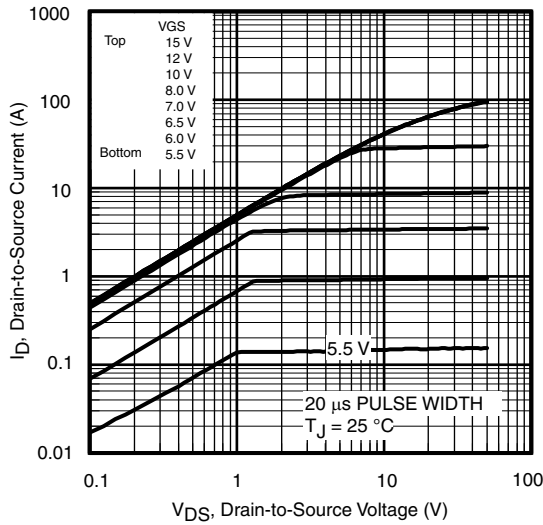


Fig. 1 - Typical Output Characteristics

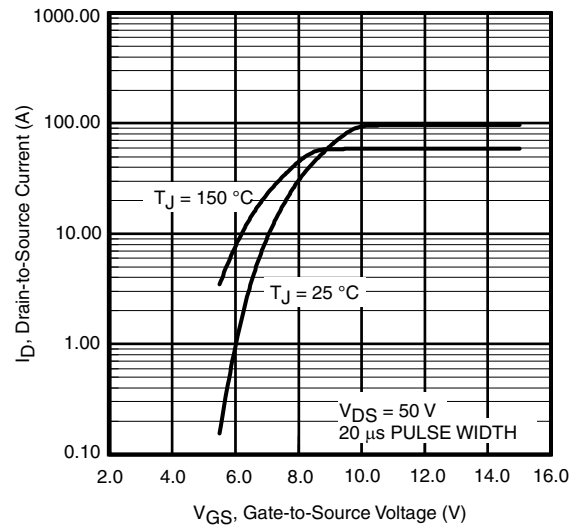


Fig. 3 - Typical Transfer Characteristics

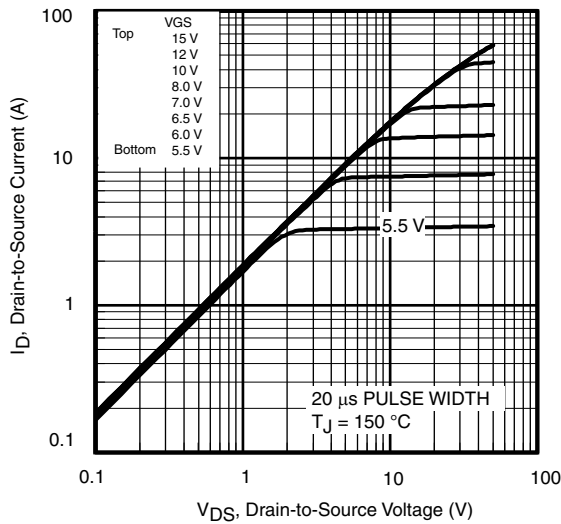


Fig. 2 - Typical Output Characteristics

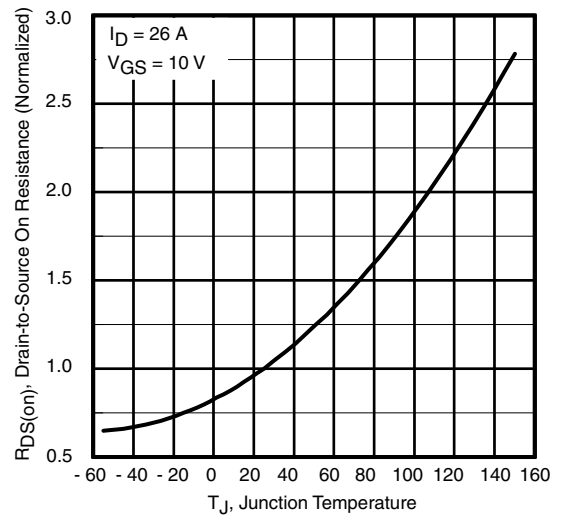
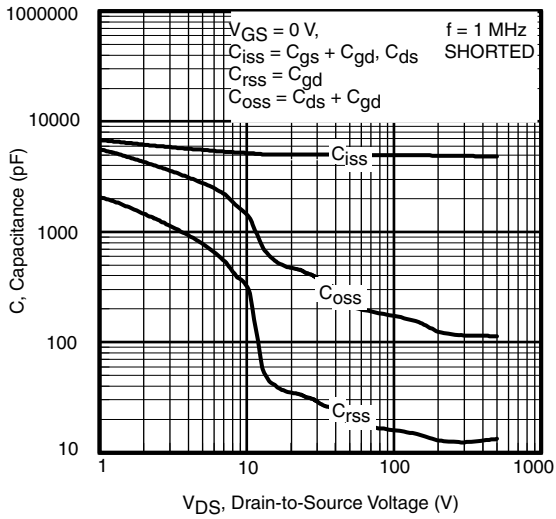
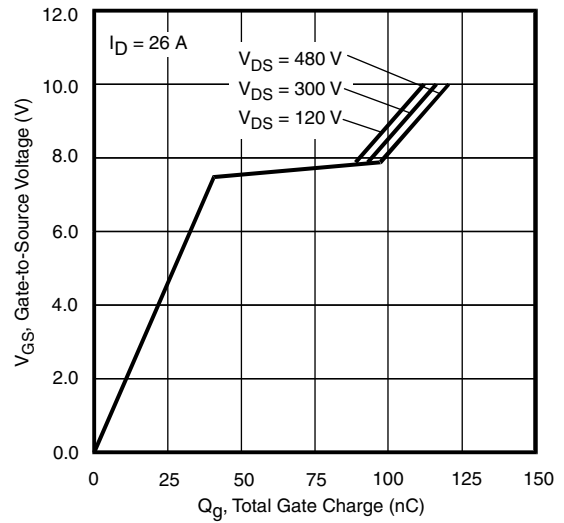


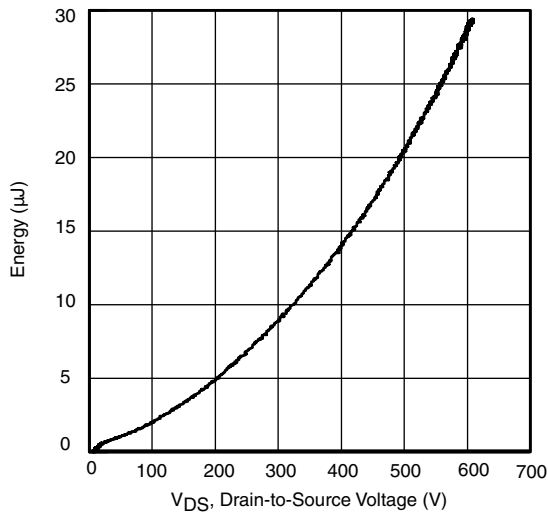
Fig. 4 - Normalized On-Resistance vs. Temperature



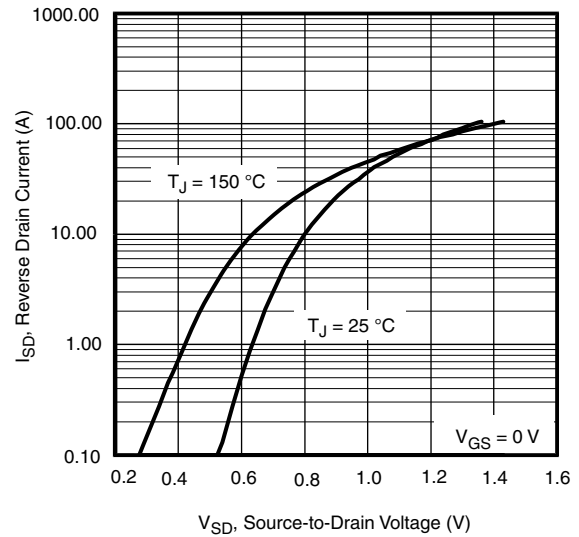
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



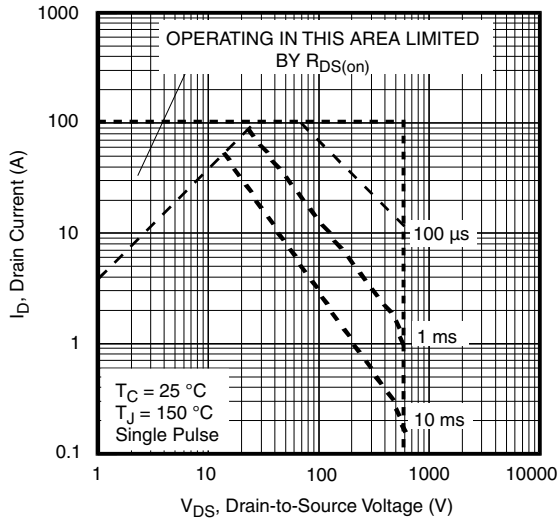
**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**



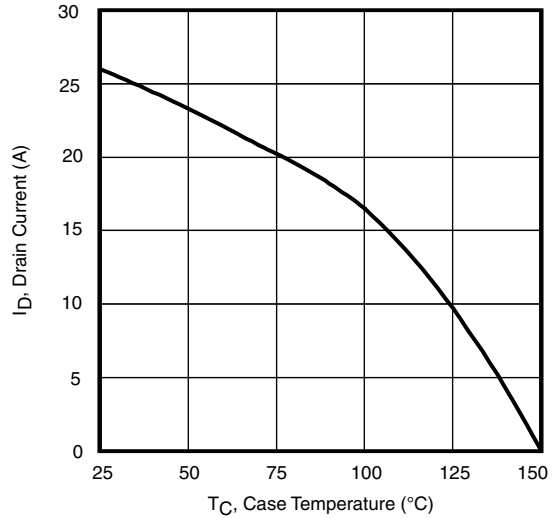
**Fig. 6 - Typical Output Capacitance Stored Energy vs.  $V_{DS}$**



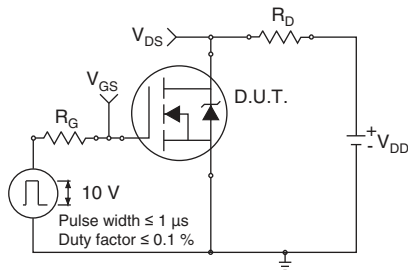
**Fig. 8 - Typical Source-Drain Diode Forward Voltage**



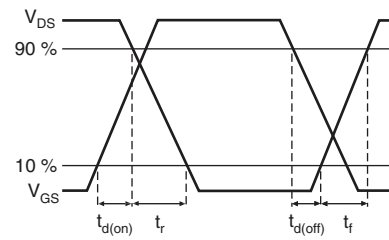
**Fig. 9a - Maximum Safe Operating Area**



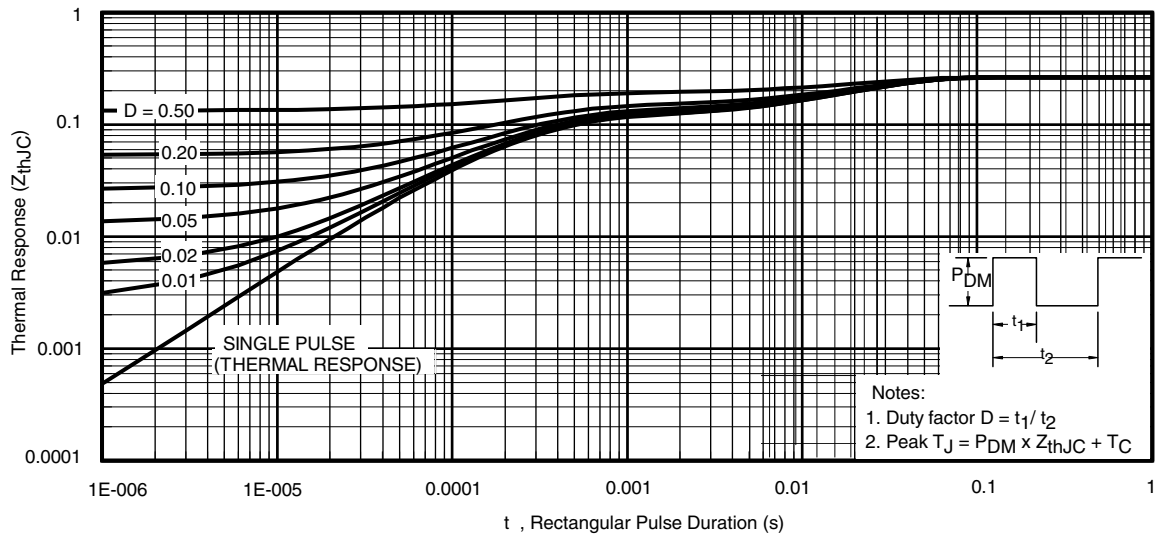
**Fig. 10 - Maximum Drain Current vs. Case Temperature**



**Fig. 11a - Switching Time Test Circuit**



**Fig. 11b - Switching Time Waveforms**



**Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

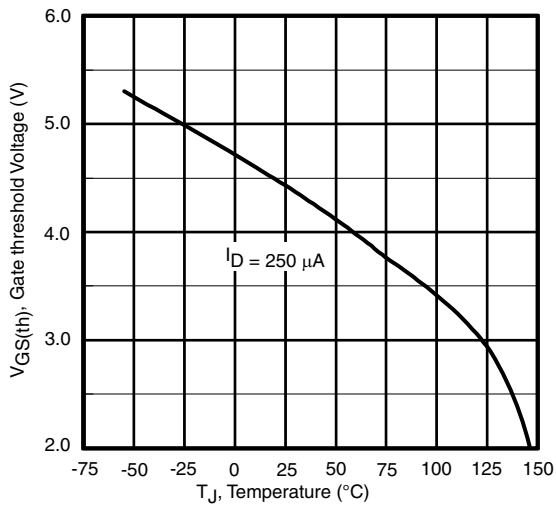


Fig. 13 - Threshold Voltage vs. Temperature

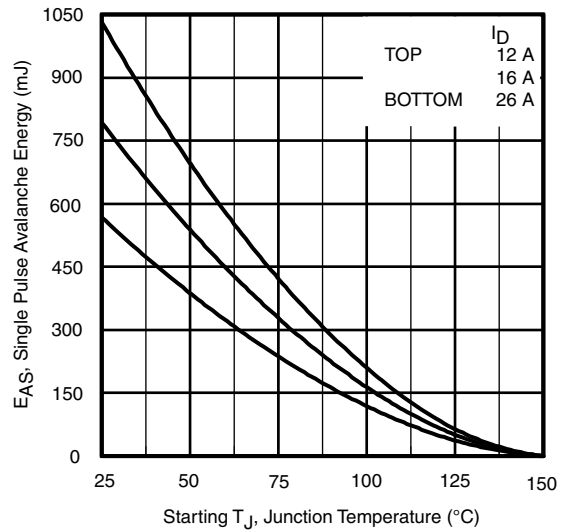


Fig. 14c - Maximum Avalanche Energy vs. Drain Current

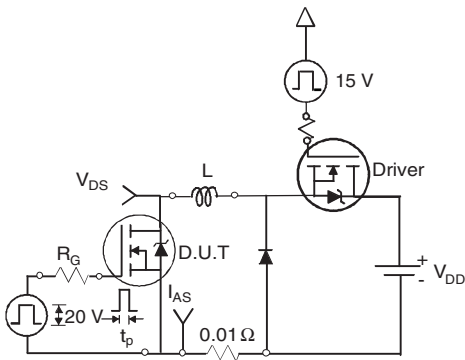


Fig. 14a - Unclamped Inductive Test Circuit

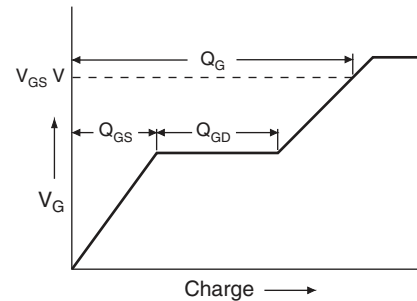


Fig. 15a - Basic Gate Charge Waveform

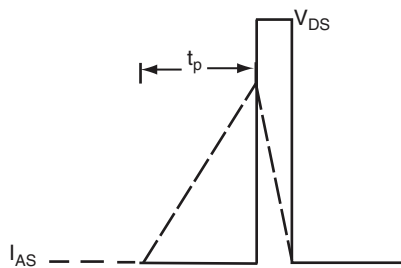


Fig. 14b - Unclamped Inductive Waveforms

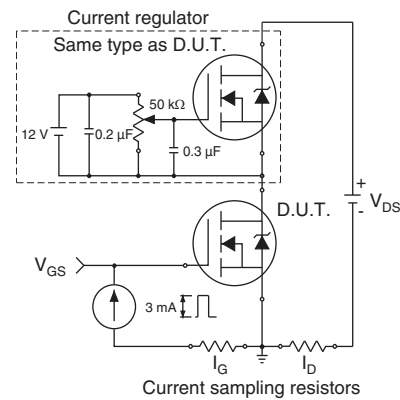
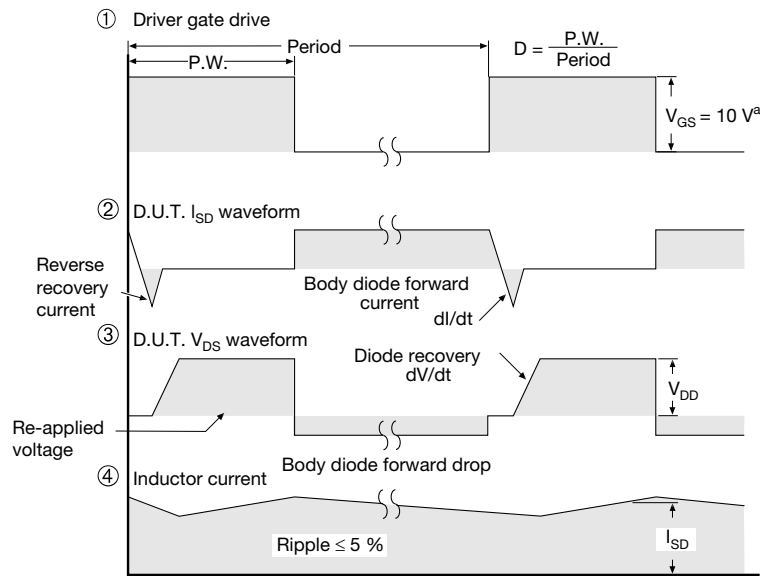
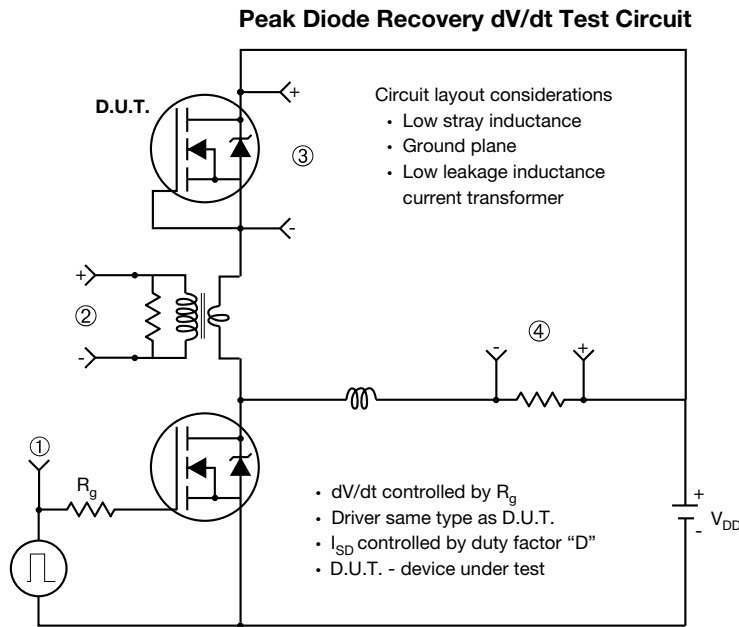


Fig. 15b - Gate Charge Test Circuit



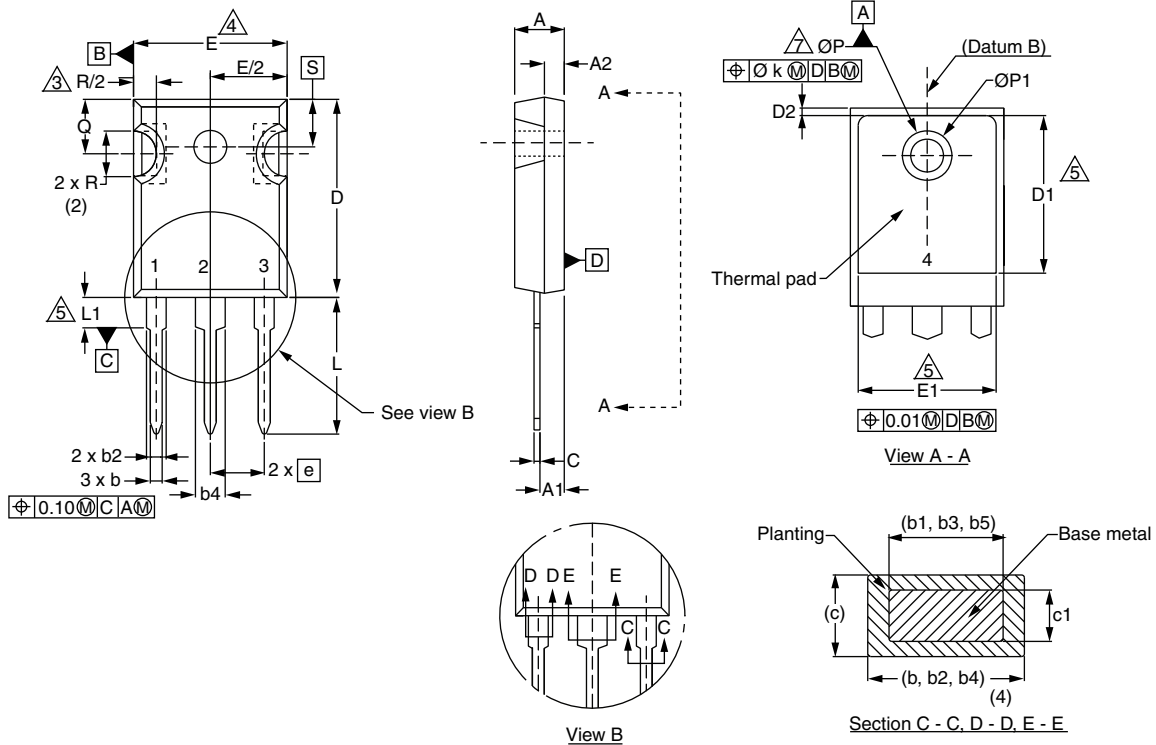
**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 16 - For N-Channel**

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### TO-247AC (High Voltage)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
$\phi k$	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
$\phi P$	3.51	3.66	0.138	0.144
$\phi P1$	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

ECN: X12-0167-Rev. B, 24-Sep-12  
DWG: 5971

#### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Contour of slot optional.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions D1 and E1.
5. Lead finish uncontrolled in L1.
6.  $\phi P$  to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
7. Outline conforms to JEDEC outline TO-247 with exception of dimension c.
8. Xian and Mingxin actually photo.







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**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**