Power MOSFET

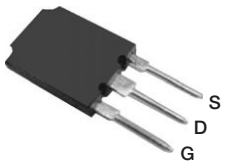
PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	560	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.270
Q_g (Max.) (nC)	76	
Q_{gs} (nC)	21	
Q_{gd} (nC)	34	
Configuration	Single	

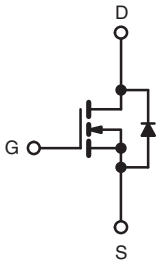
FEATURES

- Low Figure-of-Merit R_{on} x Q_g
- 100 % Avalanche Tested
- High Peak Current Capability
- dV/dt Ruggedness
- Improved t_{rr}/Q_{rr}
- Improved Gate Charge
- High Power Dissipations Capability
- Compliant to RoHS Directive 2002/95/EC

RoHS COMPLIANT

Super-247





N-Channel MOSFET

ORDERING INFORMATION	
Package	Super-247
Lead (Pb)-free	SiHS20N50C-E3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	500	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current (T_J = 150 °C)[e]	V_{GS} at 10 V	T_C = 25 °C	I_D	20	A
		T_C = 100 °C		11	
Pulsed Drain Current[a]			I_{DM}	80	
Linear Derating Factor				1.8	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	361	mJ
Maximum Power Dissipation			P_D	250	W
Peak Diode Recovery dV/dt[c]			dV/dt	5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature.
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 2.5 mH, R_g = 25 Ω, I_{AS} = 17 A.
c. I_{SD} ≤ 18 A, dI/dt ≤ 380 A/µs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
d. 1.6 mm from case.
e. Limited by maximum junction temperature.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.5	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	700	-	mV/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V		-	-	25	µA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 10 A	-	0.225	0.270	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 10 A		-	6.4	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz		-	2451	2942	pF
Output Capacitance	C_{oss}			-	300	360	
Reverse Transfer Capacitance	C_{rss}			-	26	32	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 18 A, V_{DS} = 400 V	-	65	76	nC
Gate-Source Charge	Q_{gs}			-	21	-	
Gate-Drain Charge	Q_{gd}			-	29	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 250 V, I_D = 18 A, R_g = 9.1 Ω		-	80	-	ns
Rise Time	t_r			-	27	-	
Turn-Off Delay Time	$t_{d(off)}$			-	32	-	
Fall Time	t_f			-	44	-	
Gate Input Resistance	R_g	f = 1 MHz, open drain		-	1.1	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	20	A
Pulsed Diode Forward Current	I_{SM}			-	-	80	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 18 A, V_{GS} = 0 V		-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = I_S, dI/dt = 100 A/µs, V = 35 V		-	503	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	6.7	-	µC
Reverse Recovery Current	I_{RRM}			-	30	-	A

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

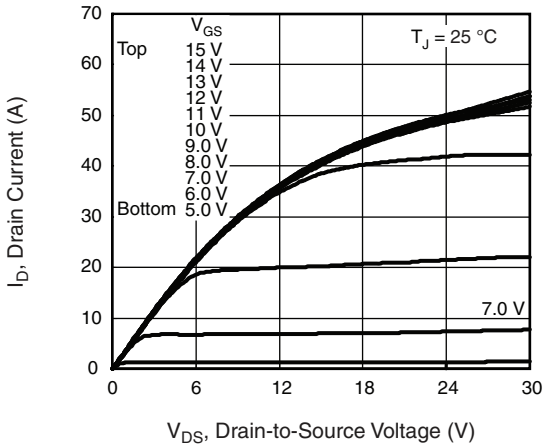


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

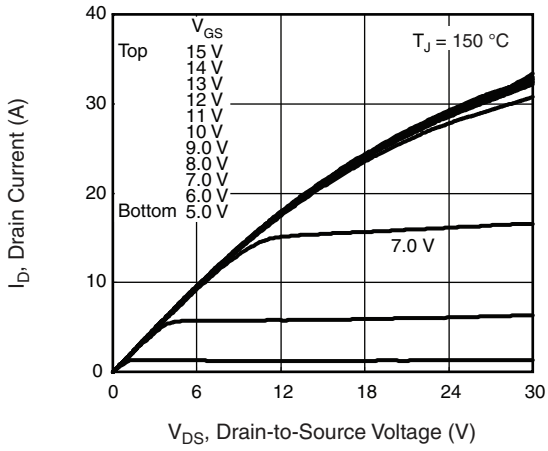


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

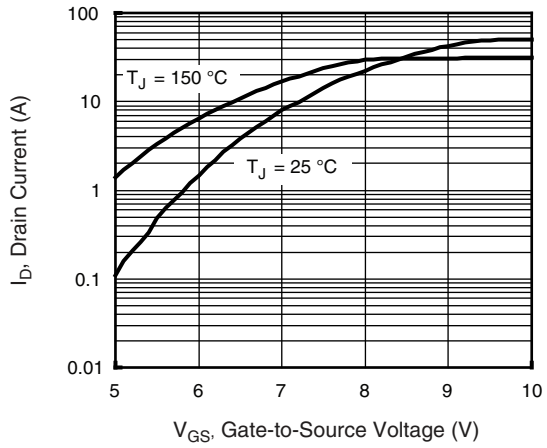


Fig. 3 - Typical Transfer Characteristics

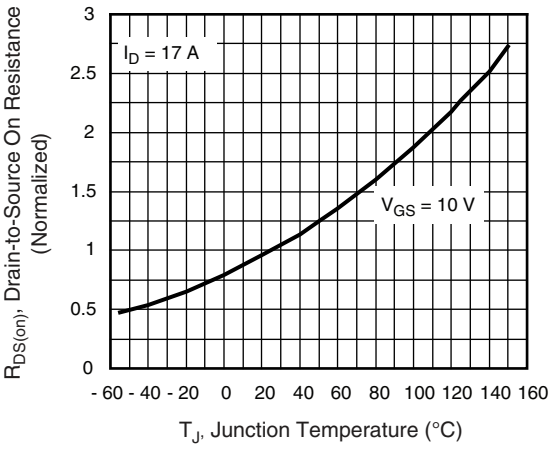


Fig. 4 - Normalized On-Resistance vs. Temperature

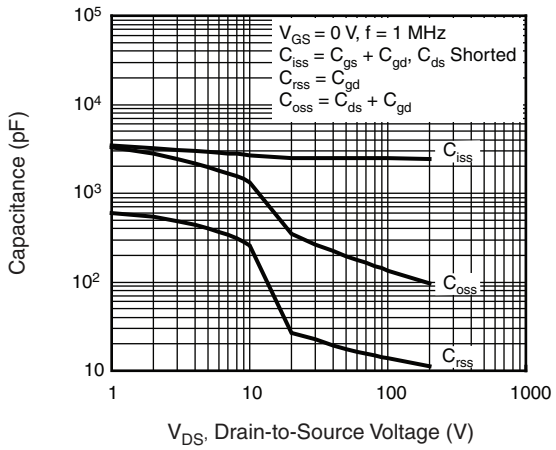


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

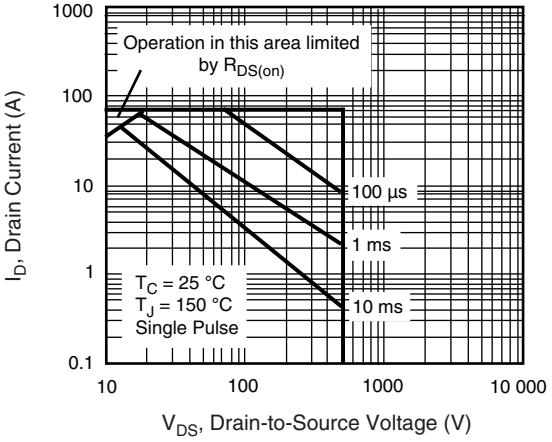


Fig. 8 - Maximum Safe Operating Area

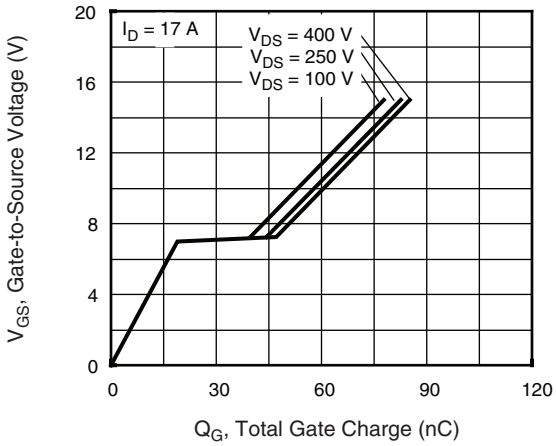


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

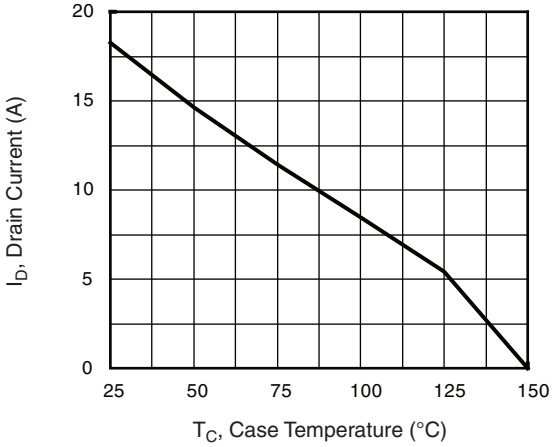


Fig. 9 - Maximum Drain Current vs. Case Temperature

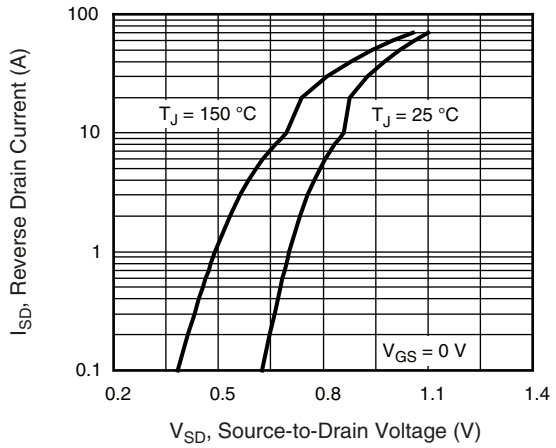


Fig. 7 - Typical Source-Drain Diode Forward Voltage

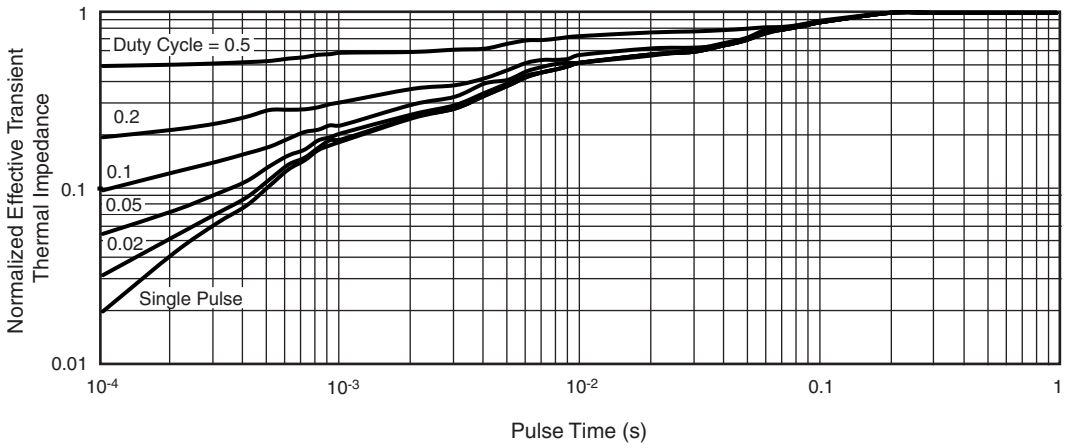


Fig. 10 - Normalized Thermal Transient Impedance, Junction-to-Case (Super-247)

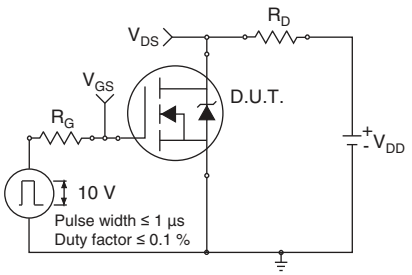


Fig. 11a - Switching Time Test Circuit

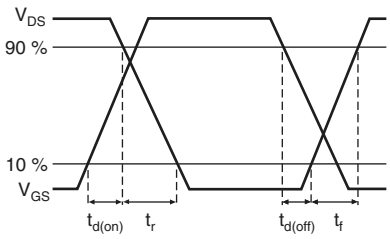


Fig. 11b - Switching Time Waveforms

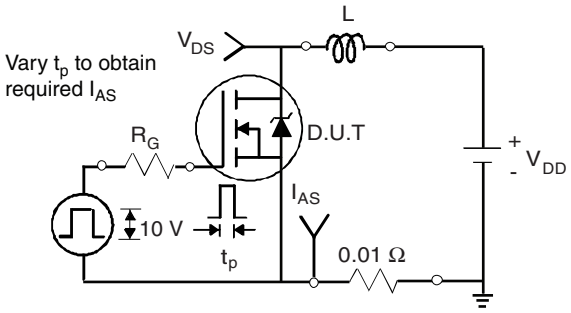


Fig. 12a - Unclamped Inductive Test Circuit

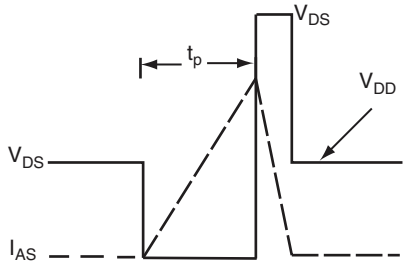


Fig. 12b - Unclamped Inductive Waveforms

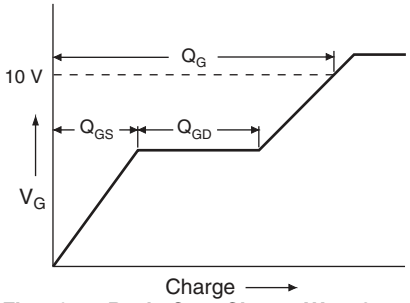


Fig. 13a - Basic Gate Charge Waveform

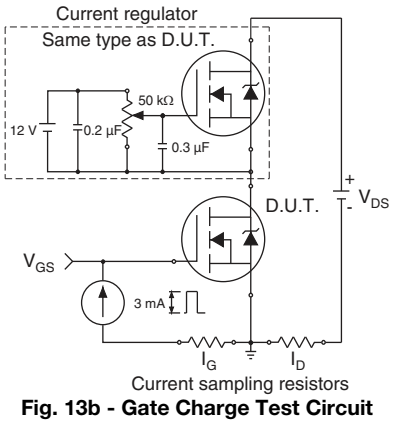
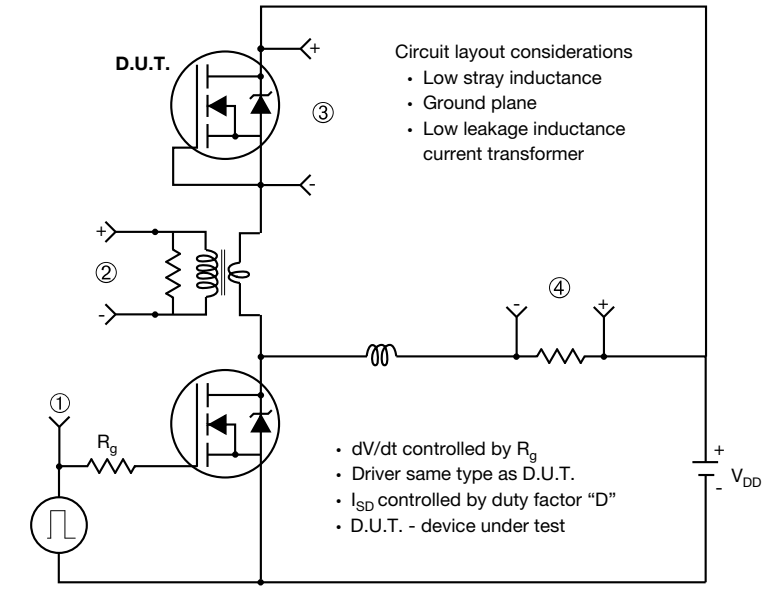
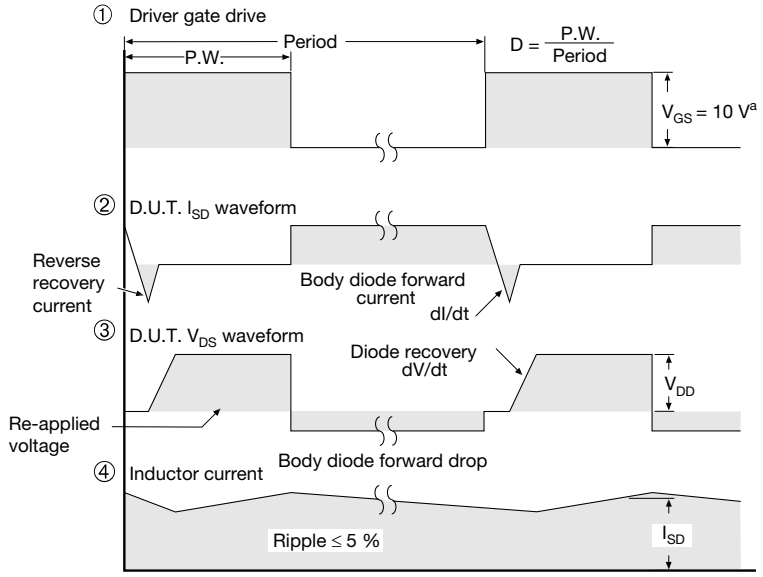


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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