

TSSOP-8

Pin Definition:

- | | |
|-------------|-------------|
| 1. Drain 1 | 8. Drain 2 |
| 2. Source 1 | 7. Source 2 |
| 3. Source 1 | 6. Source 2 |
| 4. Gate 1 | 5. Gate 2 |

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (m Ω)	I_D (A)
-20	40 @ $V_{GS} = -4.5V$	-5
	50 @ $V_{GS} = -2.5V$	-4
	60 @ $V_{GS} = -1.8V$	-3

Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

- Load Switch
- PA Switch

Ordering Information

Part No.	Package	Packing
TSM6981DCA RV	TSSOP-8	3Kpcs / 13" Reel
TSM6981DCA RVG	TSSOP-8	3Kpcs / 13" Reel

Note: "G" denote for Halogen Free Product

Absolute Maximum Rating ($T_a = 25^\circ C$ unless otherwise noted)

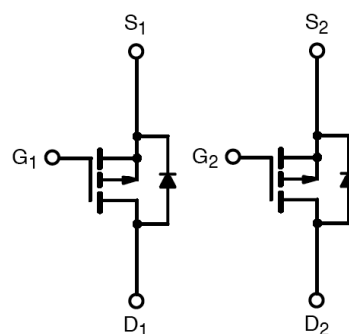
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current, $V_{GS} @ 4.5V$.	I_D	-5	A
Pulsed Drain Current, $V_{GS} @ 4.5V$	I_{DM}	-30	A
Continuous Source Current (Diode Conduction) ^{a,b}	I_S	-1.0	A
Maximum Power Dissipation	P_D	$T_a = 25^\circ C$	1.14
		$T_a = 70^\circ C$	0.73
Operating Junction Temperature	T_J	+150	$^\circ C$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ C$

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Foot (Drain) Thermal Resistance	$R\theta_{JF}$	40	$^\circ C/W$
Junction to Ambient Thermal Resistance (PCB mounted)	$R\theta_{JA}$	75	$^\circ C/W$

Notes:

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

Block Diagram


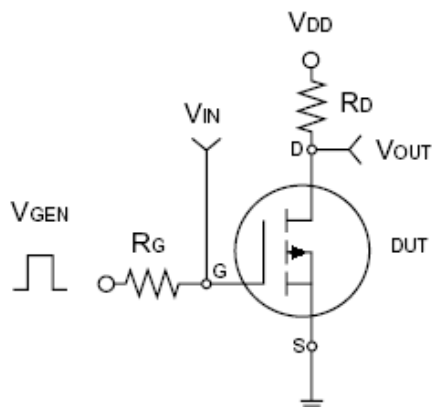
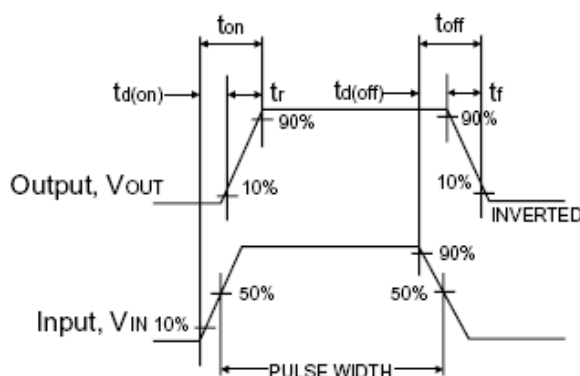
Dual P-Channel MOSFET

Electrical Specifications (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	BV_{DSS}	-20	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	$V_{GS(TH)}$	-0.4	--	-1.0	V
Zero Gate Voltage Drain Current	$V_{DS} = -16V, V_{GS} = 0V$	I_{DSS}	--	--	-1.0	μA
Gate Body Leakage	$V_{GS} = \pm 8V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
On-State Drain Current	$V_{DS} \leq -5V, V_{GS} = -4.5V$	$I_{D(ON)}$	-20	--	--	A
Drain-Source On-State Resistance	$V_{GS} = -4.5V, I_D = -5A$	$R_{DS(ON)}$	--	30	40	m Ω
	$V_{GS} = -2.5V, I_D = -4A$		--	40	50	
	$V_{GS} = -1.8V, I_D = -3A$		--	50	60	
Forward Transconductance	$V_{DS} = -5V, I_D = -5A$	g_{fs}	--	17	--	S
Diode Forward Voltage	$I_S = -1.0A, V_{GS} = 0V$	V_{SD}	--	-0.6	-1.2	V
Dynamic^b						
Total Gate Charge	$V_{DS} = -10V, I_D = -4.7A, V_{GS} = -4.5V$	Q_g	--	12.5	19	nC
Gate-Source Charge		Q_{gs}	--	1.7	--	
Gate-Drain Charge		Q_{gd}	--	3.3	--	
Input Capacitance	$V_{DS} = -10V, V_{GS} = 0V, f = 1.0MHz$	C_{iss}	--	1020	--	pF
Output Capacitance		C_{oss}	--	191	--	
Reverse Transfer Capacitance		C_{rss}	--	140	--	
Switching^c						
Turn-On Delay Time	$V_{DD} = -10V, R_L = 10\Omega, I_D = -1A, V_{GEN} = -4.5V, R_G = 6\Omega$	$t_{d(on)}$	--	25	40	nS
Turn-On Rise Time		t_r	--	43	65	
Turn-Off Delay Time		$t_{d(off)}$	--	71	110	
Turn-Off Fall Time		t_f	--	48	75	

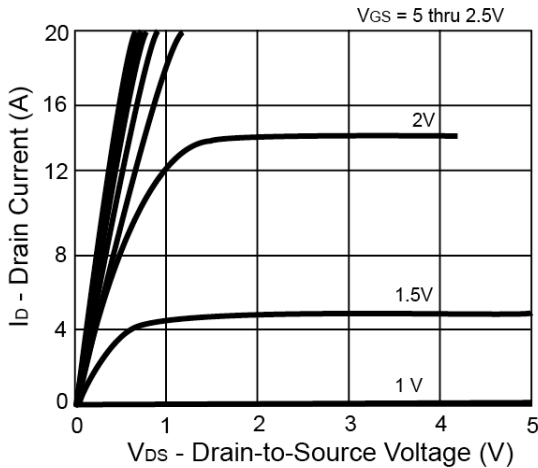
Notes:

- a. pulse test: PW $\leq 300\mu S$, duty cycle $\leq 2\%$
- b. For DESIGN AID ONLY, not subject to production testing.
- b. Switching time is essentially independent of operating temperature.

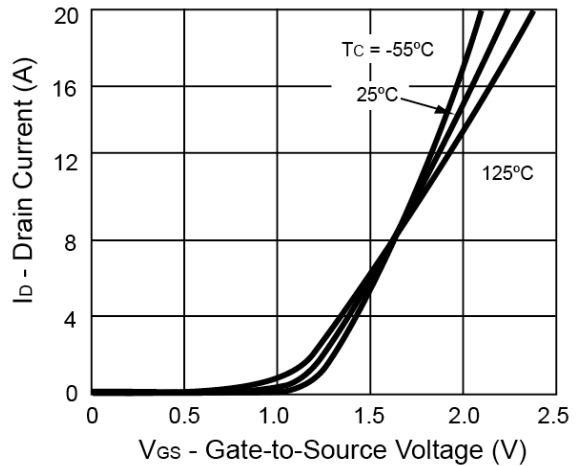

Switching Test Circuit

Switchin Waveforms

Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

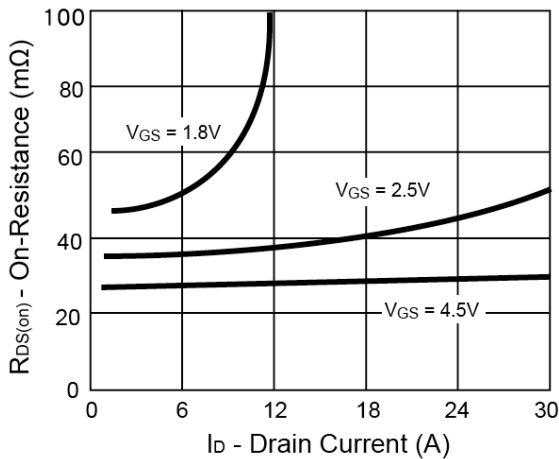
Output Characteristics



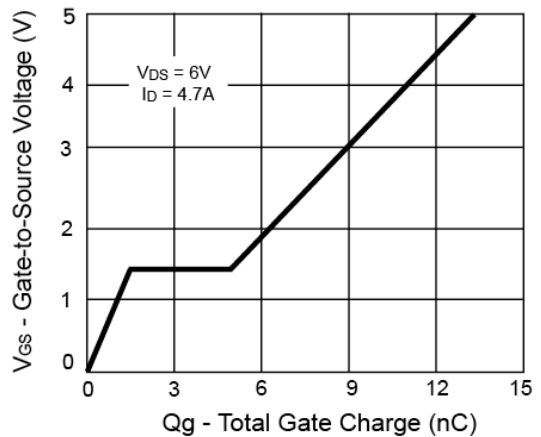
Transfer Characteristics



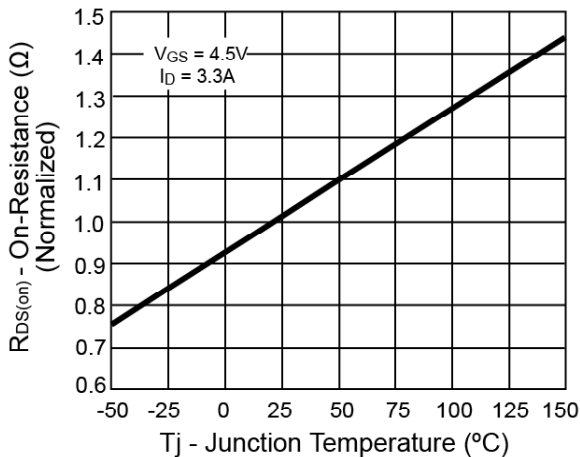
On-Resistance vs. Drain Current



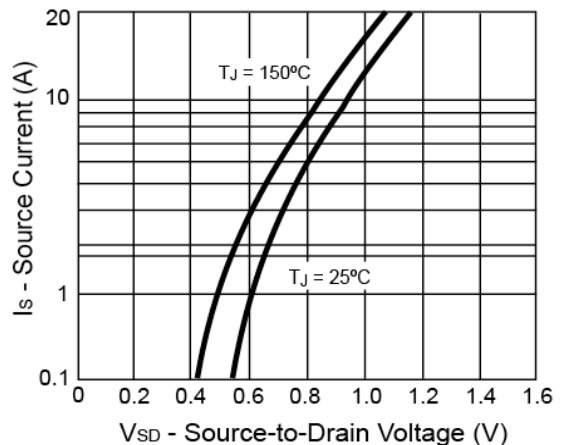
Gate Charge



On-Resistance vs. Junction Temperature

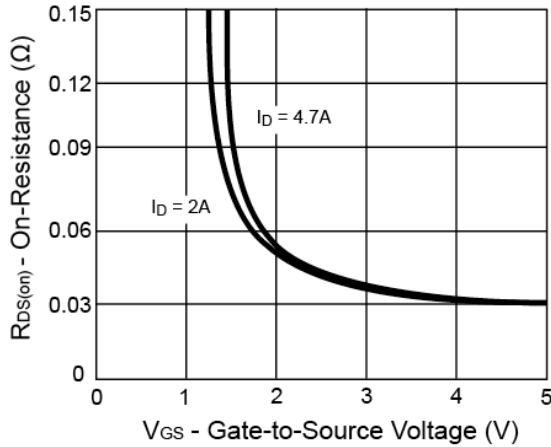


Source-Drain Diode Forward Voltage

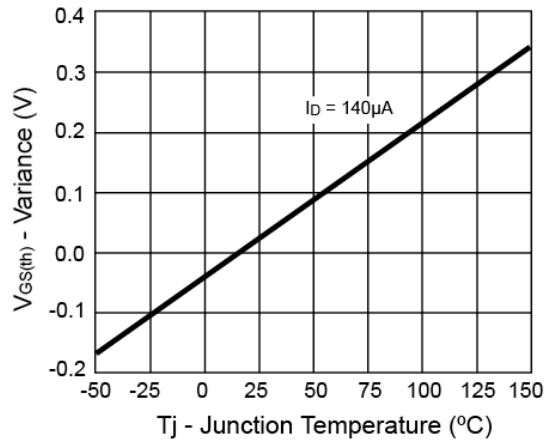


Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

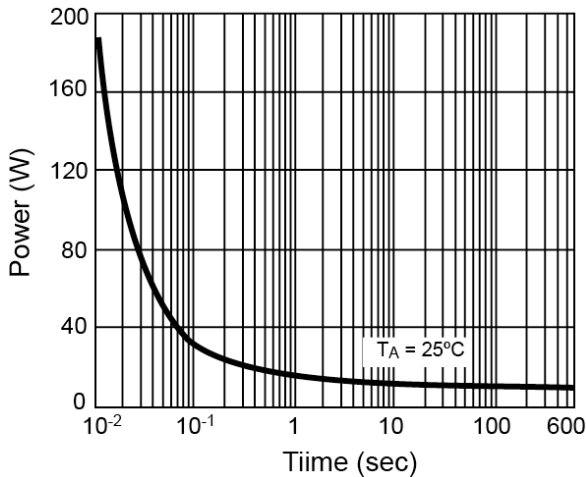
On-Resistance vs. Gate-Source Voltage



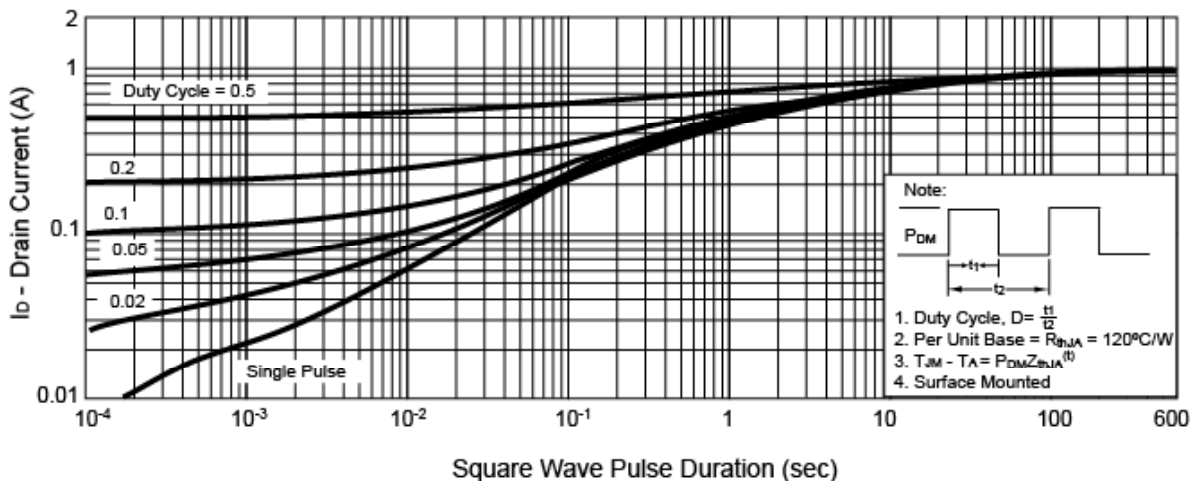
Threshold Voltage



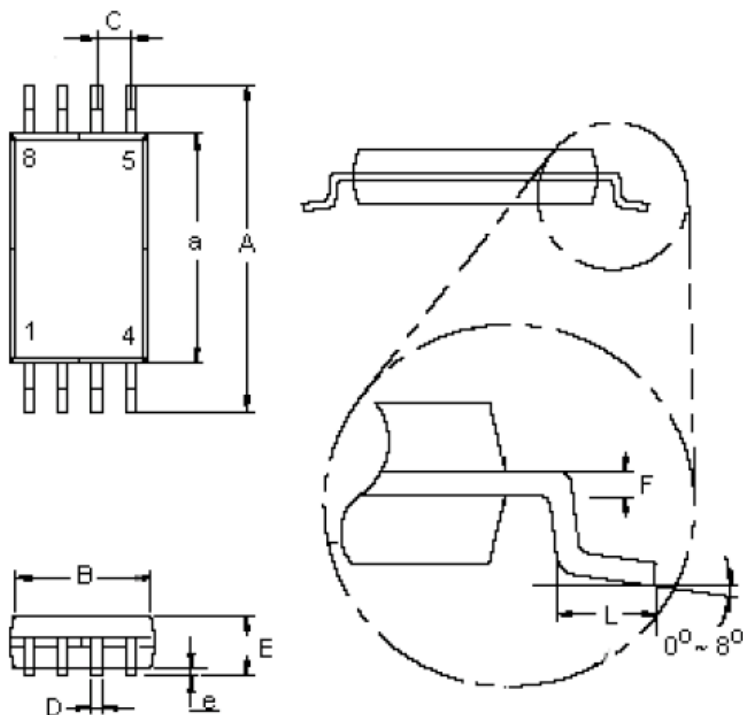
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

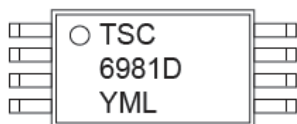


TSSOP-8 Mechanical Drawing



TSSOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.20	6.60	0.244	0.260
a	4.30	4.50	0.170	0.177
B	2.90	3.10	0.114	0.122
C	0.65 (typ)		0.025 (typ)	
D	0.25	0.30	0.010	0.019
E	1.05	1.20	0.041	0.049
e	0.05	0.15	0.002	0.009
F	0.127		0.005	
L	0.50	0.70	0.020	0.028

Marking Diagram



- Y** = Year Code
- M** = Month Code
(A=Jan, B=Feb, C=Mar, D=Apl, E=May, F=Jun, G=Jul, H=Aug, I=Sep, J=Oct, K=Nov, L=Dec)
= Month Code for Halogen Free Product
(O=Jan, P=Feb, Q=Mar, R=Apl, S=May, T=Jun, U=Jul, V=Aug, W=Sep, X=Oct, Y=Nov, Z=Dec)
- L** = Lot Code



TSM6981D

20V Dual P-Channel MOSFET

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