



TO-92



SOT-223



Pin Definition:

1. Gate
2. Drain
3. Source

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
450	4.25 @ $V_{GS}=10V$	0.25

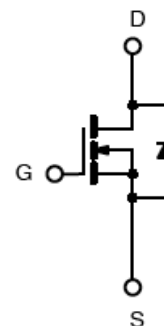
General Description

The TSM1N45 is N-Channel enhancement mode power field effect transistors are produced using planar DMOS technology process. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand higher energy pulse in the avalanche and commutation mode. There devices are well suited for electronic ballasts base and half bridge configuration.

Features

- Low gate charge @ typical 6.5nC
- Low Crss @ typical 6.5pF
- Avalanche energy specified
- Improved dv/dt capability
- Gate-Source Voltage $\pm 30V$ guaranteed

Block Diagram



N-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM1N45CT B0	TO-92	1Kpcs / Bulk
TSM1N45CT A3	TO-92	2Kpcs / Ammo
TSM1N45CW RP	SOT-223	2.5Kpcs / 13" Reel

Absolute Maximum Rating ($T_a=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	450	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current	I_D	0.5	A
Pulsed Drain Current (Note 1)	I_{DM}	4	A
Single Pulse Drain to Source Avalanche Energy (Note 2)	E_{AS}	108	mJ
Avalanche Current (Note 1)	I_{AR}	0.5	A
Repetitive Avalanche Energy (Note 1)	E_{AR}	0.25	mJ
Peak Diode Recovery dv/dt (Note 3)	dv/dt	5.5	V/ns
Total Power Dissipation @ $T_c = 25^\circ C$	TO-92	2	W
	SOT-223	15	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$

*Surface Mounted on 1"x1" FR4 board

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Lead	$R_{\theta_{JL}}$	50	$^\circ C/W$
Thermal Resistance - Junction to Case	$R_{\theta_{JC}}$	8.5	
Thermal Resistance - Junction to Ambient *	TO-92	140	$^\circ C/W$
	SOT-223	60	

*When mounted on the minimum pad size recommended (PCB mount)

Electrical Specifications (Ta=25°C, unless otherwise noted)

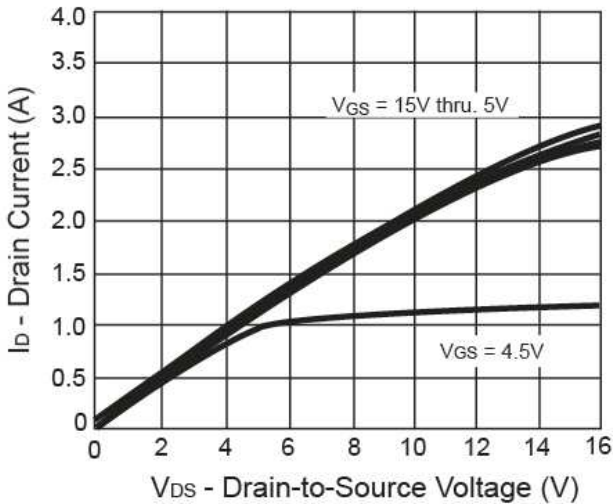
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	450	--	--	V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 0.25A$	$R_{DS(ON)}$	--	3.7	4.25	Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	2.3	3.0	3.7	V
	$V_{DS} = V_{GS}, I_D = 250mA$		3.2	4.0	4.8	
Zero Gate Voltage Drain Current	$V_{DS} = 450V, V_{GS} = 0V$	I_{DSS}	--	--	10	μA
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Forward Transconductance	$V_{DS} = 50V, I_D = 0.25A$	g_{fs}	--	0.7	--	S
Dynamic						
Total Gate Charge	$V_{DS} = 360V, I_D = 0.5A,$ $V_{GS} = 10V$ (Note 4,5)	Q_g	--	6.5	10	nC
Gate-Source Charge		Q_{gs}	--	1.3	--	
Gate-Drain Charge		Q_{gd}	--	3.2	--	
Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0MHz$	C_{iss}	--	235	--	pF
Output Capacitance		C_{oss}	--	29	--	
Reverse Transfer Capacitance		C_{rss}	--	6.5	--	
Switching						
Turn-On Delay Time	$V_{GS} = 25V, I_D = 0.5A,$ $V_{DS} = 225V, R_G = 25\Omega$ (Note 4,5)	$t_{d(on)}$	--	14.7	--	nS
Turn-On Rise Time		t_r	--	32.8	--	
Turn-Off Delay Time		$t_{d(off)}$	--	25.2	--	
Turn-Off Fall Time		t_f	--	23.7	--	
Drain-Source Diode Characteristics and Maximum Ratings						
Maximum Continuous Drain-Source Diode Forward Current		I_S	--	--	0.5	A
Maximum Pulsed Drain-Source Diode Forward Current		I_{SM}	--	--	4.0	A
Drain-Source Diode Forward Voltage	$V_{GS} = 0V, I_S = 0.5A$	V_{SD}	--	--	1.4	V
Reverse Recovery Time	$V_{GS} = 0V, I_S = 1A$ $di_F/dt = 100A/\mu S$ (Note 4)	t_{rr}	--	110	--	nS
Reverse Recovery Charge		Q_{rr}	--	0.35	--	μC

Notes:

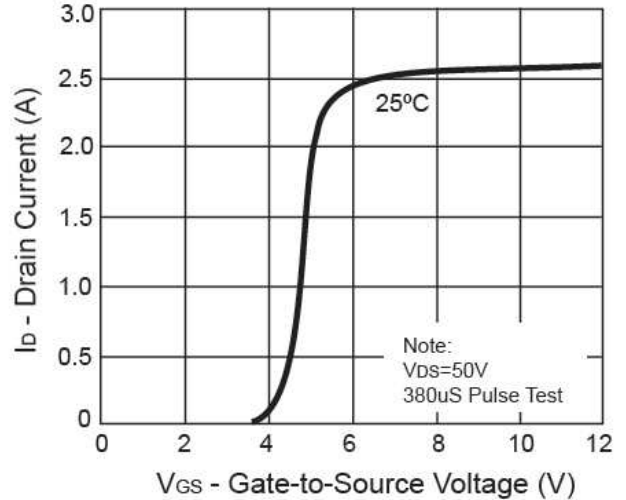
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L=75mH, I_{AS}=1.6A, V_{DD}=50V, R_G=25\Omega, \text{Starting } T_J=25^\circ C$
3. $I_{SD} \leq 0.5A, di/dt \leq 300A/\mu S, V_{DD} \leq BV_{DSS}, \text{Starting } T_J=25^\circ C$
4. Pulse test: pulse width $\leq 300\mu S$.
5. Essentially independent of operating temperature
6. a) Reference point of the is the drain $R_{\theta_{JL}}$ lead
b) When mounted on 3"x4.5" FR-4 PCB without any pad copper in a still air environment
($R_{\theta_{JA}}$ is the sum of the junction-to-case and case-to-ambient thermal resistance. $R_{\theta_{CA}}$ is determined by the user's board design)

Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

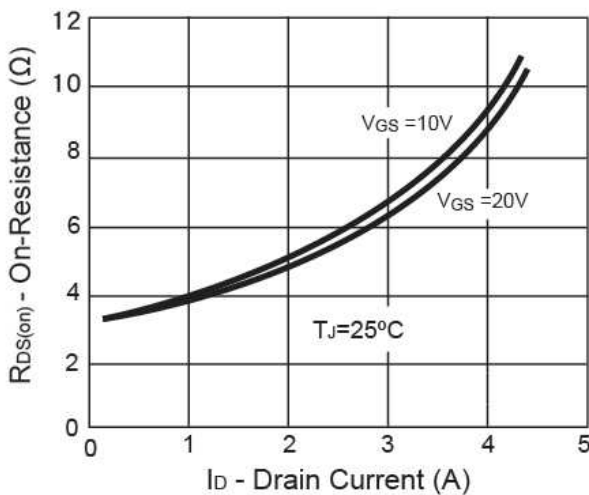
Output Characteristics



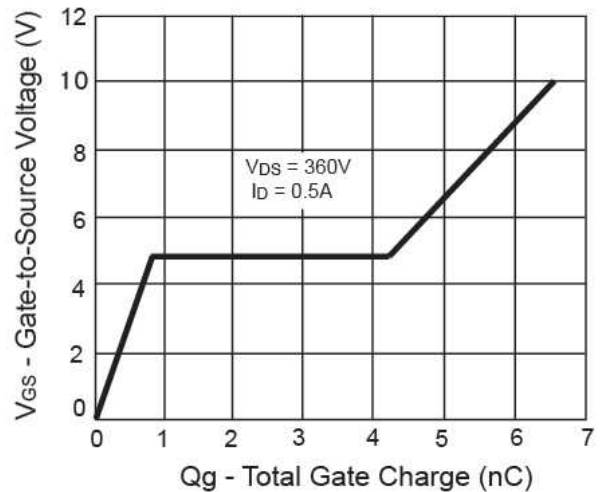
Transfer Characteristics



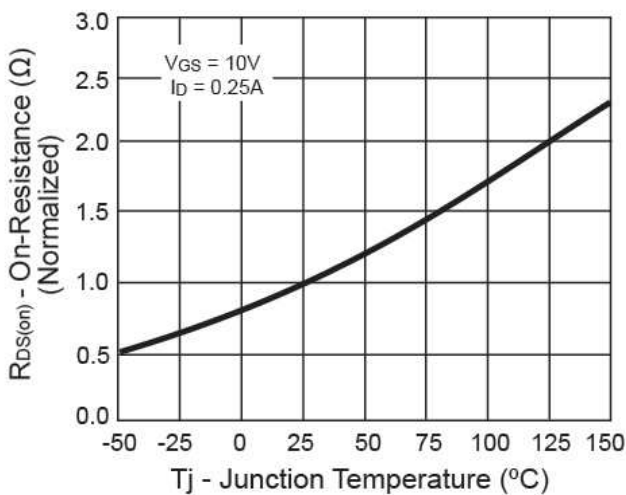
On-Resistance vs. Drain Current



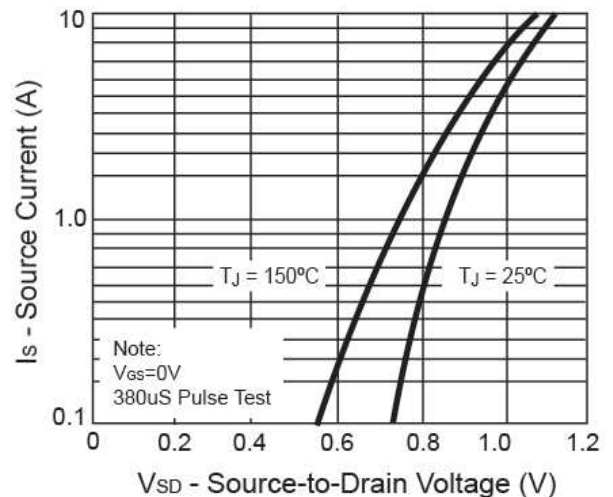
Gate Charge



On-Resistance vs. Junction Temperature



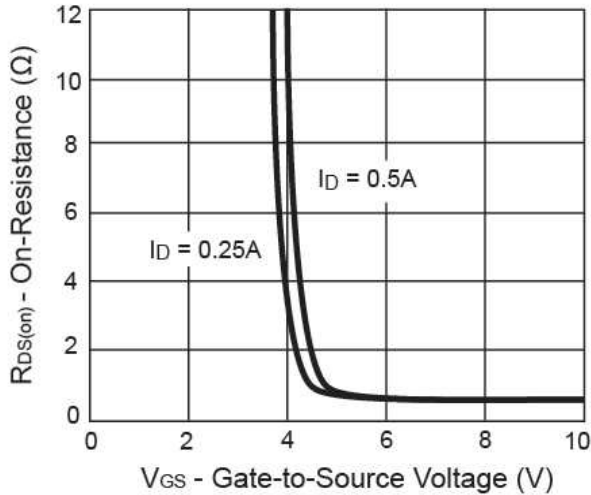
Source-Drain Diode Forward Voltage



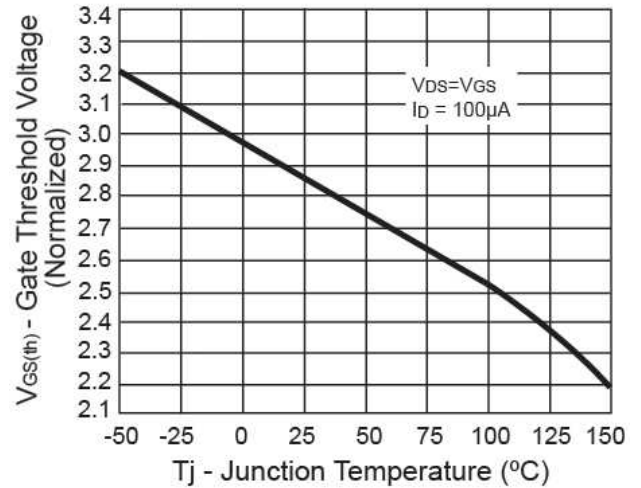


Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

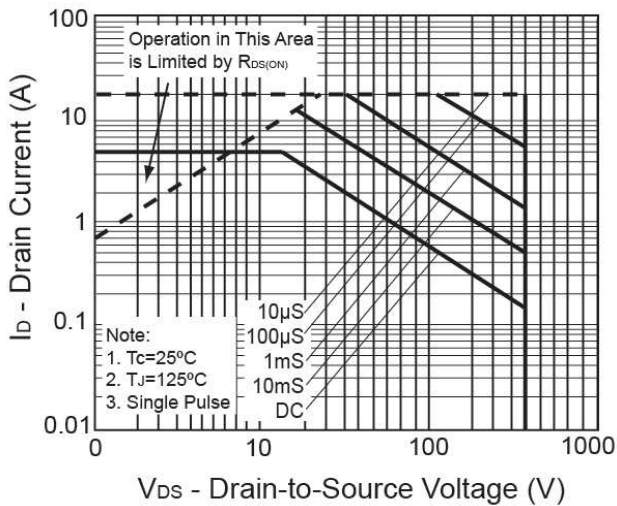
On-Resistance vs. Gate-Source Voltage



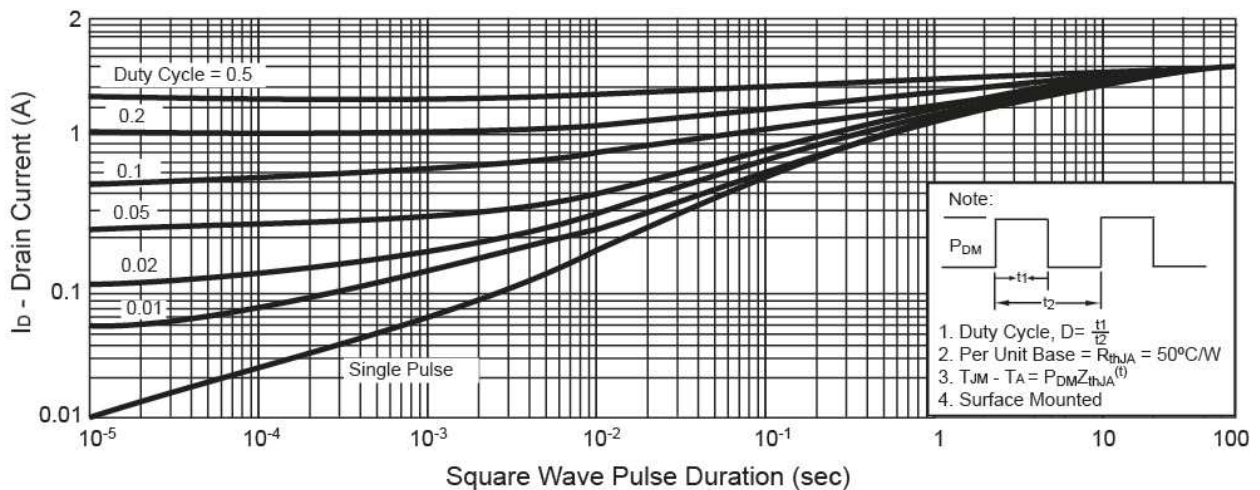
Threshold Voltage



Maximum Safe Operating Area

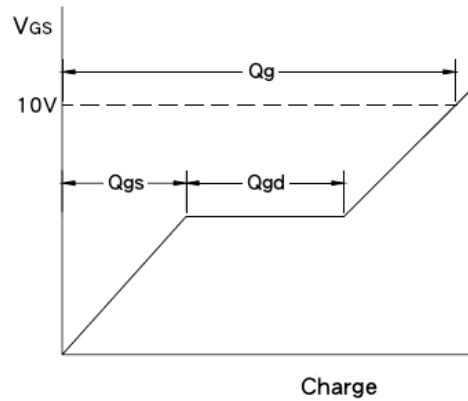
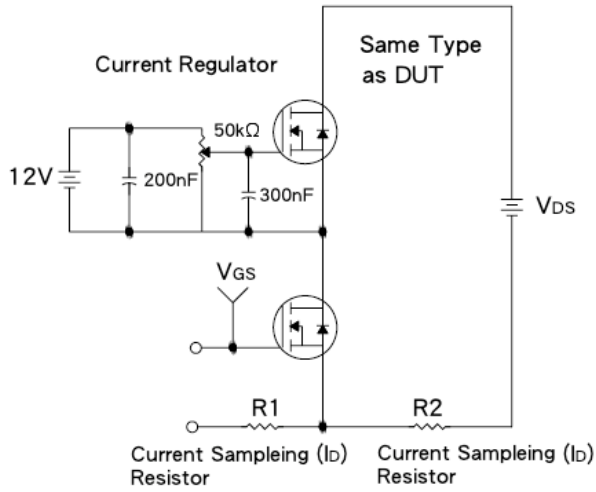


Normalized Thermal Transient Impedance, Junction-to-Ambient

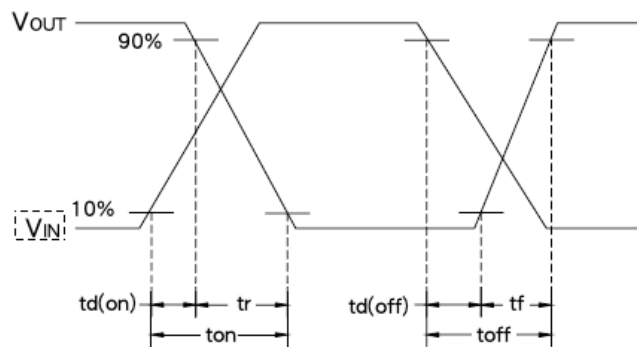
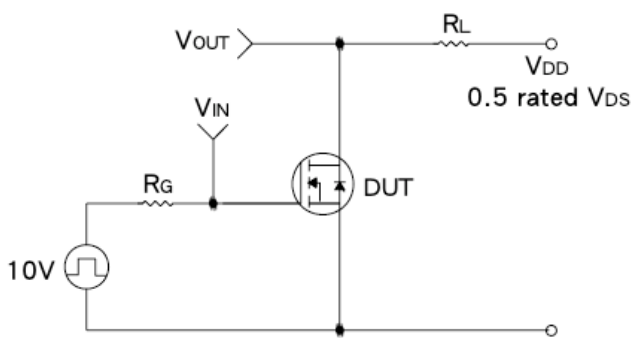




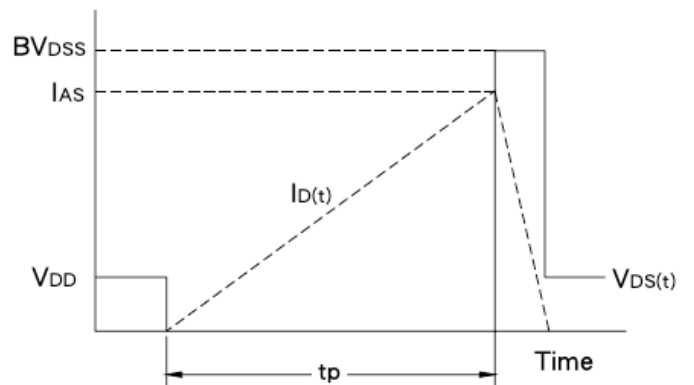
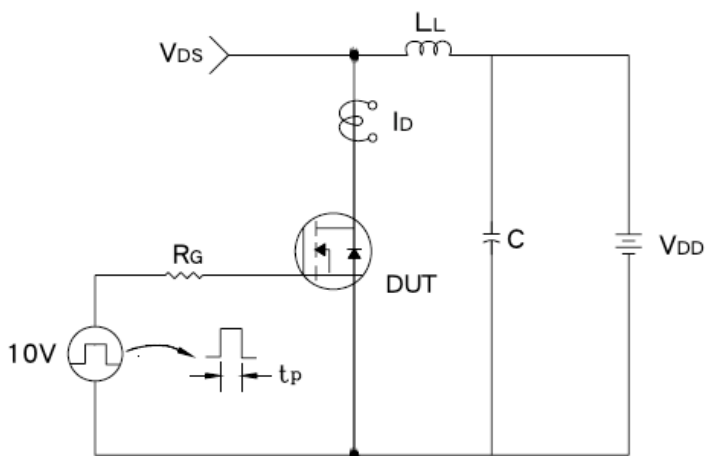
Gate Charge Test Circuit & Waveform



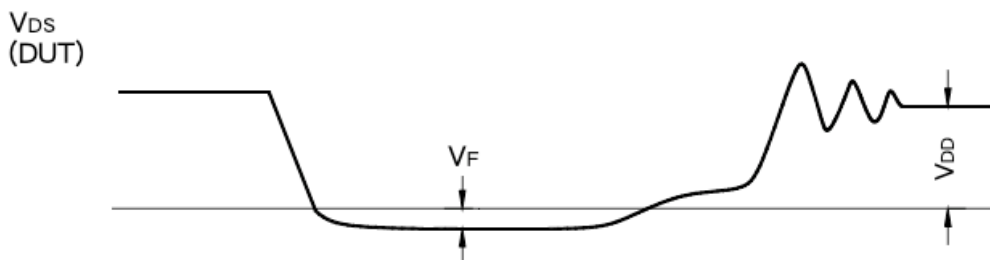
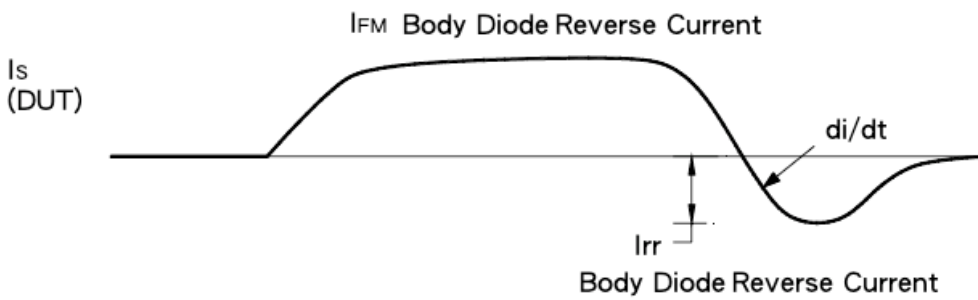
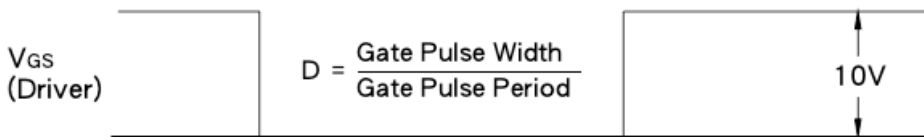
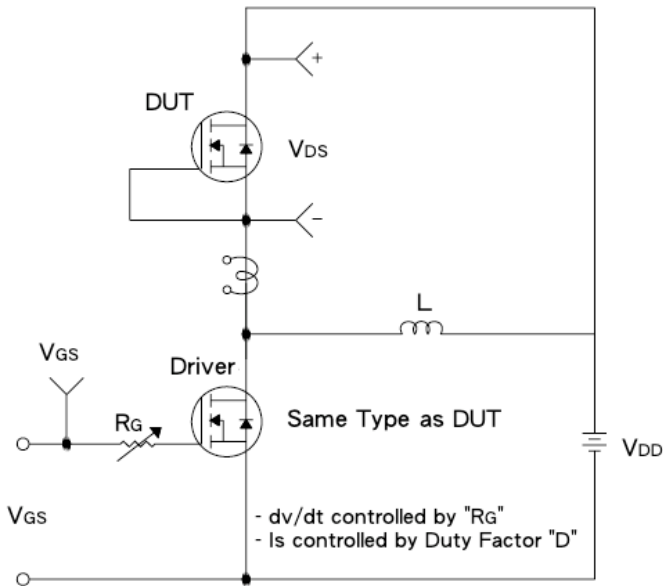
Resistive Switching Test Circuit & Waveform



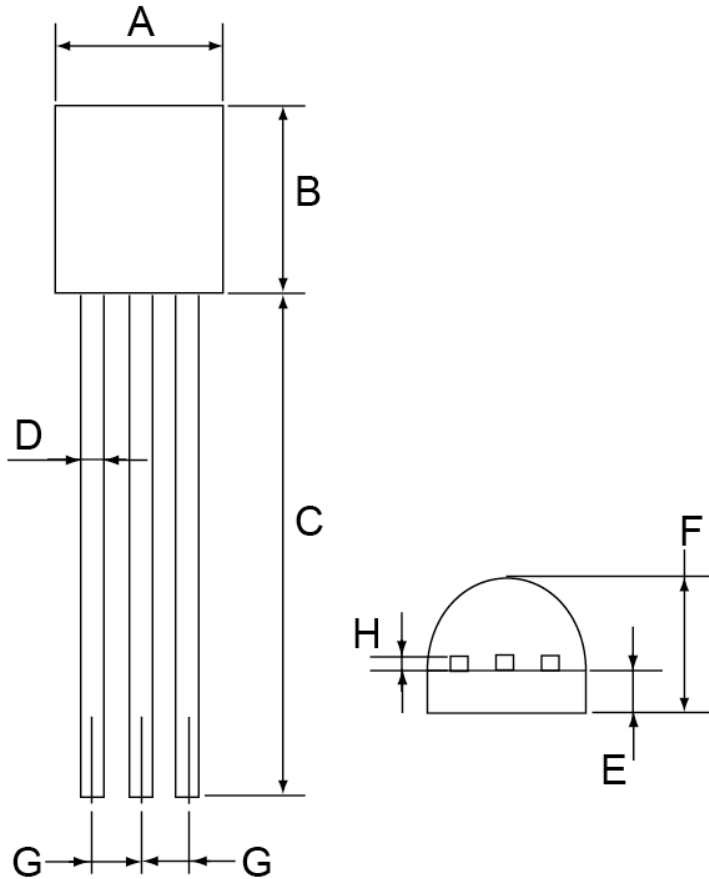
E_{AS} Test Circuit & Waveform



Diode Reverse Recovery Time Test Circuit & Waveform

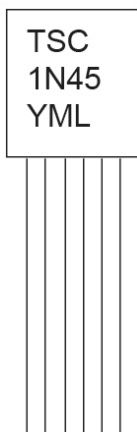


TO-92 Mechanical Drawing



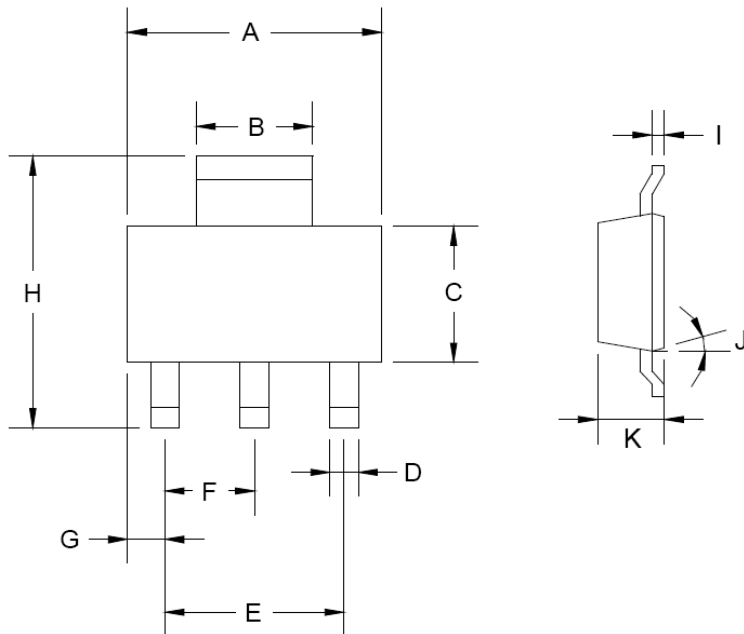
TO-92 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.70	0.169	0.185
B	4.30	4.70	0.169	0.185
C	13.53 (typ)		0.532 (typ)	
D	0.39	0.49	0.015	0.019
E	1.18	1.28	0.046	0.050
F	3.30	3.70	0.130	0.146
G	1.27	1.31	0.050	0.051
H	0.33	0.43	0.013	0.017

Marking Diagram



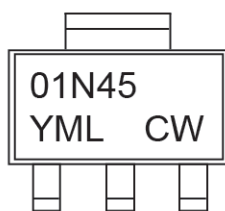
Y = Year Code
M = Month Code
(A=Jan, B=Feb, C=Mar, D=Apl, E=May, F=Jun, G=Jul, H=Aug, I=Sep, J=Oct, K=Nov, L=Dec)
L = Lot Code

SOT-223 Mechanical Drawing



DIM	SOT-223 DIMENSION			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.350	6.850	0.250	0.270
B	2.900	3.100	0.114	0.122
C	3.450	3.750	0.136	0.148
D	0.595	0.635	0.023	0.025
E	4.550	4.650	0.179	0.183
F	2.250	2.350	0.088	0.093
G	0.835	1.035	0.032	0.041
H	6.700	7.300	0.263	0.287
I	0.250	0.355	0.010	0.014
J	10°	16°	10°	16°
K	1.550	1.800	0.061	0.071

Marking Diagram



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