



**Features** 

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# **TSM35N10** 100V N-Channel Power MOSFET

# TO-252 (DPAK)

Advanced Trench Technology

Low Crss typical @ 45pF (Typ.)

Low gate charge typical @ 34nC (Typ.)

Note: "G" denote for Halogen Free Product

Low  $R_{DS(ON)} 37m\Omega$  (Max.)

**Ordering Information** 

Part No.

TSM35N10CP ROG

Pin Definition:

Packing

2.5Kpcs / 13" Reel

1. Gate 2. Drain

3. Source

# PRODUCT SUMMARY

V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (mΩ)	I <sub>D</sub> (A)
100	37 @ V <sub>GS</sub> =10V	32

## **Block Diagram**

# Gate O

N-Channel MOSFET

### Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Package

TO-252

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	100	V	
Gate-Source Voltage		V <sub>GS</sub>	±20	V	
	T <sub>C</sub> =25℃		32		
	T <sub>C</sub> =70℃		26	A	
Continuous Drain Current	T <sub>A</sub> =25℃	– I <sub>D</sub>	5		
	T <sub>A</sub> =70℃		4		
Drain Current-Pulsed Note 1		I <sub>DM</sub>	70	А	
Avalanche Current, L=0.1mH		I <sub>AS</sub> , I <sub>AR</sub>	35	А	
Avalanche Energy, L=0.1mH		E <sub>AS</sub> , E <sub>AR</sub>	61	mJ	
	T <sub>C</sub> =25℃		83.3		
Meximum Devier Discinction	T <sub>C</sub> =70℃		53.3	۱۸/	
Maximum Power Dissipation	$T_A=25^{\circ}$ $P_D$		2	W	
	T <sub>A</sub> =70℃		1.3	l	
Storage Temperature Range		T <sub>STG</sub>	-55 to +150	ĉ	
Operating Junction Temperature Range		TJ	-55 to +150	ĉ	

\* Limited by maximum junction temperature

### **Thermal Performance**

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	RƏ <sub>JC</sub>	1.5	°C/W
Thermal Resistance - Junction to Ambient	RƏ <sub>JA</sub>	62	°C/W



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### Electrical Specifications (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Тур	Max	Uni
Static						1
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_{D} = 250uA$	BV <sub>DSS</sub>	100			V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 10A$	R <sub>DS(ON)</sub>		30	37	mΩ
	$V_{GS} = 4.5V, I_D = 10A$	R <sub>DS(ON)</sub>		32	42	mΩ
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 uA$	V <sub>GS(TH)</sub>	1	2	3	V
Zero Gate Voltage Drain Current	$V_{DS} = 100V, V_{GS} = 0V$	I <sub>DSS</sub>			1	uA
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I <sub>GSS</sub>			±100	nA
Dynamic					•	
Total Gate Charge	$V_{DS} = 50V, I_D = 10A,$ $V_{GS} = 10V$	Qg		34		nC
Gate-Source Charge		Q <sub>gs</sub>		6		
Gate-Drain Charge		$Q_gd$		9		
Input Capacitance	$V_{DS} = 30V, V_{GS} = 0V,$ f = 1.0MHz	C <sub>iss</sub>		1598		pF
Output Capacitance		C <sub>oss</sub>		132		
Reverse Transfer Capacitance		C <sub>rss</sub>		45		
Switching						
Turn-On Delay Time	$V_{GS} = 10V, V_{DS} = 50V,$ $R_G = 3\Omega$	t <sub>d(on)</sub>		7		
Turn-On Rise Time		t <sub>r</sub>		7		
Turn-Off Delay Time		t <sub>d(off)</sub>		29		nS
Turn-Off Fall Time		t <sub>f</sub>		7		
Drain-Source Diode Characteristic	s and Maximum Rating					
Drain-Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =10A	V <sub>SD</sub>	-	0.7		V
Reverse Recovery Time	I <sub>S</sub> = 10A, T <sub>J</sub> =25 °C	t <sub>fr</sub>		32		nS
Reverse Recovery Charge	dl/dt = 500A/us	Q <sub>fr</sub>		200		nC

Notes:

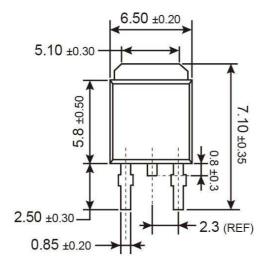
1. Pulse Test: Pulse Width  $\leq$  300µs, Duty Cycle  $\leq$  2%.

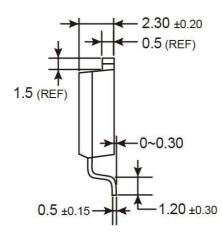
 $R\theta_{JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal 2. reference is defined as the solder mounting surface of the drain pins.  $R\theta_{JC}$  is guaranteed by design while  $R\theta_{CA}$ is determined by the user's board design. R0JA shown below for single device operation on FR-4 in still air



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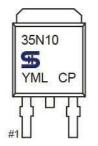
# **TO-252 Mechanical Drawing**





Unit: Millimeters

## **Marking Diagram**



- Y = Year Code
- **M** = Month Code for Halogen Free Product
  - (**O**=Jan, **P**=Feb, **Q**=Mar, **R**=Apl, **S**=May, **T**=Jun, **U**=Jul, **V**=Aug, **W**=Sep, **X**=Oct, **Y**=Nov, **Z**=Dec)
- L = Lot Code



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