

TO-252  
(DPAK)



Pin Definition:

1. Gate
2. Drain
3. Source

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ (m $\Omega$ )	$I_D$ (A)
200	92 @ $V_{GS}=10V$	18

### Features

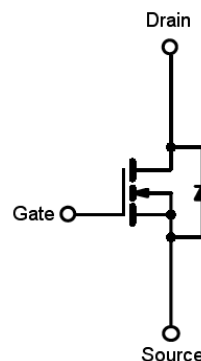
- Advanced Trench Technology
- Low  $R_{DS(ON)}$  92m $\Omega$  (Max.)
- Low gate charge typical @ 55nC (Typ.)
- Low  $C_{rss}$  typical @ 73pF (Typ.)

### Ordering Information

Part No.	Package	Packing
TSM19N20CP ROG	TO-252	2.5Kpcs / 13" Reel

Note: "G" denote for Halogen Free Product

### Block Diagram



N-Channel MOSFET

### Absolute Maximum Rating ( $T_a = 25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	200	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current @ $T_C=25^{\circ}C$	$I_D$	18	A
Drain Current Pulsed (Note 1)	$I_{DM}$	72	A
Avalanche Current	$I_{AS}$	8	A
Avalanche Energy, L=10mH	$E_{AS}$	320	mJ
Maximum Power Dissipation @ $T_C=25^{\circ}C$	$P_D$	48	W
Storage Temperature Range	$T_{STG}$	-55 to +150	$^{\circ}C$
Operating Junction Temperature Range	$T_J$	-55 to +150	$^{\circ}C$

\* Limited by maximum junction temperature

### Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	$R_{\theta JC}$	2.6	$^{\circ}C/W$
Thermal Resistance - Junction to Ambient	$R_{\theta JA}$	50	$^{\circ}C/W$

Notes: Surface mounted on FR4 board  $t \leq 10sec$

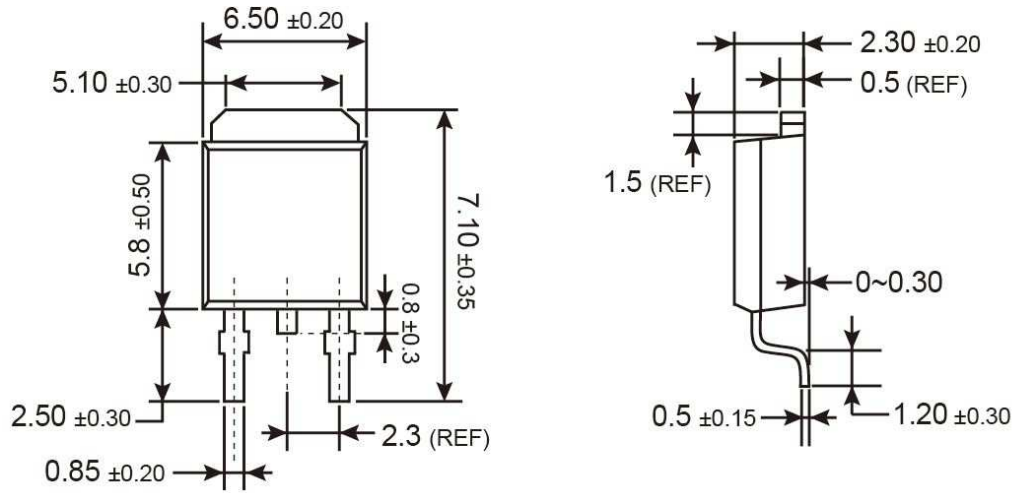
**Electrical Specifications** (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250uA	BV <sub>DSS</sub>	200	--	--	V
Drain-Source On-State Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 10A	R <sub>DS(ON)</sub>	--	80	92	mΩ
Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250uA	V <sub>GS(TH)</sub>	2	--	4	V
Zero Gate Voltage Drain Current	V <sub>DS</sub> = 160V, V <sub>GS</sub> = 0V	I <sub>DSS</sub>	--	--	1	uA
Gate Body Leakage	V <sub>GS</sub> = ±30V, V <sub>DS</sub> = 0V	I <sub>GSS</sub>	--	--	±100	nA
<b>Dynamic</b>						
Total Gate Charge	V <sub>DS</sub> = 100V, I <sub>D</sub> = 10A, V <sub>GS</sub> = 10V	Q <sub>g</sub>	--	55	--	nC
Gate-Source Charge		Q <sub>gs</sub>	--	18	--	
Gate-Drain Charge		Q <sub>gd</sub>	--	17	--	
Input Capacitance	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V, f = 1.0MHz	C <sub>iss</sub>	--	2300	--	pF
Output Capacitance		C <sub>oss</sub>	--	145	--	
Reverse Transfer Capacitance		C <sub>rss</sub>	--	73	--	
<b>Switching</b>						
Turn-On Delay Time	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 100V, R <sub>G</sub> = 3Ω	t <sub>d(on)</sub>	--	17	--	nS
Turn-On Rise Time		t <sub>r</sub>	--	12	--	
Turn-Off Delay Time		t <sub>d(off)</sub>	--	28	--	
Turn-Off Fall Time		t <sub>f</sub>	--	10	--	
<b>Drain-Source Diode Characteristics and Maximum Rating</b>						
Drain-Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =10A	V <sub>SD</sub>	--	--	1.3	V
Reverse Recovery Time	I <sub>S</sub> = 10A, T <sub>J</sub> =25 °C	t <sub>fr</sub>	--	82	--	nS
Reverse Recovery Charge	di/dt = 100A/us	Q <sub>fr</sub>	--	276	--	nC

**Notes:**

- Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- Rθ<sub>JA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Rθ<sub>JC</sub> is guaranteed by design while Rθ<sub>CA</sub> is determined by the user's board design. Rθ<sub>JA</sub> shown below for single device operation on FR-4 in still air

## TO-252 Mechanical Drawing



Unit: Millimeters

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