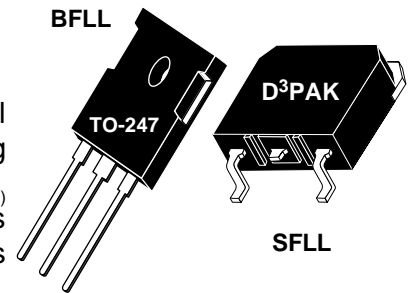
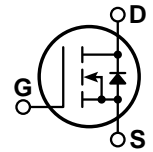


POWER MOS 7® FREDFET

Power MOS 7® is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7® by significantly lowering $R_{DS(ON)}$ and Q_g . Power MOS 7® combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.



- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge, Q_g
- Increased Power Dissipation
- Easier To Drive
- TO-247 or Surface Mount D3PAK Package
- **FAST RECOVERY BODY DIODE**




MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT30M75	UNIT
V_{DSS}	Drain-Source Voltage	300	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	44	Amps
I_{DM}	Pulsed Drain Current ^①	176	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	329	Watts
	Linear Derating Factor	2.63	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	44	Amps
E_{AR}	Repetitive Avalanche Energy ^①	30	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	1300	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu\text{A}$)	300			Volts
$I_{D(on)}$	On State Drain Current ^② ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	44			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, 22A$)			0.075	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = 300V, V_{GS} = 0V$)			250	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 240V, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			1000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1mA$)	3		5	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

APT Website - <http://www.advancedpower.com>

DYNAMIC CHARACTERISTICS

APT30M75 BFLL - SFLL

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1 \text{ MHz}$		3018		pF
C_{oss}	Output Capacitance			771		
C_{riss}	Reverse Transfer Capacitance			43		
Q_g	Total Gate Charge ^③	$V_{GS} = 10V$ $V_{DD} = 200V$ $I_D = 44A @ 25^\circ C$		57		nC
Q_{gs}	Gate-Source Charge			21		
Q_{gd}	Gate-Drain ("Miller") Charge			23		
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 15V$ $V_{DD} = 200V$ $I_D = 44A @ 25^\circ C$ $R_G = 0.6\Omega$		13		ns
t_r	Rise Time			3		
$t_{d(off)}$	Turn-off Delay Time			20		
t_f	Fall Time			2		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			44	Amps
I_{SM}	Pulsed Source Current ^① (Body Diode)			176	
V_{SD}	Diode Forward Voltage ^② ($V_{GS} = 0V, I_S = -44A$)			1.3	Volts
dv/dt	Peak Diode Recovery dv/dt ^⑤			8	V/ns
t_{rr}	Reverse Recovery Time ($I_S = -44A, di/dt = 100A/\mu s$)	$T_j = 25^\circ C$		200	ns
		$T_j = 125^\circ C$		400	
Q_{rr}	Reverse Recovery Charge ($I_S = -44A, di/dt = 100A/\mu s$)	$T_j = 25^\circ C$		1.1	μC
		$T_j = 125^\circ C$		2.7	
I_{RRM}	Peak Recovery Current ($I_S = -44A, di/dt = 100A/\mu s$)	$T_j = 25^\circ C$		10	Amps
		$T_j = 125^\circ C$		15.1	

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.38	$^\circ C/W$
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature

② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting $T_j = +25^\circ C$, $L = 1.34mH$, $R_G = 25\Omega$, Peak $I_L = 44A$

⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. $I_S \leq -I_D 44A$ $di/dt \leq 700A/\mu s$ $V_R \leq V_{DSS}$ $T_j \leq 150^\circ C$

APT Reserves the right to change, without notice, the specifications and information contained herein.

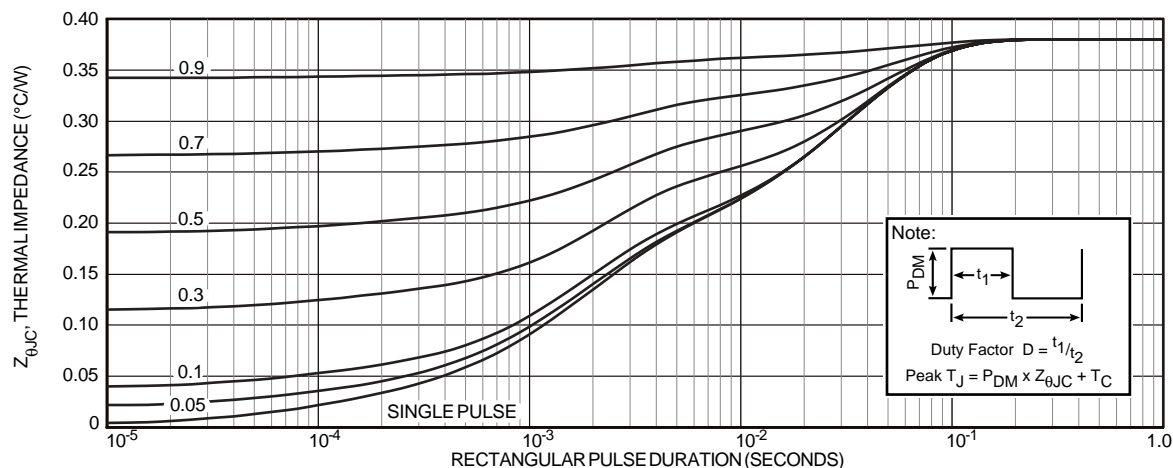


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Typical Performance Curves

APT30M75 BFLL - SFL

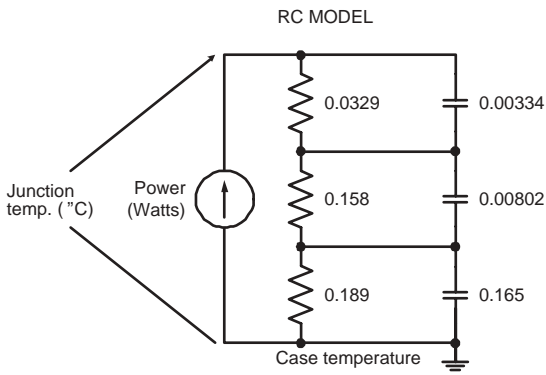


FIGURE 2, TRANSIENT THERMAL IMPEDANCE MODEL

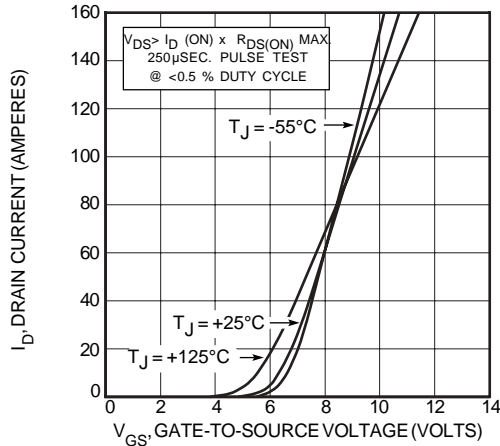


FIGURE 4, TRANSFER CHARACTERISTICS

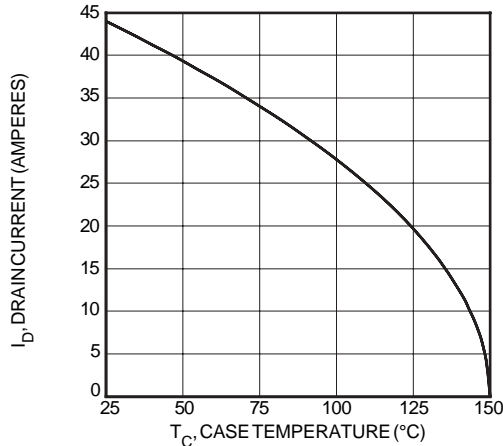


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

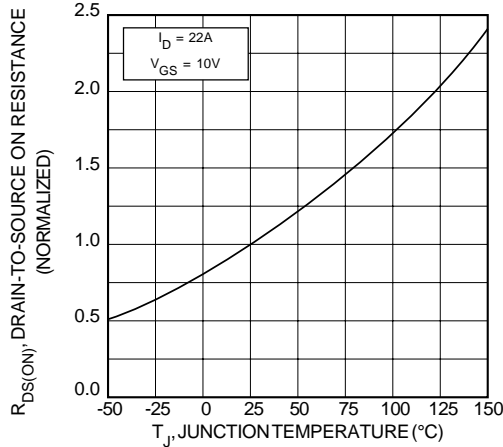


FIGURE 8, $R_{DS(ON)}$ vs. TEMPERATURE

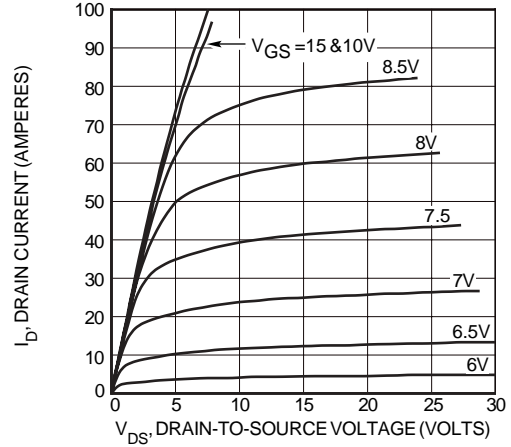


FIGURE 3, LOW VOLTAGE OUTPUT CHARACTERISTICS

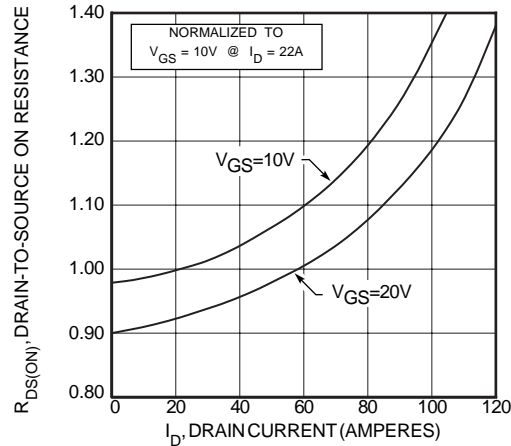


FIGURE 5, $R_{DS(ON)}$ vs DRAIN CURRENT

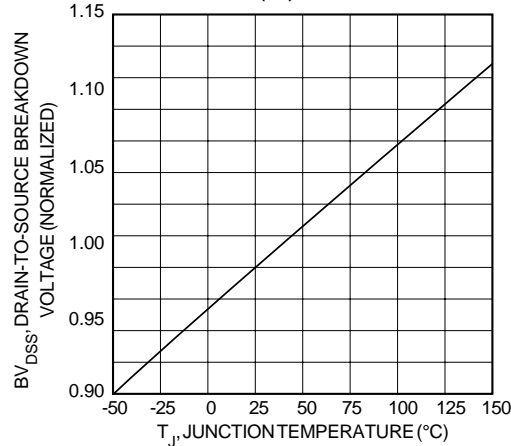


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

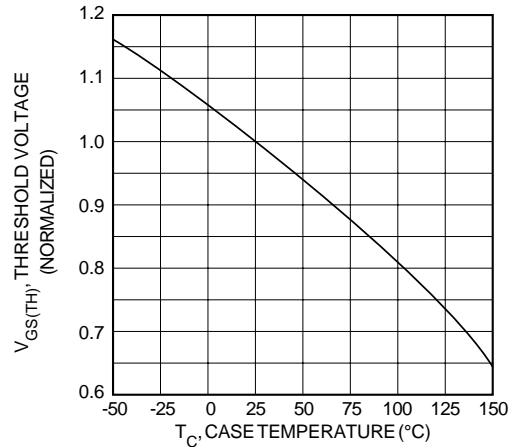


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

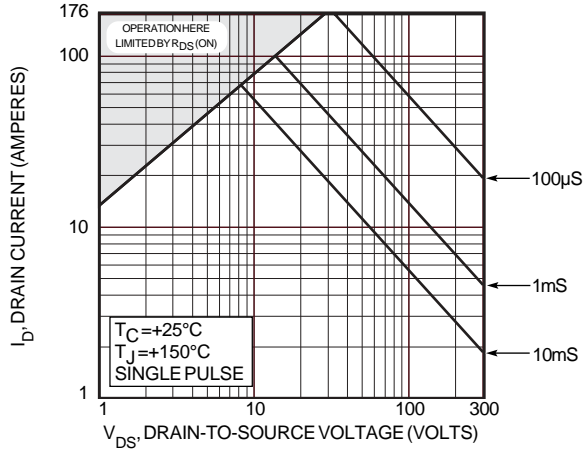


FIGURE 10, MAXIMUM SAFE OPERATING AREA

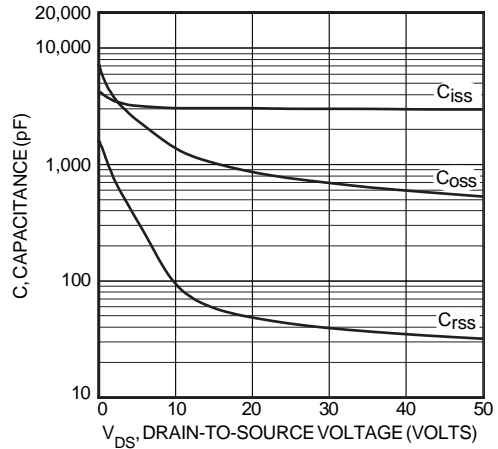


FIGURE 11, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

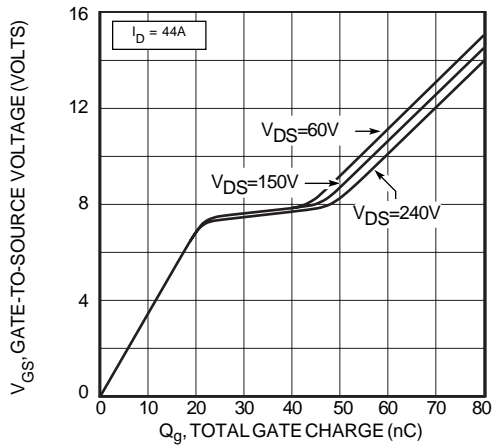


FIGURE 12, GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

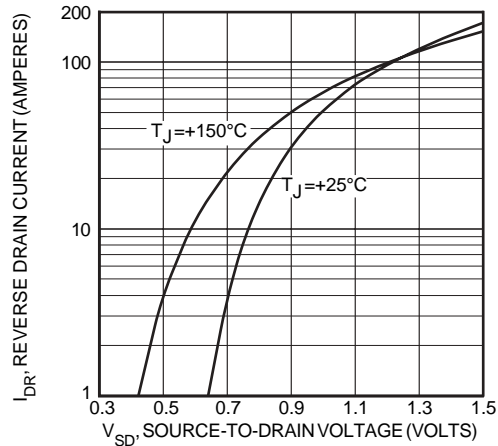
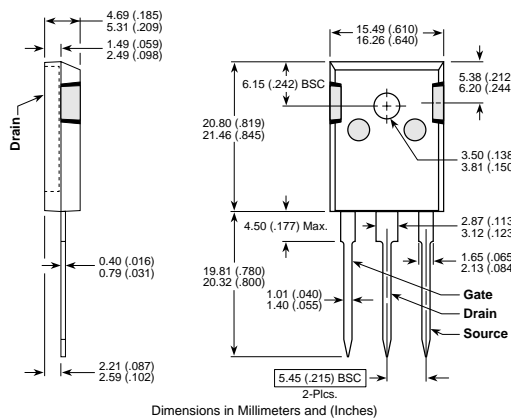
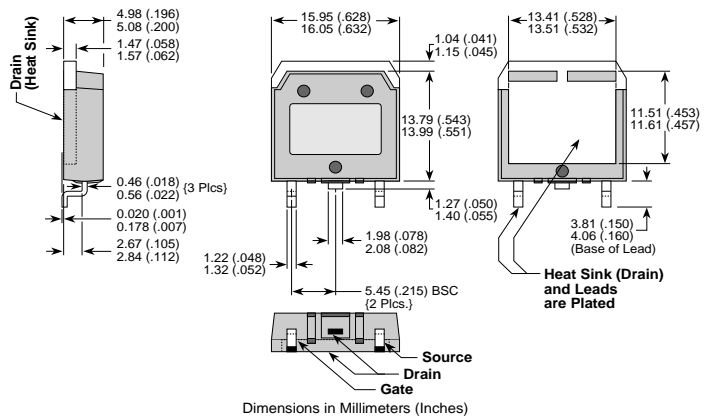


FIGURE 13, SOURCE-DRAIN DIODE FORWARD VOLTAGE

TO-247 Package Outline



D³PAK Package Outline



050-7164 Rev A 1-2003

APT's devices are covered by one or more of the following U.S. patents:	4,895,810	5,045,903	5,089,434	5,182,234	5,019,522	5,262,336
	5,256,583	4,748,103	5,283,202	5,231,474	5,434,095	5,528,058