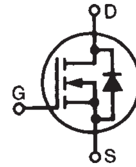
IXYS Advance Technical Information

GigaMOS™ Trench™ HiperFET™ Power MOSFET

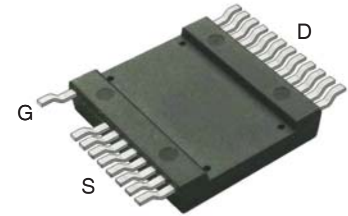
MMIX1F160N30T

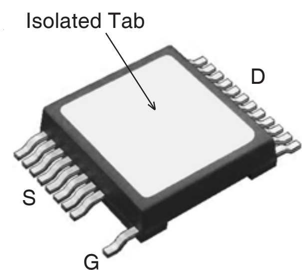
(Electrically Isolated Tab)

V_{DSS}	=	300V
I_{D25}	=	102A
$R_{DS(on)}$	≤	20mΩ
t_{rr}	≤	200ns



N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode





G = Gate D = Drain
S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	300	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	300	V
V_{GSS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	102	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	440	A
I_A	T_C = 25°C	40	A
E_{AS}	T_C = 25°C	3	J
P_D	T_C = 25°C	570	W
dv/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150°C$	20	V/ns
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6mm (0.062 in.) from Case for 10s	300	°C
T_{SOLD}	Plastic Body for 10s	260	°C
V_{ISOL}	50/60 Hz, 1 Minute	2500	V~
F_C	Mounting Force	50..200 / 11..45	N/lb.
Weight		8	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 3mA	300			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 8mA	2.5		5.0	V
I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			±200	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0V			50	µA
	Note 2, T_J = 125°C			3	mA
$R_{DS(on)}$	V_{GS} = 10V, I_D = 60A, Note 1			20	mΩ

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Substrate
  - Excellent Thermal Transfer
  - Increased Temperature and Power Cycling Capability
  - High Isolation Voltage (2500V~)
- Very High Current Handling Capability
- Fast Intrinsic Diode
- Avalanche Rated
- Very Low $R_{DS(on)}$

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- DC-DC Converters and Off-Line UPS
- Primary-Side Switch
- High Speed Power Switching Applications

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Symbol	Test Conditions ($T_J = 25°C$, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	$V_{DS} = 10V$, $I_D = 60A$, Note 1	100	160		S
C_{iss}	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1MHz		28		nF
C_{oss}			1770		pF
C_{rss}			125		pF
R_{GI}	Gate Input Resistance		1.4		Ω
$t_{d(on)}$	**Resistive Switching Times** $V_{GS} = 15V$, $V_{DS} = 0.5 \bullet V_{DSS}$, $I_D = 80A$ $R_G = 1\Omega$ (External)		37		ns
t_r			38		ns
$t_{d(off)}$			105		ns
t_f			25		ns
$Q_{g(on)}$	$V_{GS} = 10V$, $V_{DS} = 0.5 \bullet V_{DSS}$, $I_D = 80A$		335		nC
Q_{gs}			123		nC
Q_{gd}			56		nC
R_{thJC}				0.22	°C/W
R_{thCS}			0.05		°C/W
R_{thJA}			30		°C/W

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25°C$, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
I_S	$V_{GS} = 0V$			160	A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			640	A
V_{SD}	$I_F = 60A$, $V_{GS} = 0V$, Note 1			1.3	V
t_{rr}	$I_F = 80A$, $V_{GS} = 0V$ -di/dt = 100A/μs $V_R = 75V$			200	ns
I_{RM}			13		A
Q_{RM}			1.06		μC

Notes:

1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.
2. Part must be heatsunk for high-temp Ices measurement.

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

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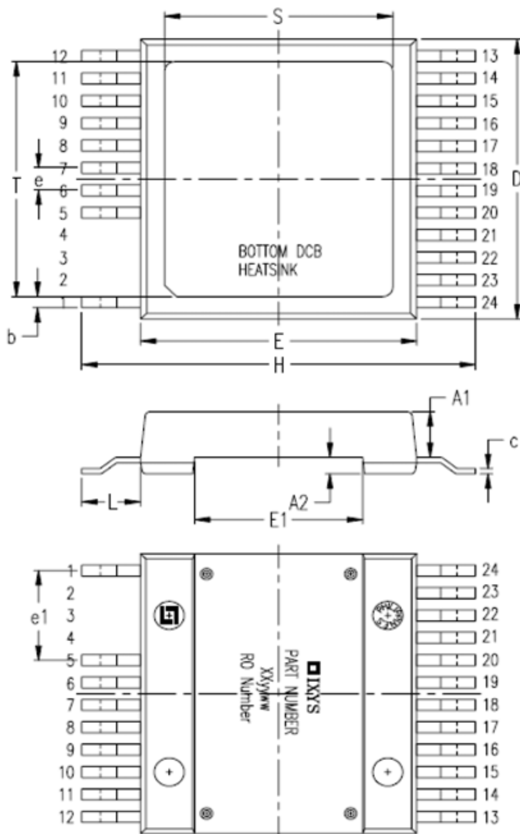
IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,850,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405 B2 6,710,463 6,727,585 6,759,692 6,771,478 B2 7,005,734 B2 7,063,975 B2 7,071,537 7,157,338B2

Package Outline



A

(SCALE: 5X)
α
L2
L1

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.209	.224	5.30	5.70
A1	.154	.161	3.90	4.10
A2	.055	.063	1.40	1.60
b	.035	.045	0.90	1.15
c	.018	.026	0.45	0.65
D	.976	.994	24.80	25.25
E	.898	.915	22.80	23.25
E1	.543	.559	13.80	14.20
e	.079 BSC		2.00 BSC	
e1	.315 BSC		8.00 BSC	
H	1.272	1.311	32.30	33.30
L	.181	.209	4.60	5.30
L1	.051	.067	1.30	1.70
L2	.000	.006	0.00	0.15
S	.736	.760	18.70	19.30
T	.815	.839	20.70	21.30
α	0	4°	0	4°

PIN: 1 = Gate
5-12 = Source
13-24 = Drain

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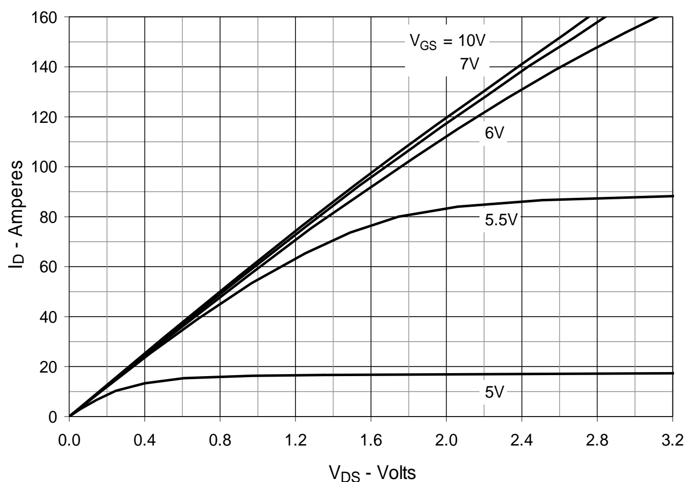

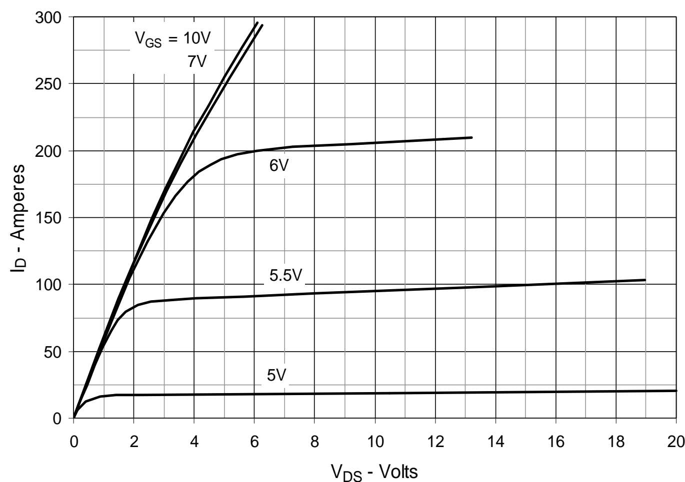

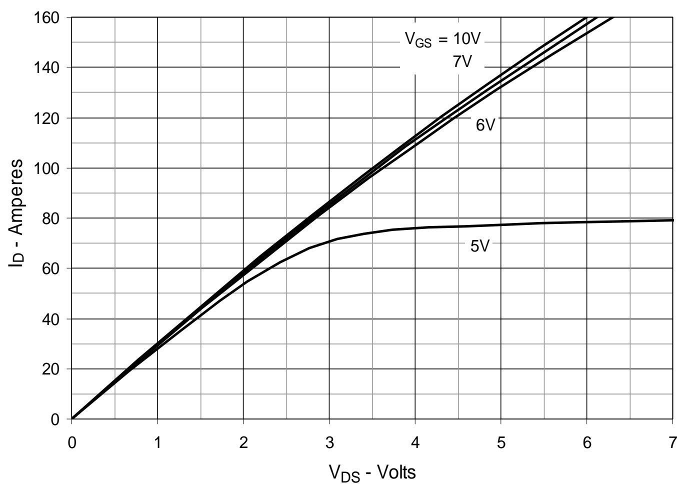

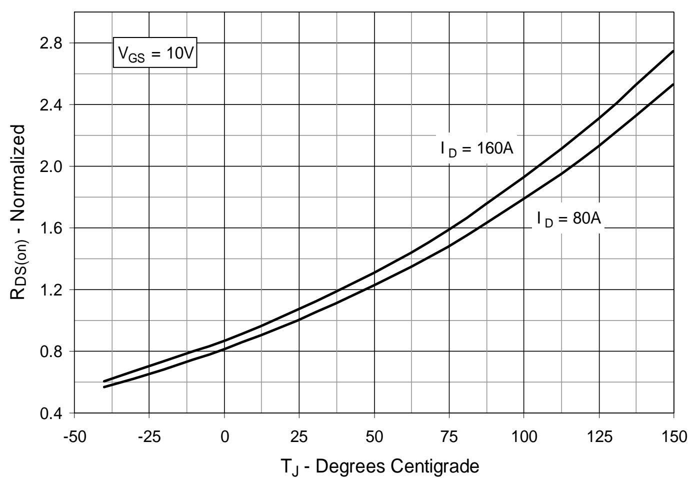

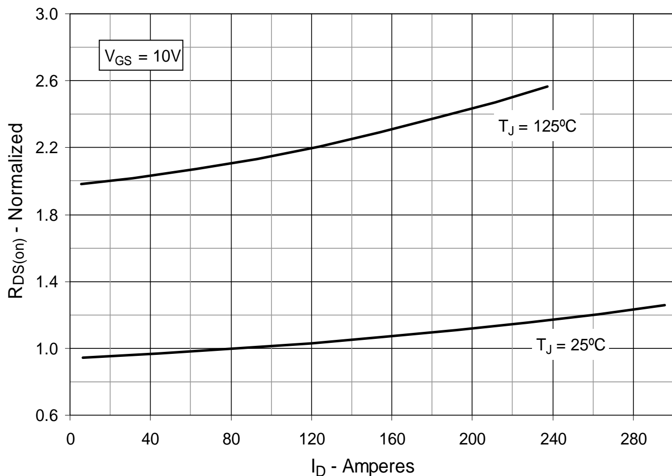

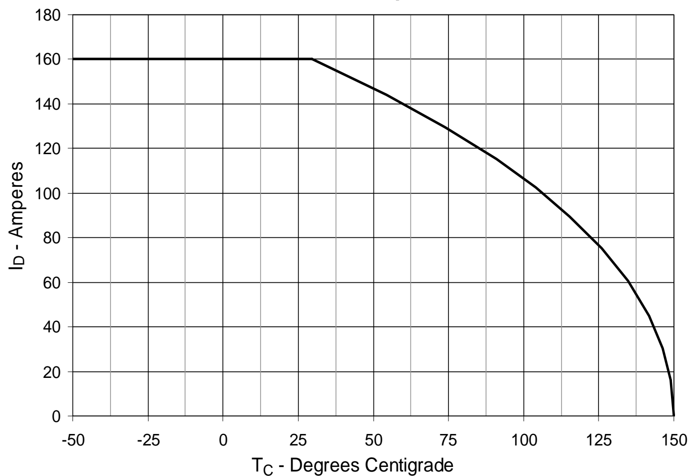

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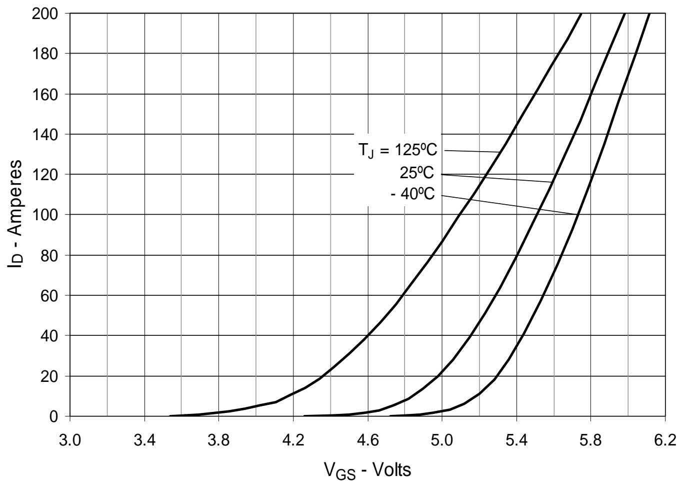

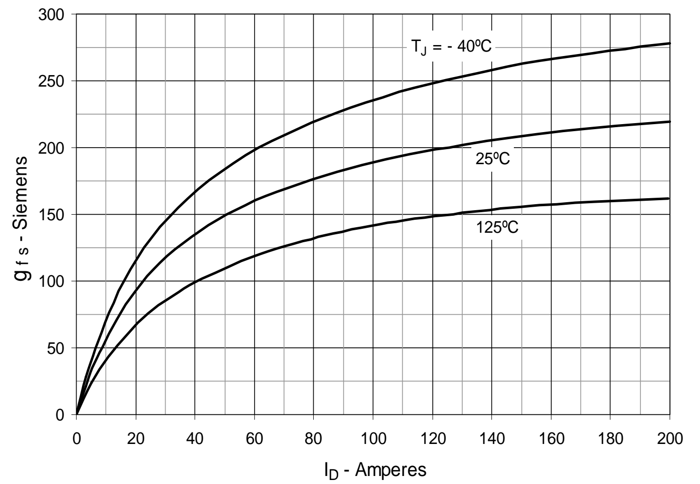

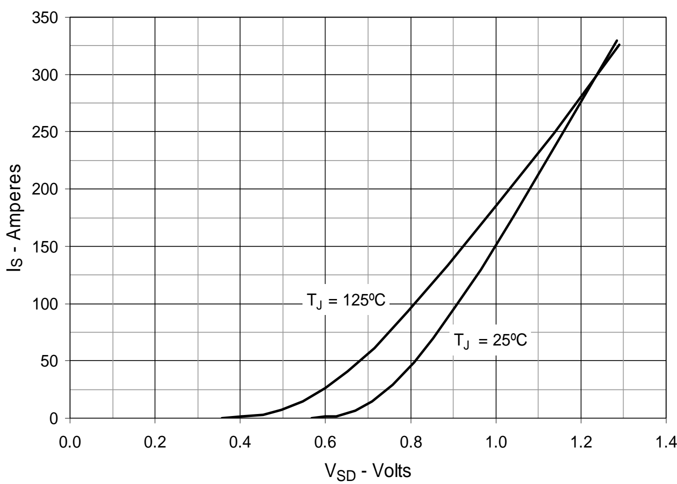

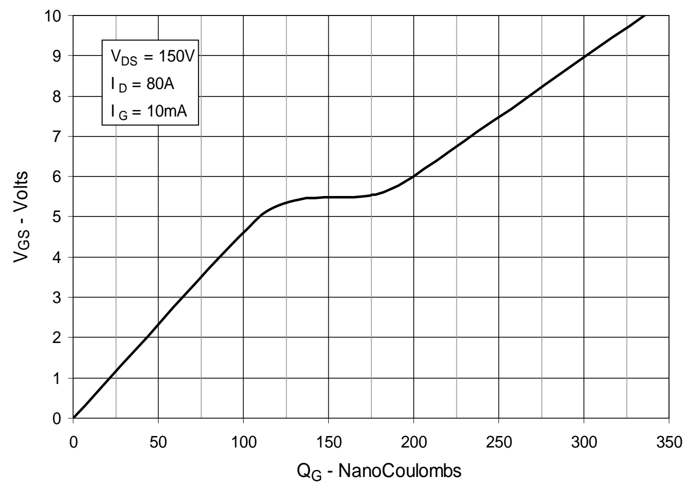

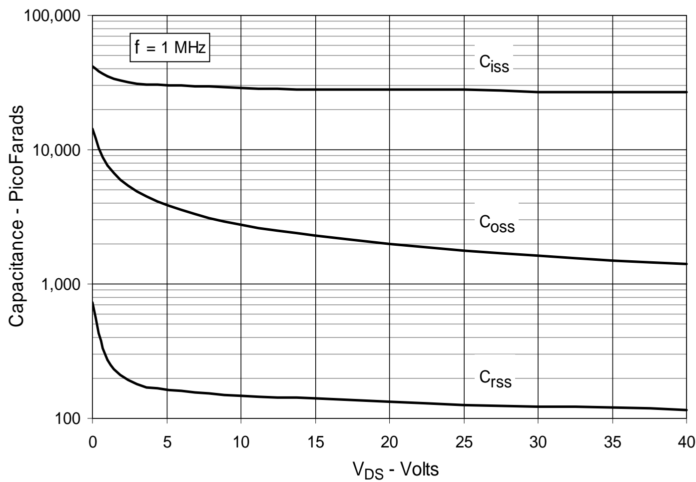

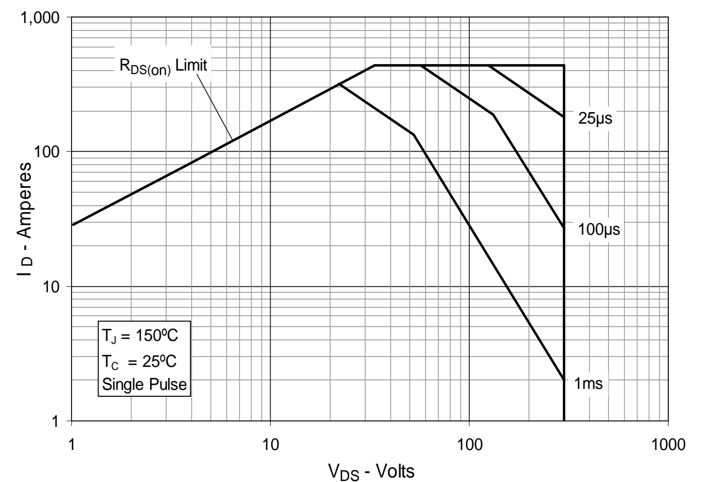

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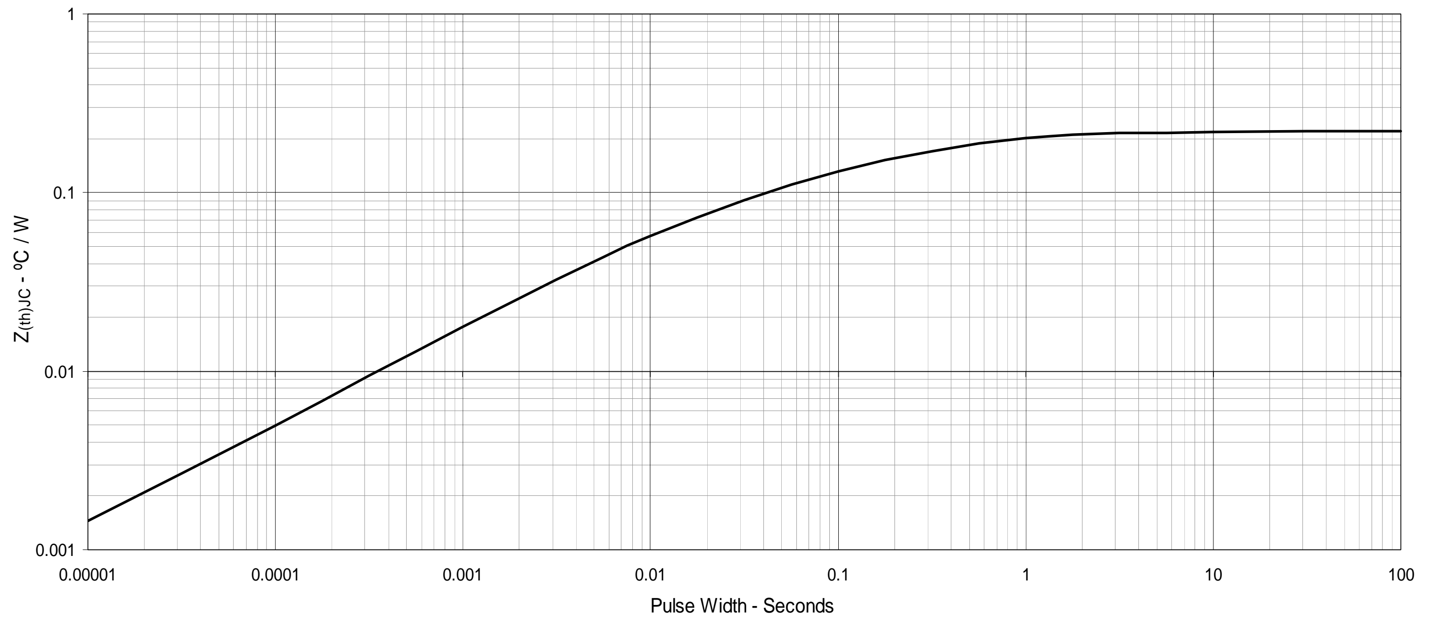

Fig. 13. Maximum Transient Thermal Impedance

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