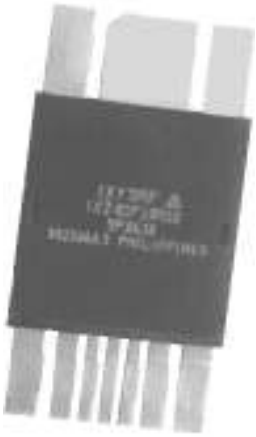
IXYS RF

# IXZ4DF18N50
## RF Power MOSFET & DRIVER

**Driver / MOSFET Combination**
**DEIC-515 Driver combined with IXZ318N50 MOSFET**
**Gate driver matched to MOSFET**

**500 Volts**
**19 A**
**0.29 Ohms**



### Features

- Isolated substrate
  - high isolation voltage (>2500V)
  - excellent thermal transfer
  - Increased temperature and power cycling capability
- IXYS advanced Z-MOS process
- Low $R_{ds(ON)}$
- Very low insertion inductance(<2nH)
- No beryllium oxide (BeO) or other hazardous materials
- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-up protected
- Low quiescent supply current

### Advantages

- Optimized for RF and high speed
- Easy to mount—no insulators needed
- High power density
- Single package reduces size and heat sink area

### Applications

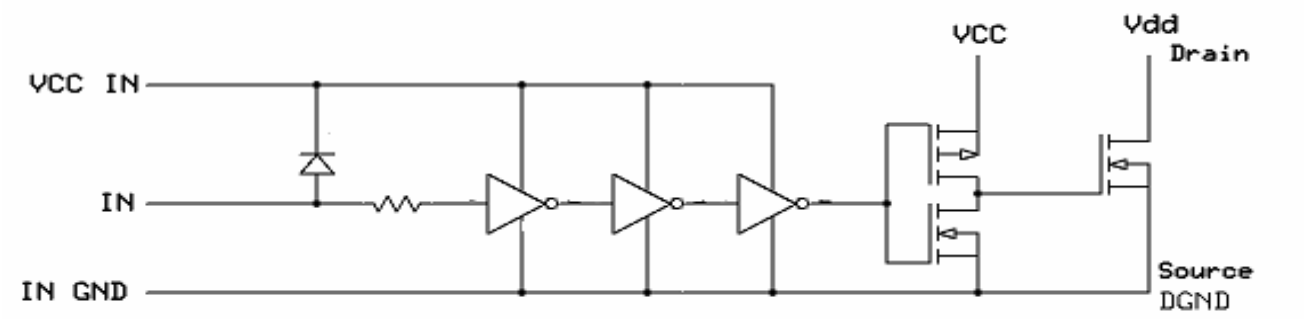
- Class D or E Switching Amplifier
- Multi MHz Switch Mode Power Supplies (SMPS)

### Description

The IXZ4DF18N50 is a CMOS high speed high current gate driver and ZMOS MOSFET combination specifically designed Class D and E HF RF applications at up to 40MHz, as well as other applications. The IXZ4DF18N50 in pulse mode can provide 95A of peak current while producing voltage rise and fall times of less than 4ns, and minimum pulse widths of 8ns. The input of the driver is fully immune to latch up over the entire operating range. Designed with small internal delays, the IXZ4DF18N50 is suitable for higher power operation where combiners are used. Its features and wide safety margin in operating voltage and power make the IXZ4DF18N50 unmatched in performance and value.

The IXZ4DF18N50 is packaged in DEI's low inductance RF package incorporating DEI's RF layout techniques to minimize stray lead inductances for optimum switching performance. The IXZ4DF18N50 is a surface-mountable device.

**Figure 1.**
**Functional Diagram**

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## Device Specifications

| Parameter | Value |
|---|---|
| Maximum Junction Temperature | 150°C |
| Operating Temperature Range | - 40°C to 85°C |
| Weight | 5.5g |

| Symbol | Test Conditions | Maximum Ratings |
|---|---|---|
| $f_{MAX}$ | $I_D = 0.5I_{DM25}$ | 40MHz |
| $V_{DSS}$ | | 500V |
| $V_{CC}$, $V_{CCIN}$ | | 20V |
| $I_{DSS}$ | $V_{DS} = 0.8V_{DSS}$ $T_J = 25C$<br>$V_{GS} = 0V$ $T_J = 125C$ | 50uA<br>1mA |
| $I_{DM25}$ | $T_C$ = 25°C | 19A |
| $I_{DM}$ | $T_C$ = 25°C, Pulse limited by $T_{JM}$ | 95A |
| $I_{AR}$ | $T_C$ = 25°C | 19A |
| $P_T$ (MOSFET and Driver) | $T_C$ = 25°C | 500 W |
| $R_{thJC}$ | | 0.25 °C/W |
| $R_{thJHS}$ | | TBD °C/W |

## Device Performance

| Symbol | Test Condition | Minimum | Typical | Maximum |
|---|---|---|---|---|
| $R_{ds(ON)}$ | $V_{CC}$ = 15 V, $I_D = 0.5I_{DM25}$<br>Pulse Test, t ≤ 300µS, Duty Cycle ≤ 2% | | 0.29 Ω | |
| $V_{CC}$, $V_{CCIN}$ | | 8V | 15V | 20V |
| IN (Signal Input) | | - 5V | | $V_{CCIN}$+0.3V |
| $V_{IH}$ (High Input Voltage) | | $V_{CCIN}$ -2V | | $V_{CCIN}$+0.3V |
| $V_{IL}$ (Low Input Voltage) | | | 0.8V | |
| $Z_{IN}$ | f = 1MHz | | 7960 Ω | |
| $C_{stray}$ | f = 1MHz Any one pin to the back plane metal | | 46pf | |
| $C_{OSS}$ | $V_{GS}$ = 0V, $V_{DS} = 0.8V_{DSS}$(max) , f =1MHz | | 139pf | |
| $t_{ONDLY}$ | $T_C$ = 25°C<br>$V_{CC}$, $V_{CCIN}$, $V_{IN}$ = 15V, 1µS Pulse,<br>$V_{DS}$ = 50V, $R_L$ = 5.0Ω | | 17 nS | |
| $t_{OFFDLY}$ | | | 26 nS | |
| $t_R$ | $T_C$ = 25°C<br>$V_{CC}$, $V_{CCIN}$, $V_{IN}$ = 15V,1µS Pulse,<br>$V_{DS}$ = 50V, $R_L$ = 5.0Ω | | 3 nS | |
| $t_F$ | | | 3 nS | |

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Fig. 2

Extended Output Characteristics @ 25°C

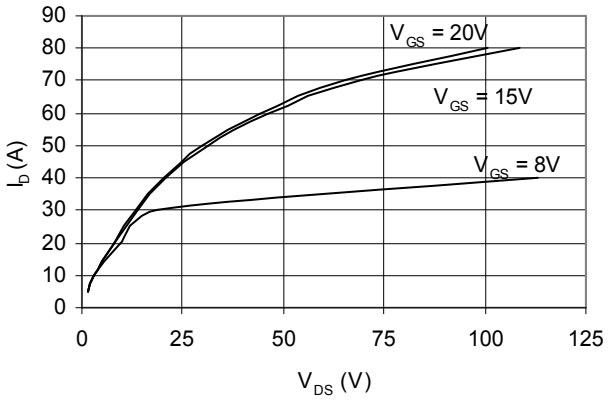


Fig. 3

$R_{DS(ON)}$ vs. Temperature
$I_D$ = 0.5 $I_{DM}$

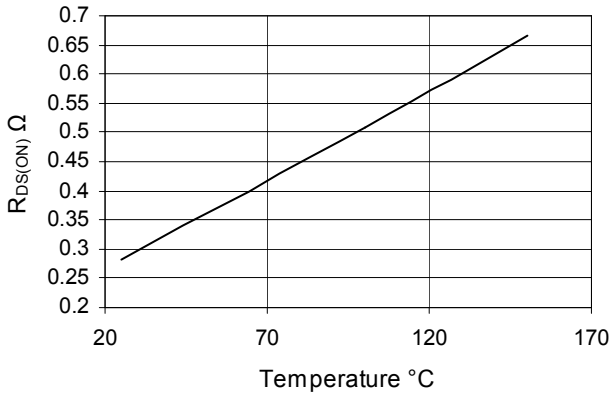


Fig. 4

Propagation Delay ON vs. Supply Voltage
$I_D$ = 0.5 $I_{DM}$

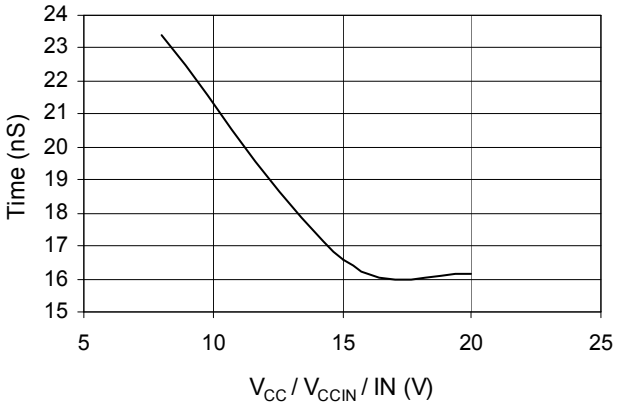


Fig. 5

Propagation Delay OFF vs. Supply Voltage
$I_D$= 0.5 $I_{DM}$

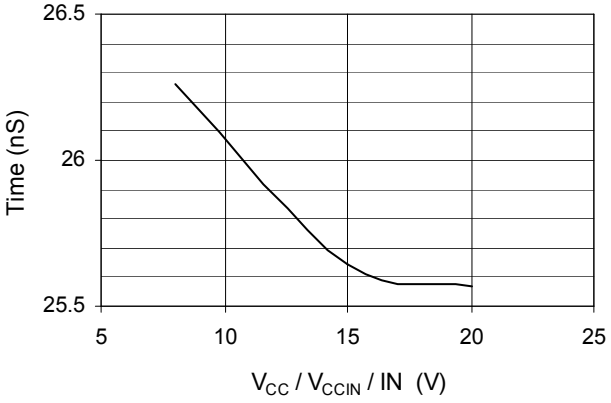


Fig. 6

Propagation Delay ON vs. Temperature
$I_D$= 0.5 $I_{DM}$, $V_{CC}$ / $V_{CCIN}$ / IN = 15V

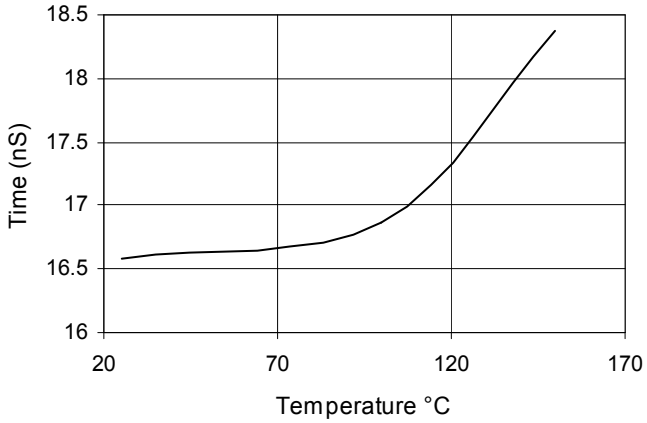


Fig. 7

Propagation Delay OFF vs. Temperature
$I_D$ = 0.5 $I_{DM}$, $V_{CC}$ / $V_{CCIN}$ / IN =15V

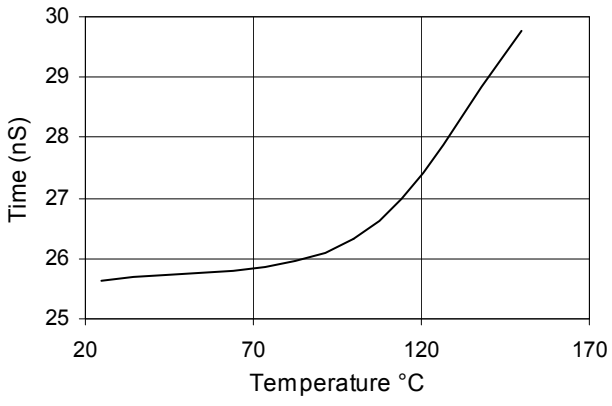


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Fig. 8

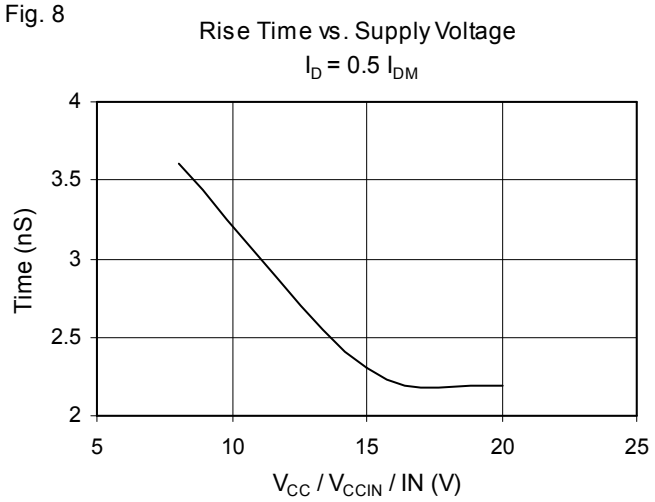


Fig. 9

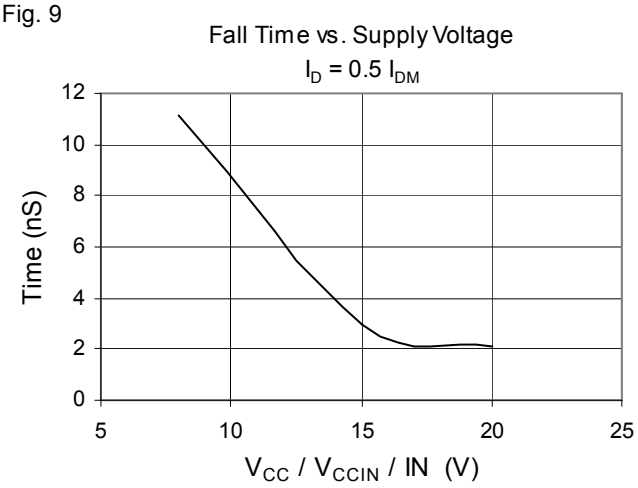


Fig. 10

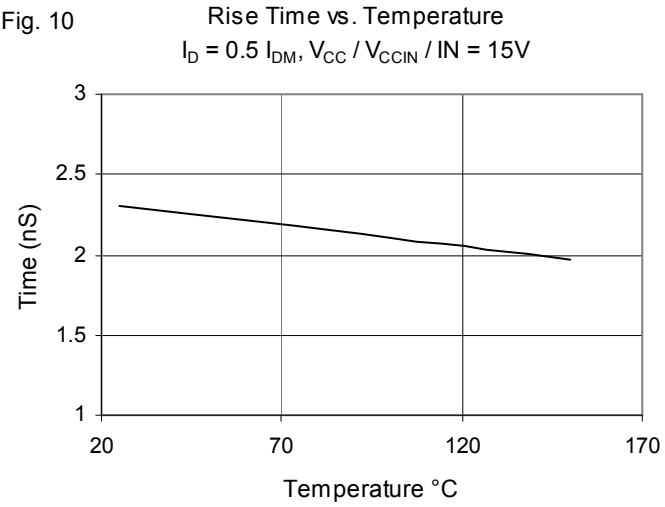


Fig. 11

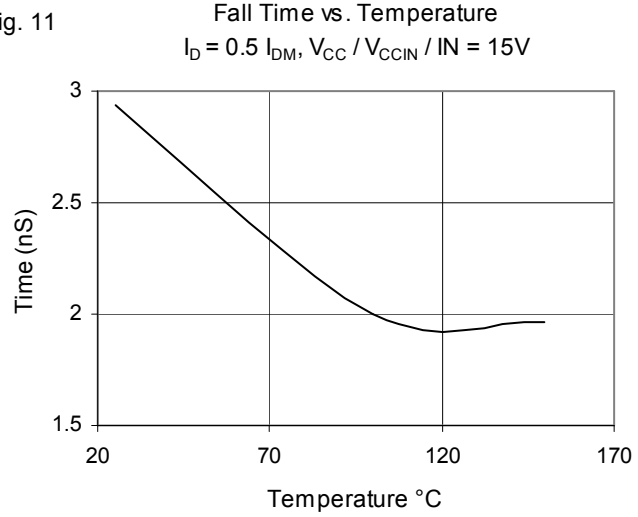


Fig. 12

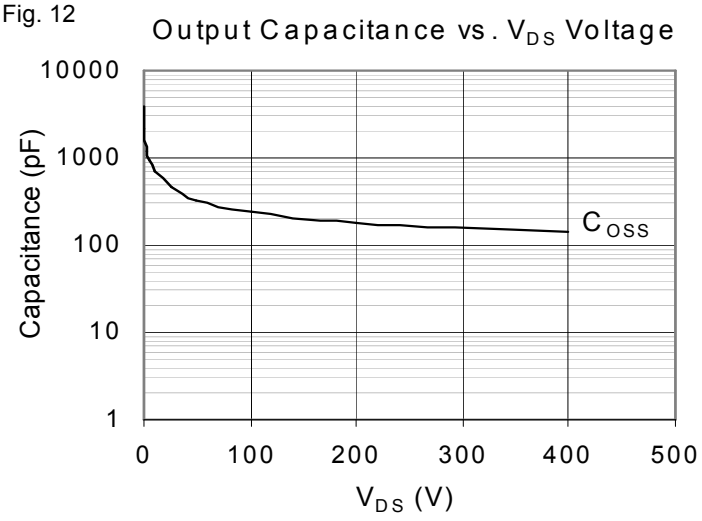


Fig. 13

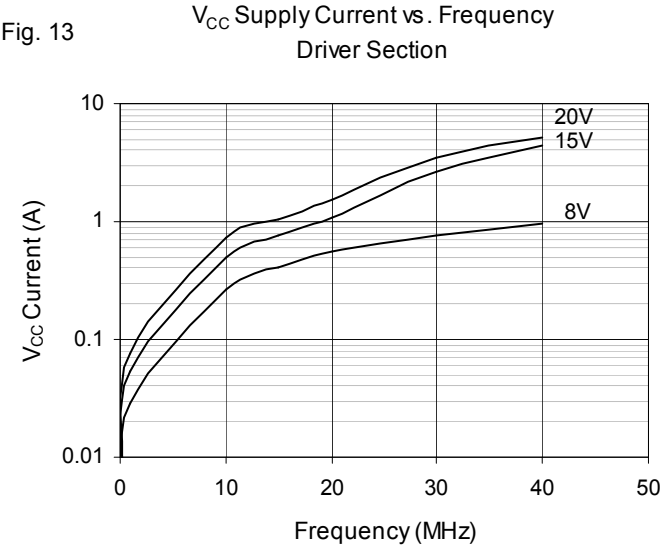


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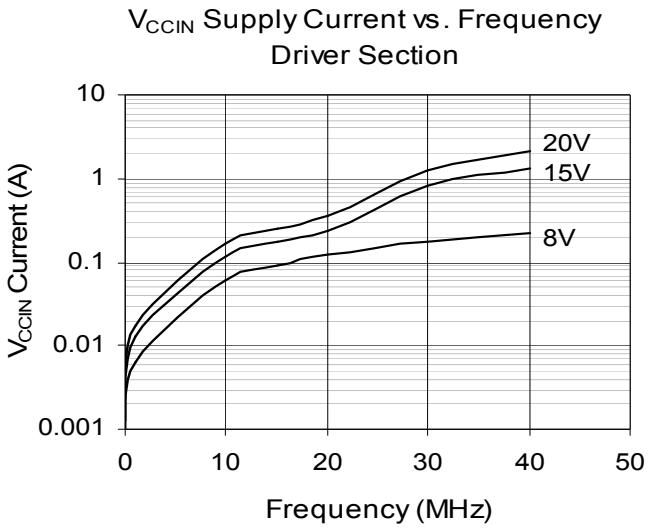
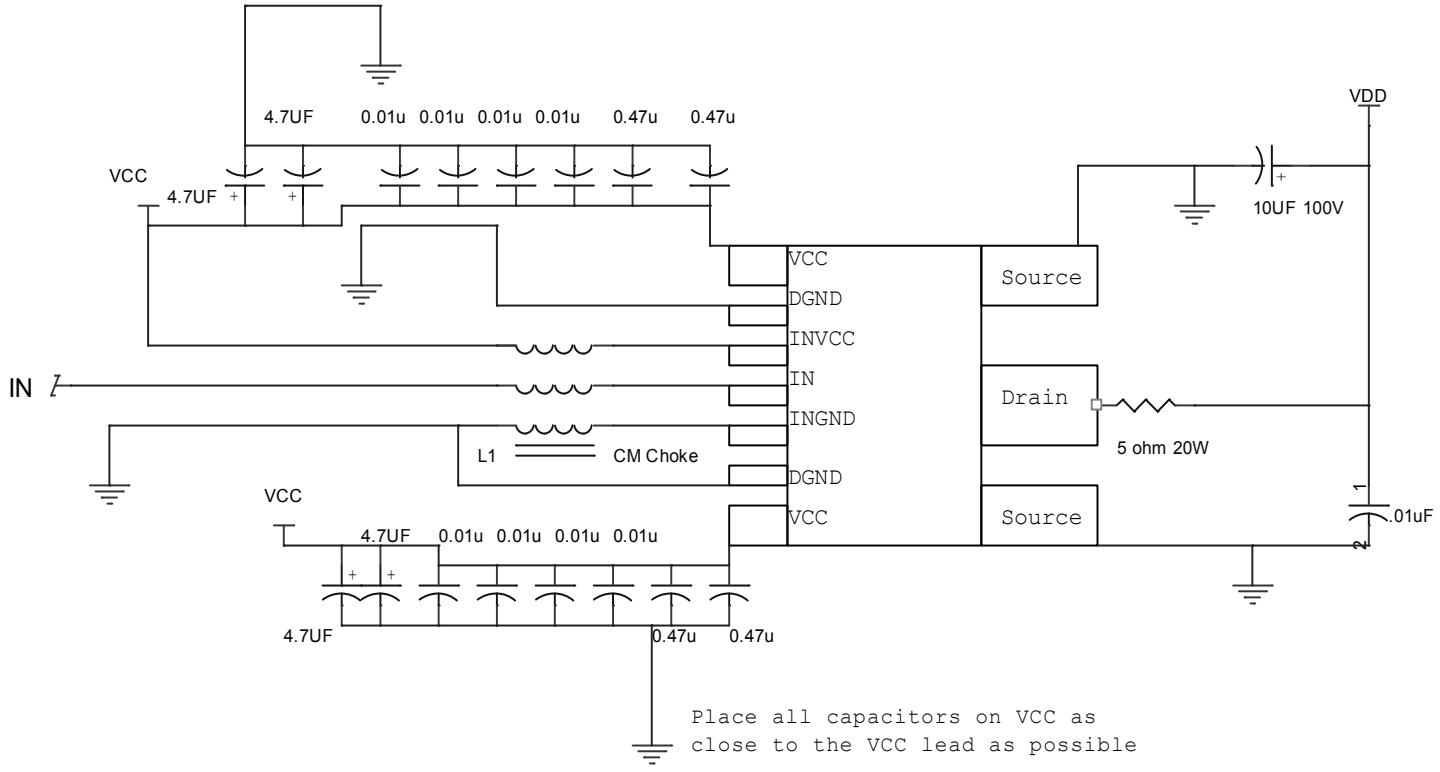
Fig. 14




# Test Circuit

Fig. 15

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## Lead Description

| SYMBOL | FUNCTION | DESCRIPTION |
|---|---|---|
| Drain | MOSFET Drain | Drain of Power MOSFET. |
| Source | MOSFET Source | Source of Power MOSFET. This connection is common to DGND. |
| VCC | Driver Section Supply Voltage | Power supply input for the driver output section. These leads provide power to the output section of the DEIC515 driver. Both leads must be connected. |
| VCCIN | Input Section Supply Voltage | Input for the positive input section power-supply voltage. This lead provide power to the input section of the DEIC515 driver. This lead should not be directly connected to VCC. |
| IN | Input | Input signal. |
| DGND | Power Driver Ground | The system ground leads. Internally connected to all circuitry, these leads provide ground reference for the entire chip. These leads should be connected to a low noise analog ground plane for optimum performance. |
| INGND | Input Section Ground | The input section ground lead. This lead is a Kelvin connection internally connected to DGND. This lead must not be connected to DGND as excessive current can damage this lead. |



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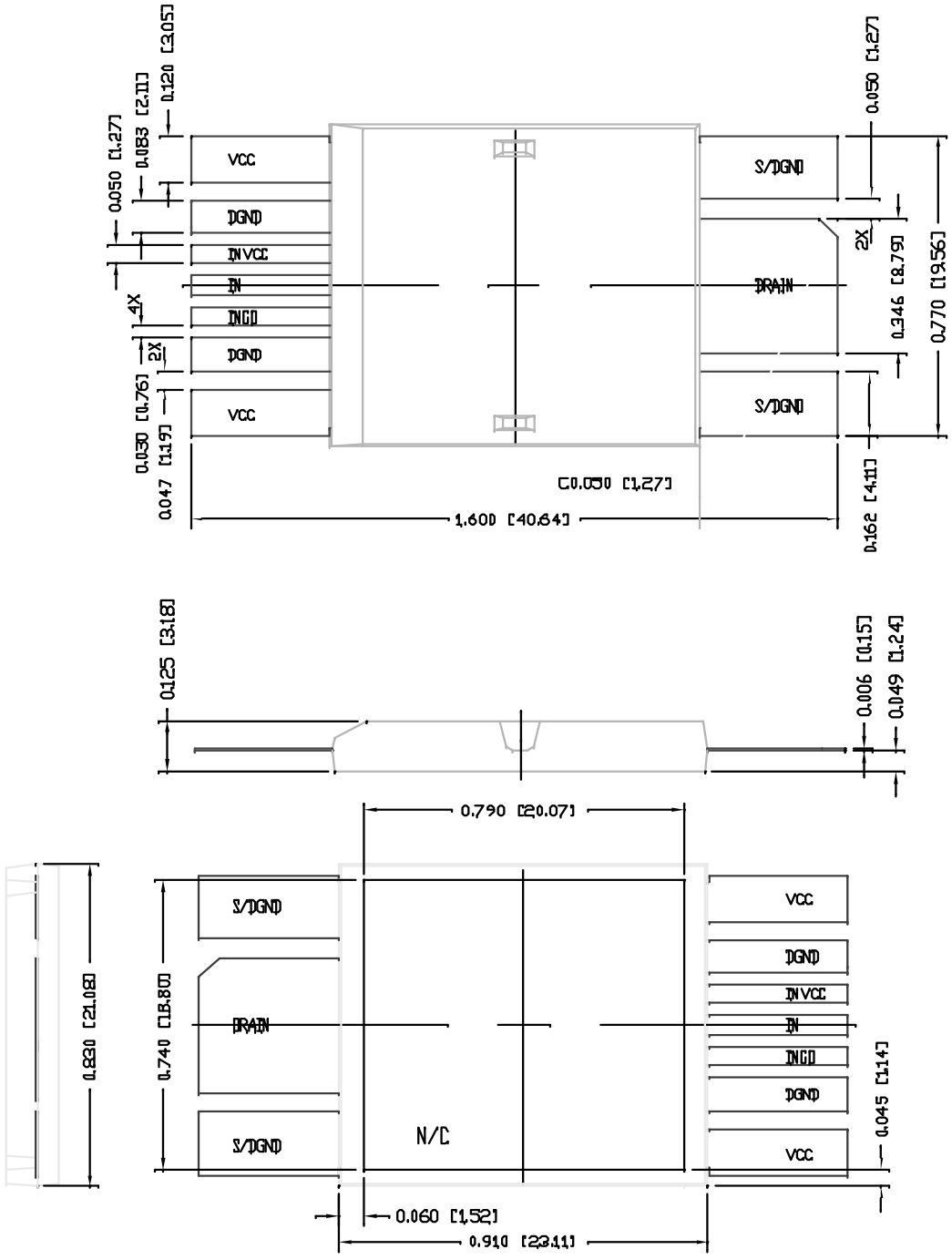
**Fig. 16 IXZ4DF18N50 Package Outline**

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