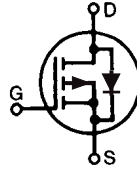


TrenchP™
Power MOSFETs
IXTT68P20T
IXTH68P20T

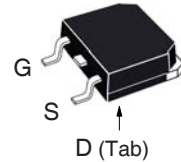
$$V_{DSS} = -200V$$

$$I_{D25} = -68A$$

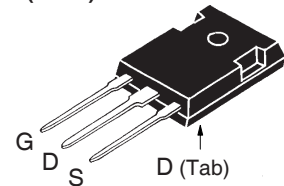
$$R_{DS(on)} \leq 55m\Omega$$

 P-Channel Enhancement Mode
 Avalanche Rated


TO-268 (IXTT)



TO-247 (IXTH)


 G = Gate D = Drain
 S = Source Tab = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $150^\circ C$	- 200	V
V_{DGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GS} = 1M\Omega$	- 200	V
V_{GSS}	Continuous	± 15	V
V_{GSM}	Transient	± 25	V
I_{D25}	$T_C = 25^\circ C$	- 68	A
I_{DM}	$T_C = 25^\circ C$, Pulse Width Limited by T_{JM}	- 200	A
I_A	$T_C = 25^\circ C$	- 68	A
E_{AS}	$T_C = 25^\circ C$	2.5	J
dv/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ C$	10	V/ns
P_D	$T_C = 25^\circ C$	568	W
T_J		- 55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		- 55 ... +150	$^\circ C$
T_L	1.6mm (0.062 in.) from Case for 10s	300	$^\circ C$
T_{SOLD}	Plastic Body for 10s	260	$^\circ C$
M_d	Mounting Torque (TO-247)	1.13 / 10	Nm/lb.in.
Weight	TO-268	4	g
	TO-247	6	g

Features

- International Standard Packages
- Avalanche Rated
- Extended FBSOA
- Fast Intrinsic Diode
- Low $R_{DS(ON)}$ and Q_G

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- High-Side Switching
- Push Pull Amplifiers
- DC Choppers
- Automatic Test Equipment
- Current Regulators
- Battery Charger Applications

Symbol	Test Conditions ($T_J = 25^\circ C$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = -250\mu A$	- 200		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\mu A$	- 2.0		V
I_{GSS}	$V_{GS} = \pm 15V$, $V_{DS} = 0V$			± 100 nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 125^\circ C$			- 10 μA - 200 μA
$R_{DS(on)}$	$V_{GS} = -10V$, $I_D = 0.5 \cdot I_{D25}$, Note 1			55 m Ω

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = -10\text{V}$, $I_D = 0.5 \cdot I_{D25}$, Note 1	55	90	S
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = -25\text{V}$, $f = 1\text{MHz}$		33.4	nF
C_{oss}			1300	pF
C_{rss}			307	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = -10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$ $R_G = 1\Omega$ (External)		63	ns
t_r			29	ns
$t_{d(off)}$			115	ns
t_f			18	ns
$Q_{g(on)}$	$V_{GS} = -10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$		380	nC
Q_{gs}			125	nC
Q_{gd}			70	nC
R_{thJC}				0.22°C/W
R_{thCS}	TO-247	0.21		$^\circ\text{C/W}$

Source-Drain Diode

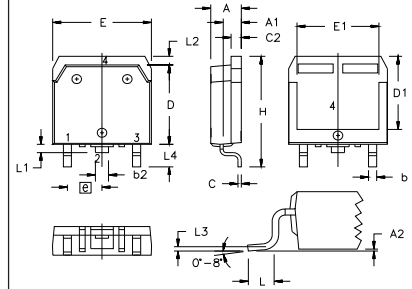
Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			- 68 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			- 270 A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{V}$, Note 1			-1.4 V
t_{rr}	$I_F = -34\text{A}$, $-di/dt = -100\text{A}/\mu\text{s}$ $V_R = -100\text{V}$, $V_{GS} = 0\text{V}$		245	ns
Q_{RM}			2.6	μC
I_{RM}			- 21.4	A

Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

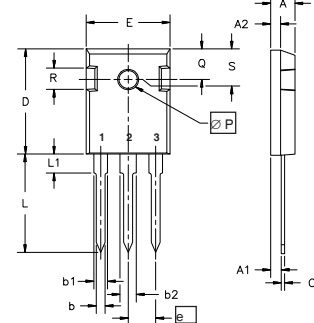
TO-268 Outline



Terminals: 1 - Gate, 2,4 - Drain, 3 - Source

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
A2	.001	.010	0.02	0.25
b	.045	.057	1.15	1.45
b2	.075	.083	1.90	2.10
C	.016	.026	0.40	0.65
C2	.057	.063	1.45	1.60
D	.543	.551	13.80	14.00
D1	.488	.500	12.40	12.70
E	.624	.632	15.85	16.05
E1	.524	.535	13.30	13.60
e	.215 BSC		5.45 BSC	
H	.736	.752	18.70	19.10
L	.094	.106	2.40	2.70
L1	.047	.055	1.20	1.40
L2	.039	.045	1.00	1.15
L3	.010 BSC		0.25 BSC	
L4	.150	.161	3.80	4.10

TO-247 Outline



Terminals: 1 - Gate, 2 - Drain, 3 - Source

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.7	5.3	.185	.209
A ₁	2.2	2.54	.087	.102
A ₂	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b ₁	1.65	2.13	.065	.084
b ₂	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
∅P	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S		6.15 BSC		242 BSC

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

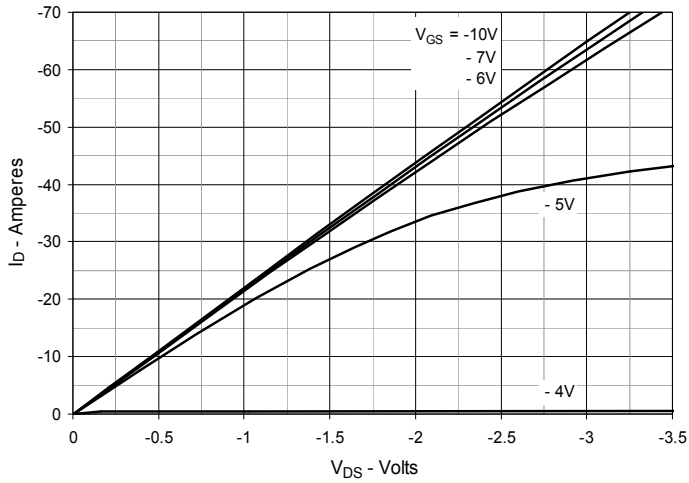


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

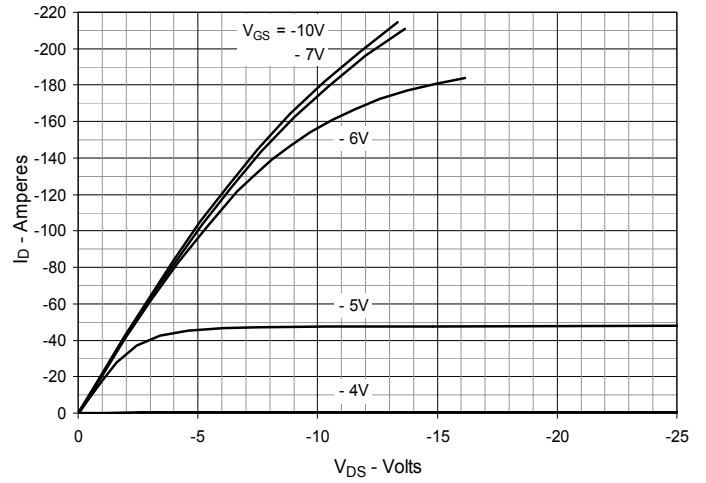


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

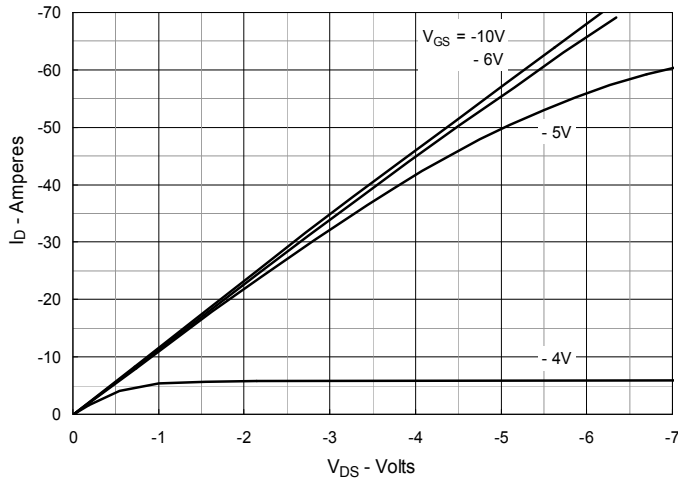


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = -34\text{A}$ vs. Junction Temperature

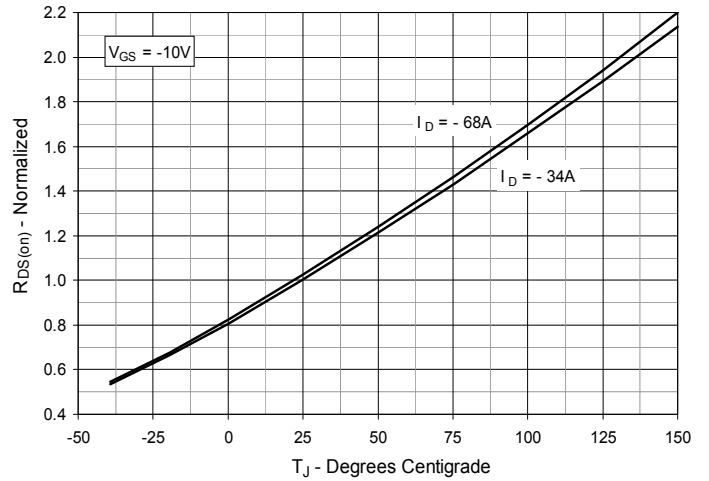


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = -34\text{A}$ vs. Drain Current

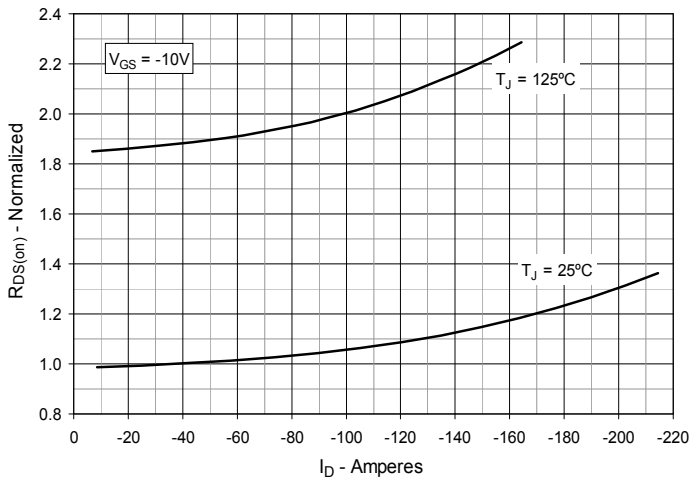


Fig. 6. Maximum Drain Current vs. Case Temperature

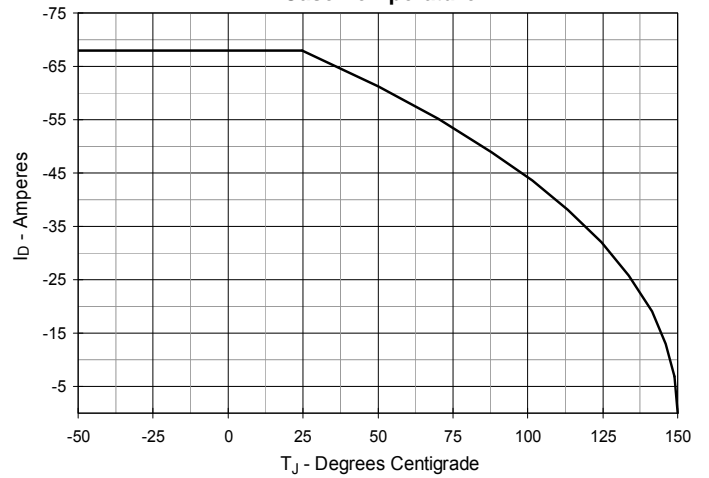


Fig. 7. Input Admittance

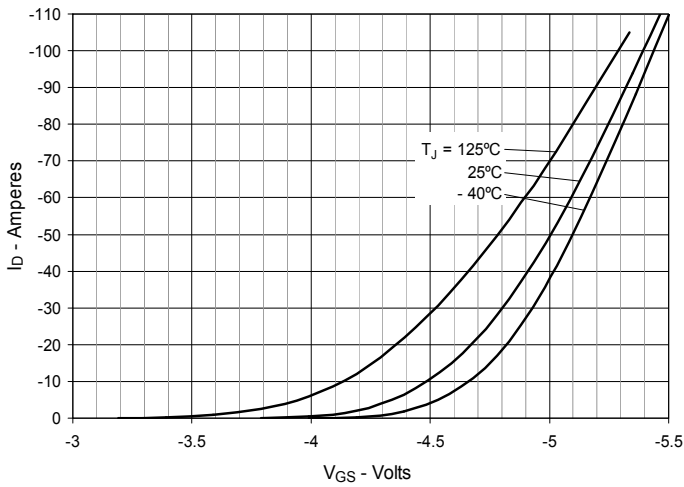


Fig. 8. Transconductance

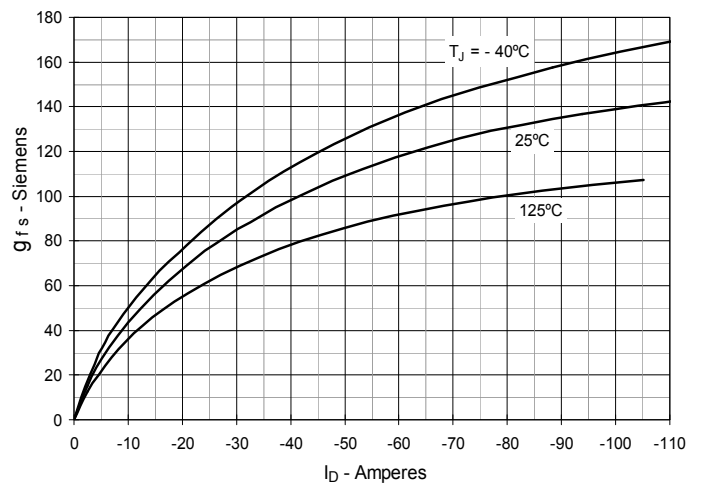


Fig. 9. Forward Voltage Drop of Intrinsic Diode

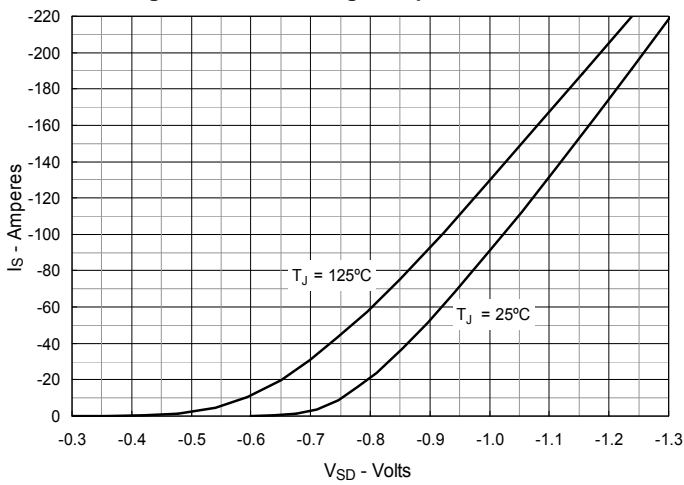


Fig. 10. Gate Charge

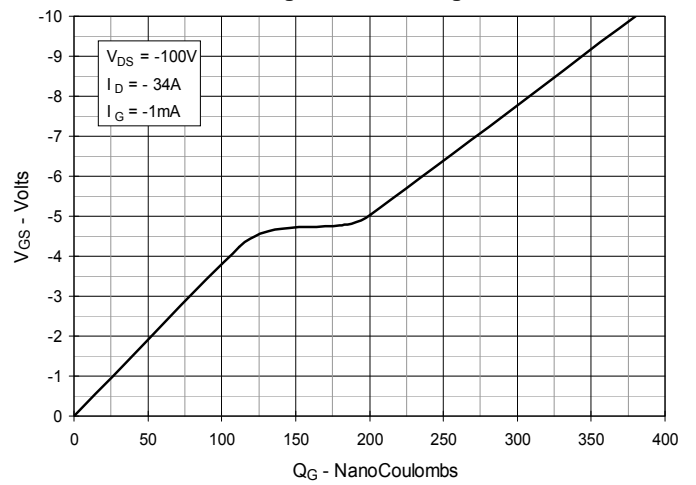


Fig. 11. Capacitance

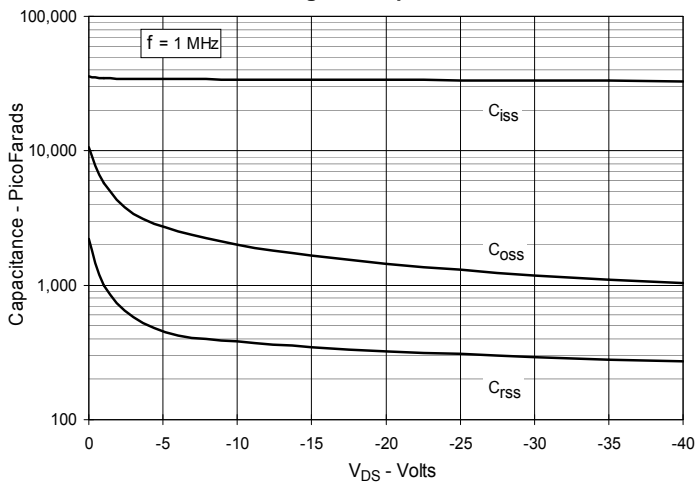


Fig. 12. Forward-Bias Safe Operating Area

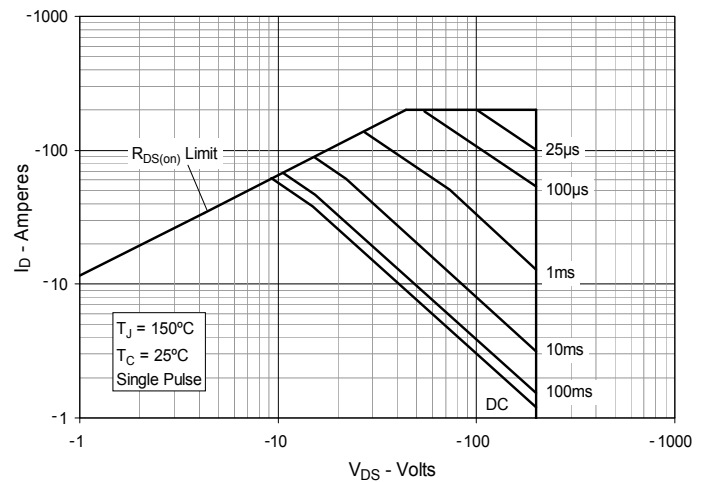


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

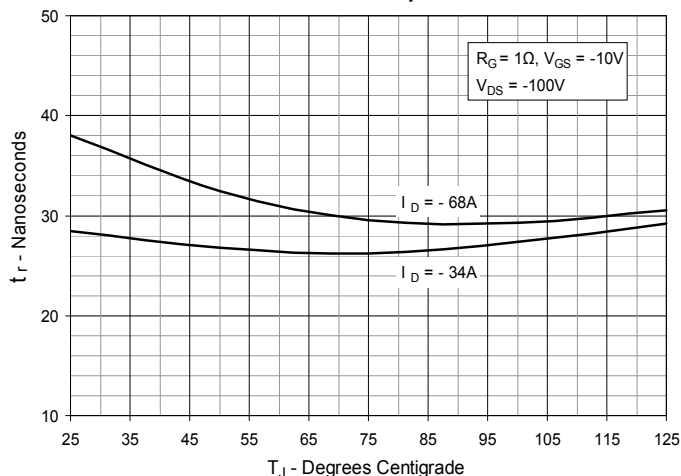


Fig. 14. Resistive Turn-on Rise Time vs. Drain Current

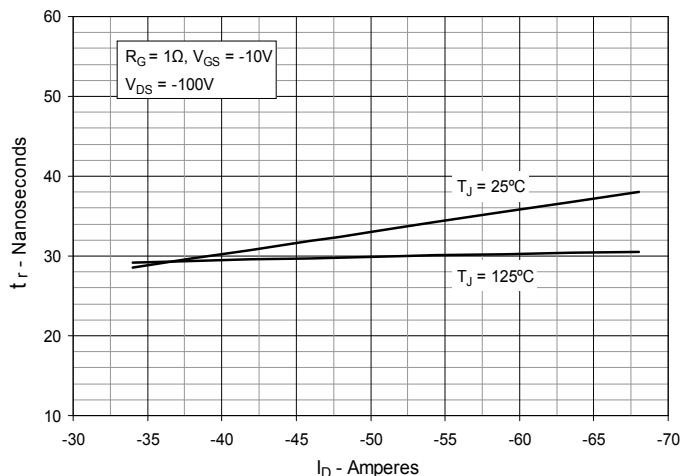


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

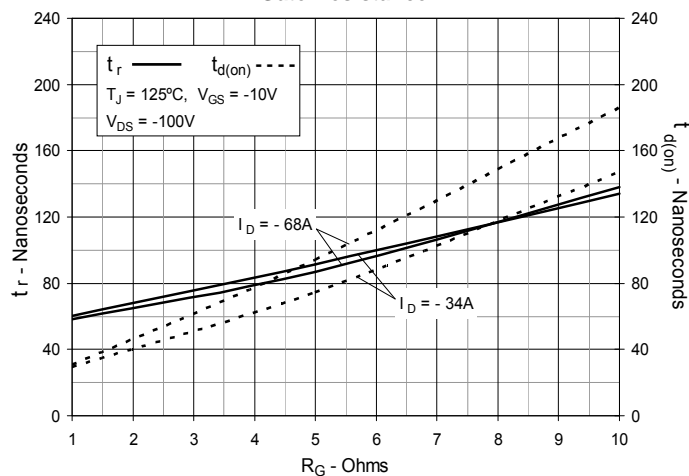


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

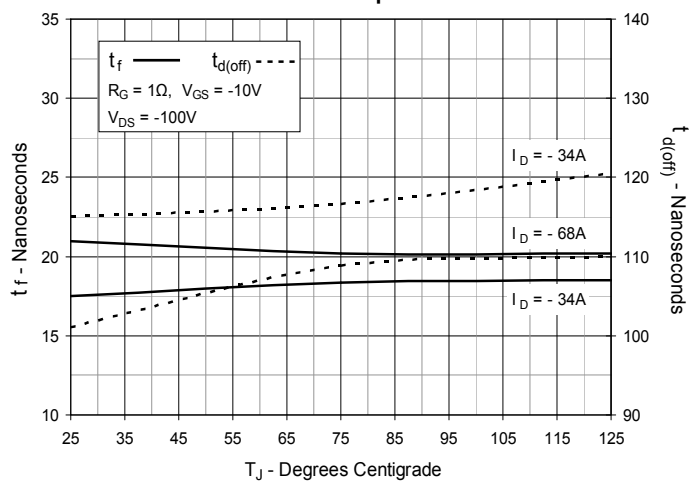


Fig. 17. Resistive Turn-off Switching Times vs. Drain Current

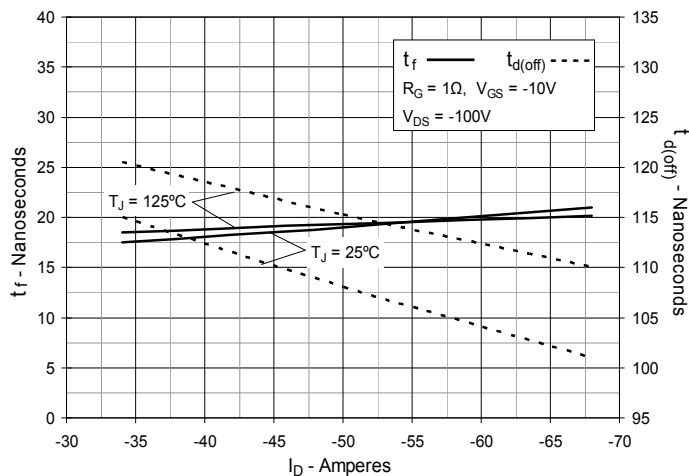


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance

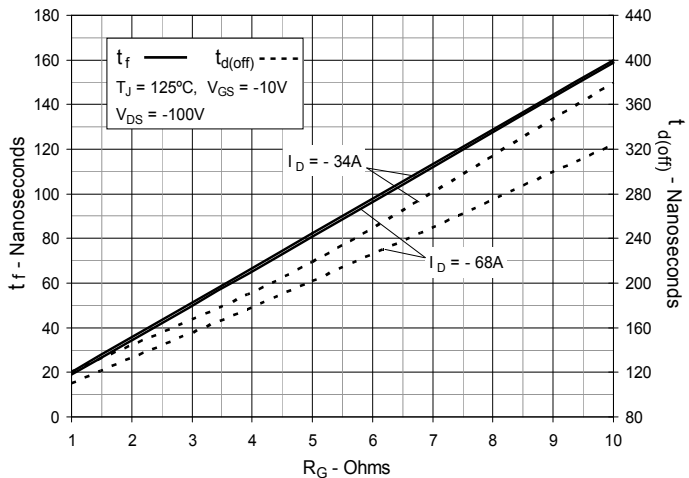


Fig. 19. Maximum Transient Thermal Impedance

