

### General Description

This planar stripe MOSFET has better characteristics, such as fast switching time, low on resistance, low gate charge and excellent avalanche characteristics. It is mainly suitable for electronic ballast and switching mode power supplies.

### FEATURES

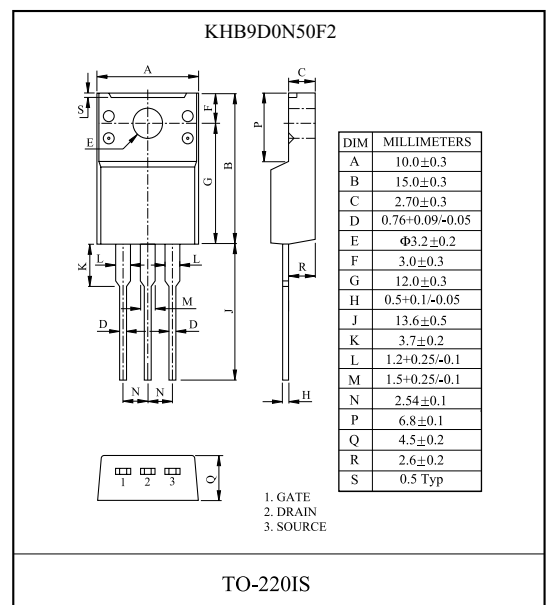
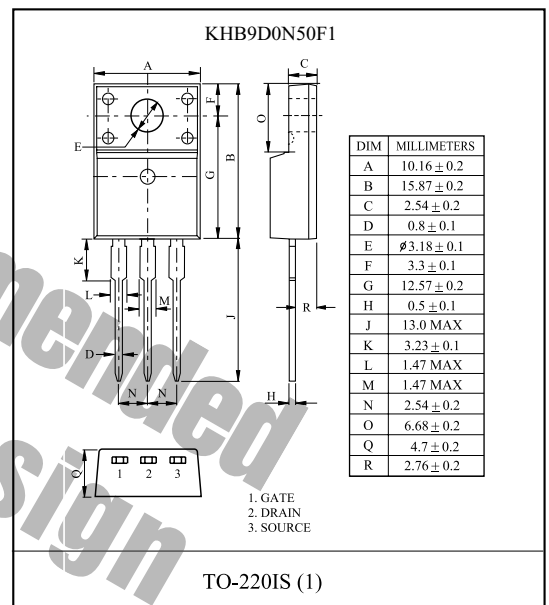
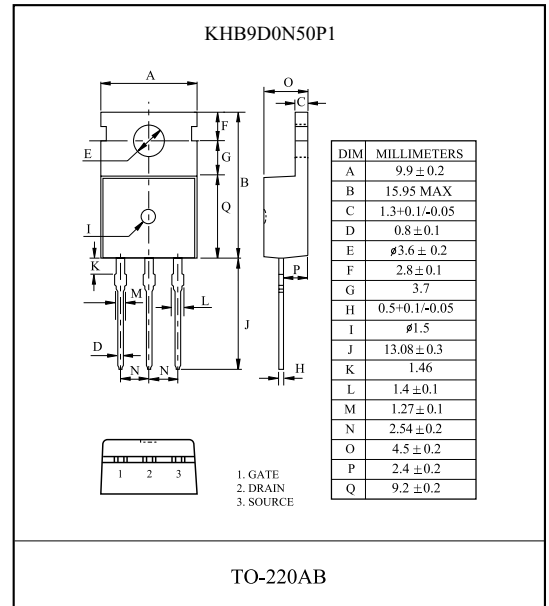
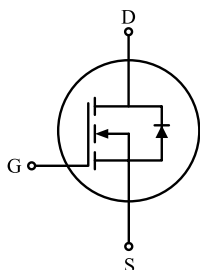
- $V_{DSS(Min.)} = 500V$ ,  $I_D = 9A$
- Drain-Source ON Resistance :  
 $R_{DS(ON)} = 0.8$  @  $V_{GS} = 10V$
- $Q_g(typ.) = 34.6nC$

### MAXIMUM RATING (Tc=25 °C)

CHARACTERISTIC	SYMBOL	RATING		UNIT
		KHB9D0N50P1	KHB9D0N50F1 KHB9D0N50F2	
Drain-Source Voltage	$V_{DSS}$	500		V
Gate-Source Voltage	$V_{GSS}$	± 30		V
Drain Current	@Tc=25	9	9*	A
	@Tc=100	5.4	5.4*	
	Pulsed (Note 1)	$I_{DP}$	36	
Single Pulsed Avalanche Energy (Note 2)	$E_{AS}$	360		mJ
Repetitive Avalanche Energy (Note 1)	$E_{AR}$	13.5		mJ
Peak Diode Recovery dv/dt (Note 3)	dv/dt	4.5		V/ns
Drain Power Dissipation	Tc=25	135	44	W
	Derate above 25	$P_D$	1.07	0.35
Maximum Junction Temperature	$T_j$	150		°C
Storage Temperature Range	$T_{stg}$	-55 ~ 150		°C
Thermal Characteristics				
Thermal Resistance, Junction-to-Case	$R_{thJC}$	0.93	2.86	/W
Thermal Resistance, Case-to-Sink	$R_{thCS}$	0.5	-	/W
Thermal Resistance, Junction-to-Ambient	$R_{thJA}$	62.5	62.5	/W

\* : Drain current limited by maximum junction temperature.

### PIN CONNECTION



# KHB9D0N50P1/F1/F2

## ELECTRICAL CHARACTERISTICS (Tc=25 °C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$I_D=250\ \mu A, V_{GS}=0V$	500	-	-	V
Breakdown Voltage Temperature Coefficient	$BV_{DSS}/T_j$	$I_D=250\ \mu A$ , Referenced to 25	-	0.57	-	V/°C
Drain Cut-off Current	$I_{DSS}$	$V_{DS}=500V, V_{GS}=0V$ ,	-	-	10	$\mu A$
Gate Threshold Voltage	$V_{th}$	$V_{DS}=V_{GS}, I_D=250\ \mu A$	2.0	-	4.0	V
Gate Leakage Current	$I_{GSS}$	$V_{GS}=\pm 30V, V_{DS}=0V$	-	-	$\pm 100$	nA
Drain-Source ON Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=4.5A$	-	0.65	0.8	$\Omega$
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=400V, I_D=9A$ $V_{GS}=10V$ (Note4,5)	-	34.6	40	nC
Gate-Source Charge	$Q_{gs}$		-	5.9	-	
Gate-Drain Charge	$Q_{gd}$		-	15.5	-	
Turn-on Delay time	$t_{d(on)}$	$V_{DD}=200V$ $R_L=22\ \Omega$ $R_G=25\ \Omega$ (Note4,5)	-	23	45	ns
Turn-on Rise time	$t_r$		-	65	140	
Turn-off Delay time	$t_{d(off)}$		-	148	241	
Turn-off Fall time	$t_f$		-	81	140	
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V, f=1.0MHz$	-	1389	1805	pF
Reverse Transfer Capacitance	$C_{rss}$		-	19.2	24.9	
Output Capacitance	$C_{oss}$		-	155.7	202	
<b>Source-Drain Diode Ratings</b>						
Continuous Source Current	$I_S$	$V_{GS}<V_{th}$	-	-	9	A
Pulsed Source Current	$I_{SP}$		-	-	36	
Diode Forward Voltage	$V_{SD}$	$I_S=9A, V_{GS}=0V$	-	-	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_S=9A, V_{GS}=0V$ ,	-	357	-	ns
Reverse Recovery Charge	$Q_{rr}$	$dI_S/dt=100A/\mu s$	-	4.87	-	$\mu C$

Note 1) Repetivity rating : Pulse width limited by junction temperature.

Note 2)  $L = 8mH, I_S=9A, V_{DD}=50V, R_G = 25\ \Omega$ , Starting  $T_j = 25\ ^\circ C$ .

Note 3)  $I_S = 9A, dI/dt = 200A/\mu s, V_{DD} = BV_{DSS}$ , Starting  $T_j = 25\ ^\circ C$ .

Note 4) Pulse Test : Pulse width  $300\ \mu s$ , Duty Cycle  $2\%$ .

Note 5) Essentially independent of operating temperature.

Fig1.  $I_D - V_{DS}$

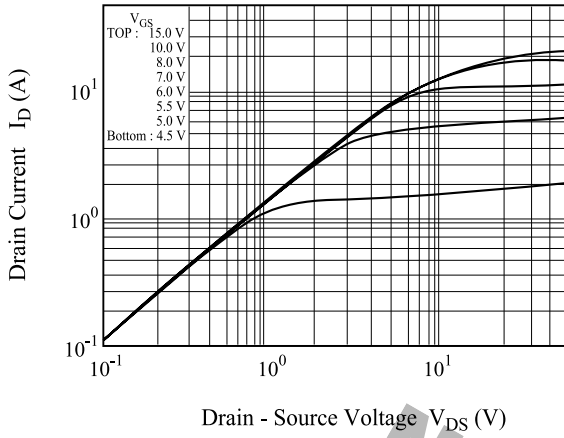


Fig2.  $I_D - V_{GS}$

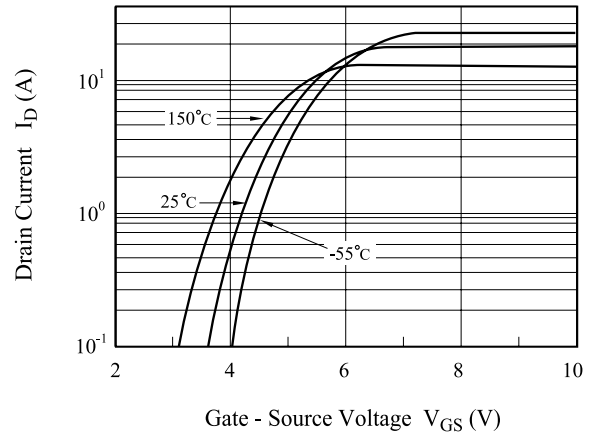


Fig3.  $BV_{DSS} - T_j$

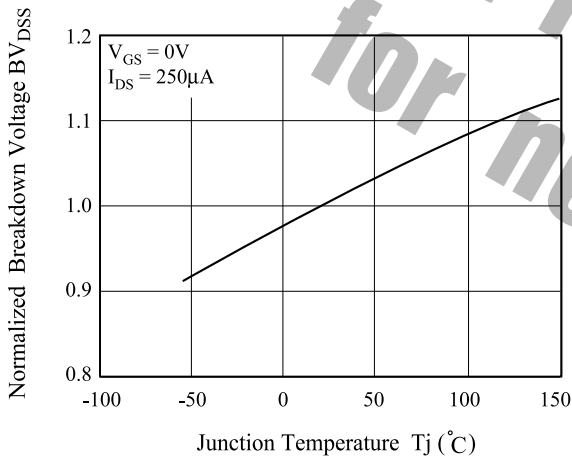


Fig4.  $R_{DS(ON)} - I_D$

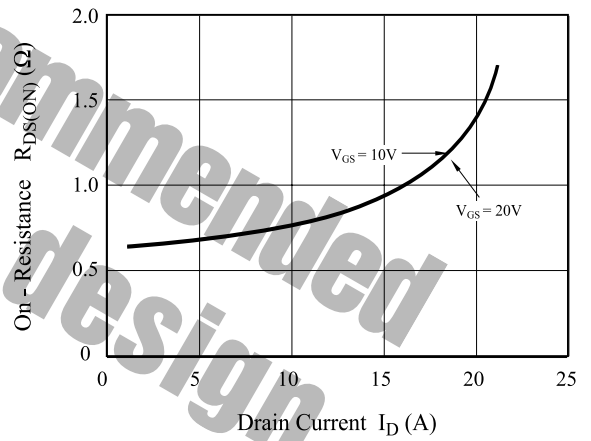


Fig5.  $I_S - V_{SD}$

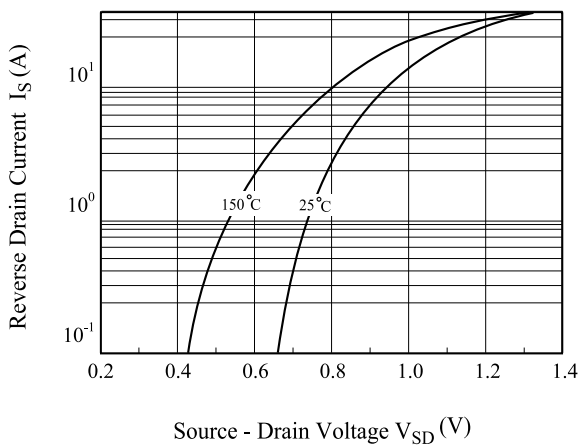
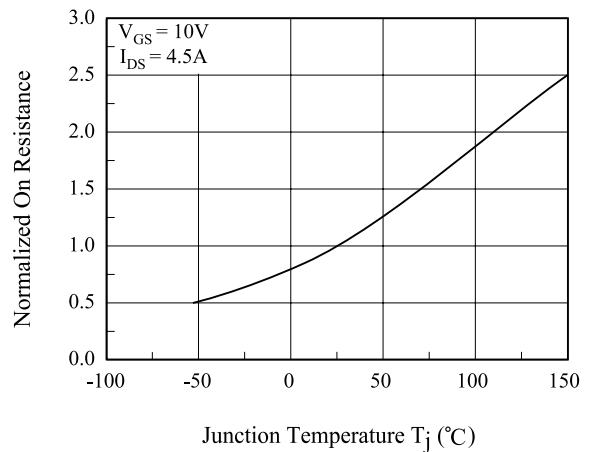
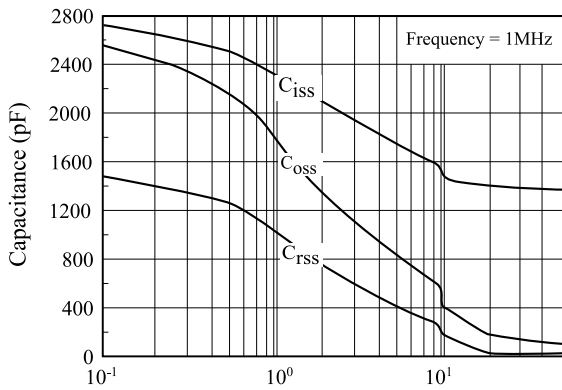


Fig6.  $R_{DS(ON)} - T_j$



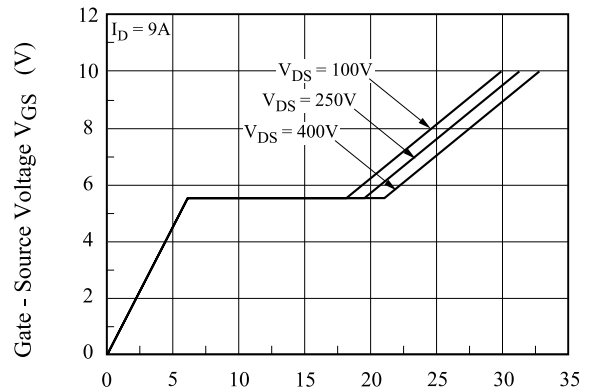
# KHB9D0N50P1/F1/F2

Fig7. C -  $V_{DS}$



Drain - Source Voltage  $V_{DS}$  (V)

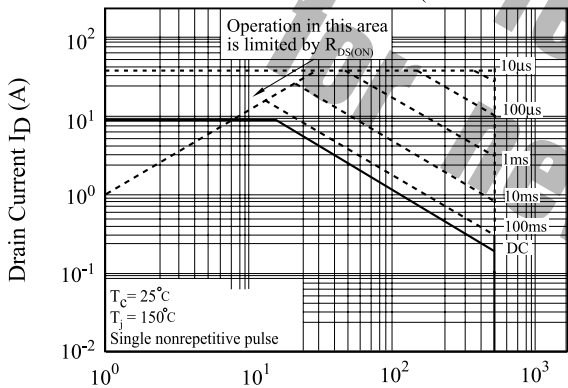
Fig8.  $Q_g$ -  $V_{GS}$



Gate - Charge  $Q_g$  (nC)

Fig9. Safe Operation Area

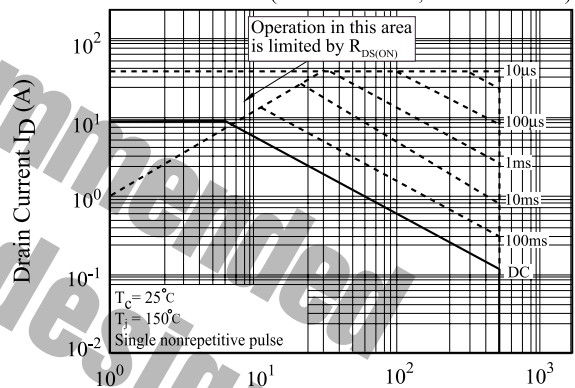
(KHB9D0N50P1)



Drain - Source Voltage  $V_{DS}$  (V)

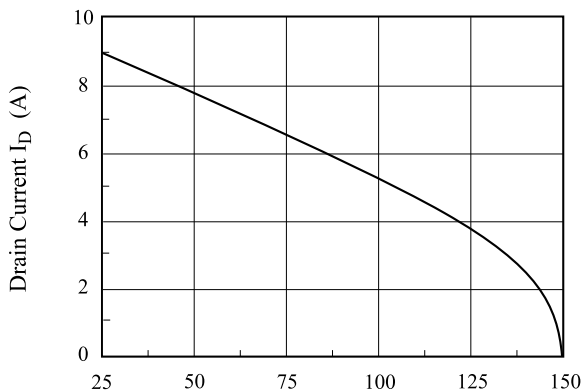
Fig10. Safe Operation Area

(KHB9D0N50F1, KHB9D0N50F2)



Drain - Source Voltage  $V_{DS}$  (V)

Fig11.  $I_D$  -  $T_j$



Junction Temperature  $T_j$  ( $^\circ C$ )

Fig12. Transient Thermal Response Curve

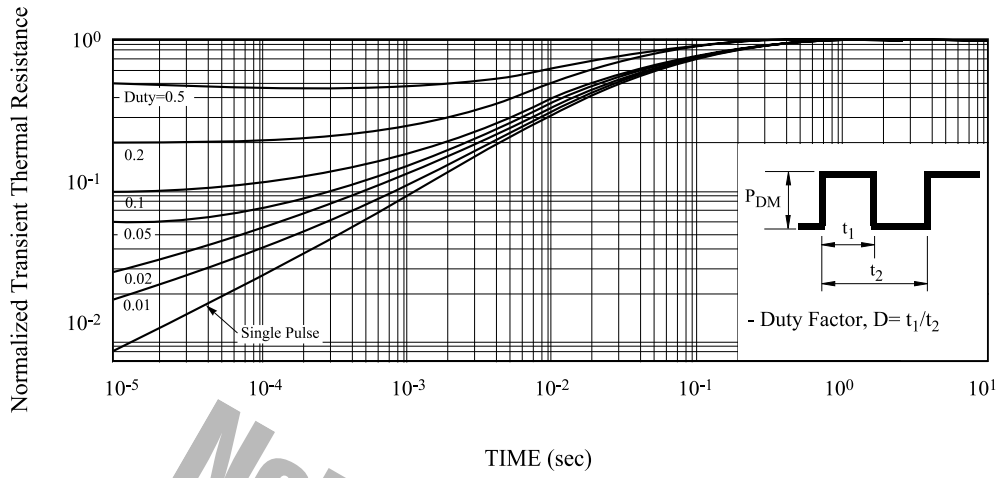


Fig13. Transient Thermal Response Curve

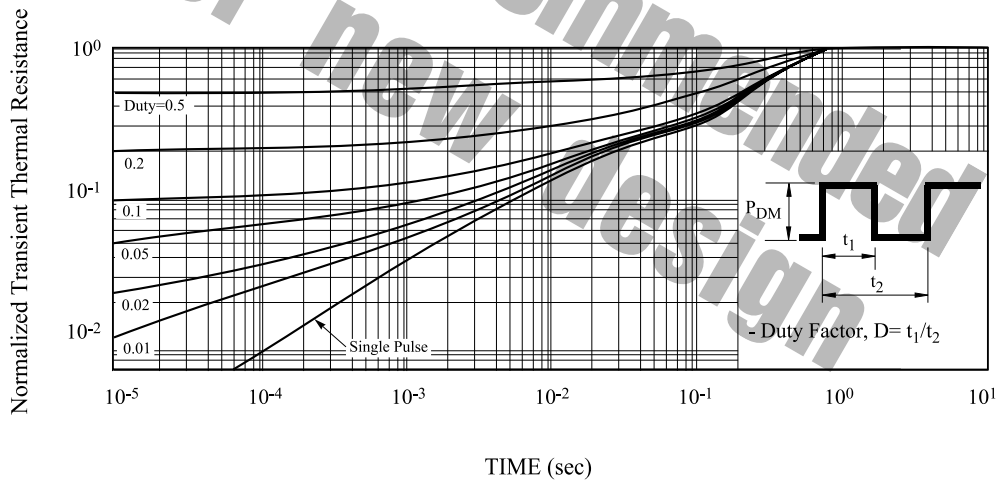


Fig14. Gate Charge

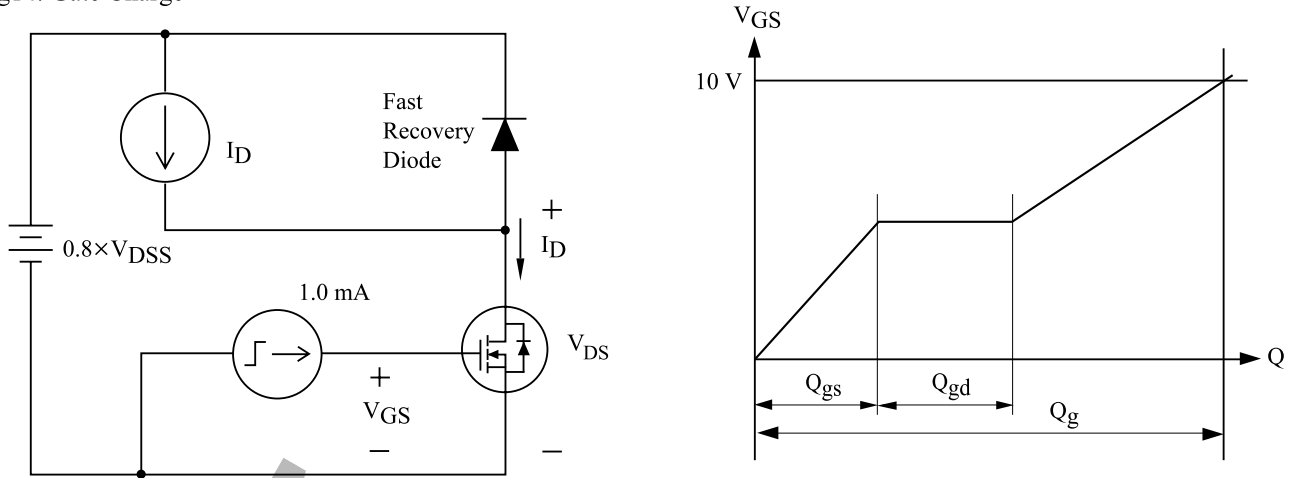


Fig15. Single Pulsed Avalanche Energy

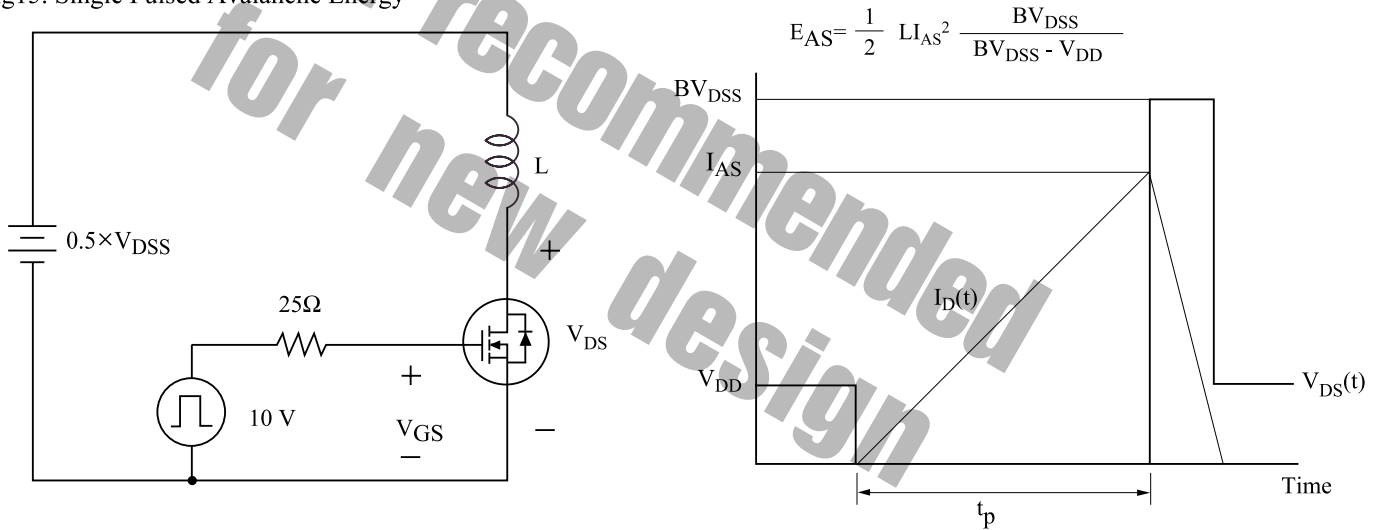


Fig16. Resistive Load Switching

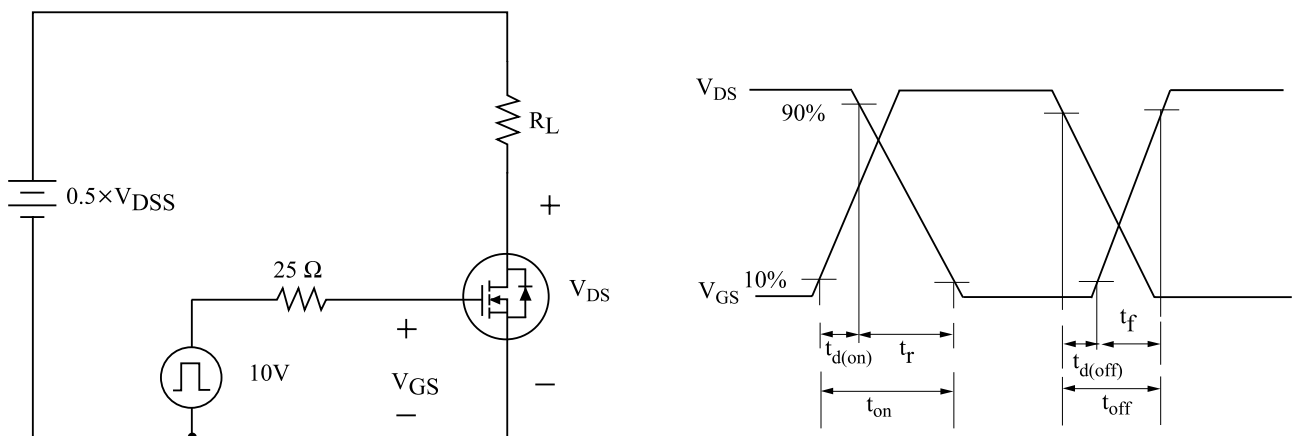
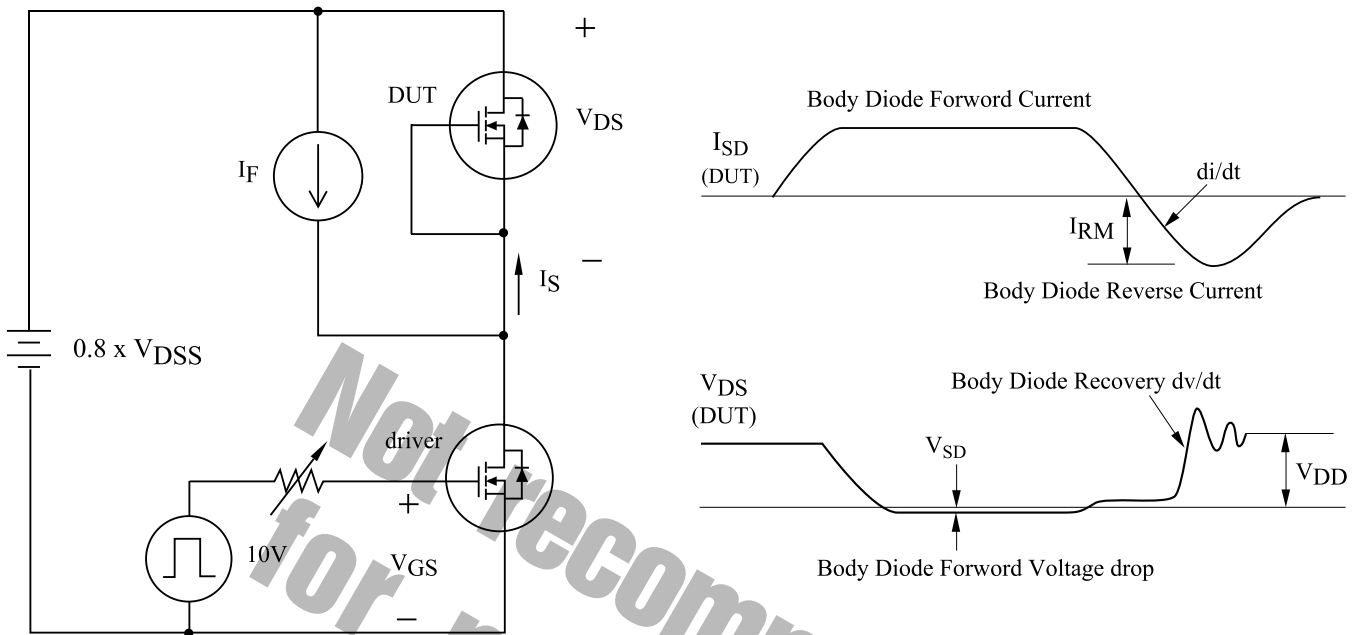


Fig17. Source - Drain Diode Reverse Recovery and  $dv/dt$



Not recommended for new design