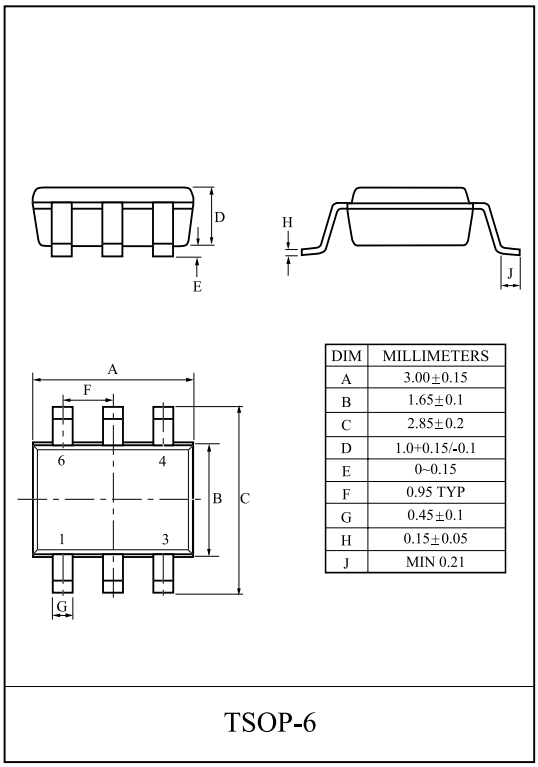
KMA2D8P20X

P-CH Trench MOSFET

General Description

It s mainly suitable for battery pack or power management in cell phone, and PDA.



DIM	MILLIMETERS
A	3.00±0.15
B	1.65±0.1
C	2.85±0.2
D	1.0+0.15/-0.1
E	0~0.15
F	0.95 TYP
G	0.45±0.1
H	0.15±0.05
J	MIN 0.21

TSOP-6

FEATURES

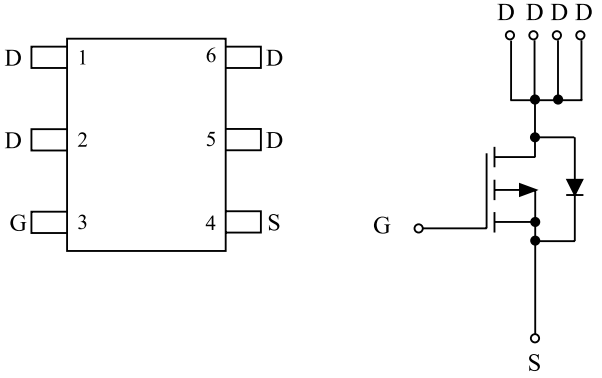
- V_{DSS}=-20V, I_D=-2.8A.
- Drain-Source ON Resistance.
  : $R_{DS(ON)}$=90mΩ(Max.) @ V_{GS}=-4.5V
  : $R_{DS(ON)}$=150mΩ(Max.) @ V_{GS}=-2.5V
- Super High Dense Cell Design for Extremely Low $R_{DS(ON)}$

MAXIMUM RATING (Ta=25℃)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	±12	V
Drain Current	DC	I_D*	-2.8	A
	Pulsed	I_{DP}	-11	
Source-Drain Diode Current		I_S*	-1.25	A
Drain Power Dissipation	Ta=25℃	P_D*	1.25	W
Maximum Junction Temperature		T_j	150	℃
Storage Temperature Range		T_{stg}	-55 150	℃
Thermal Resistance, Junction to Ambient		R_{thJA}*	100	℃/W

* : Surface Mounted on 1 ”×1 ”FR4 Board, t≤5sec.

PIN CONNECTION (TOP VIEW)



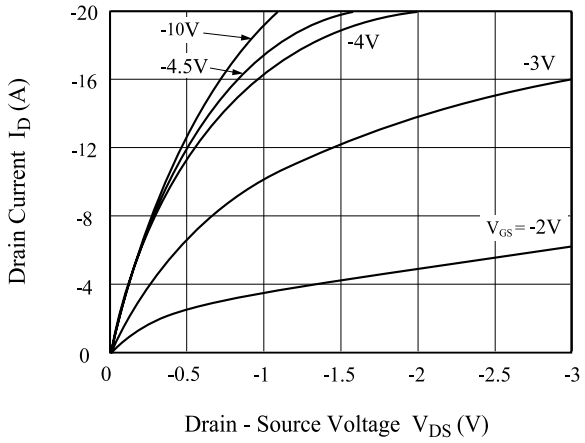
ELECTRICAL CHARACTERISTICS (Ta=25℃)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=-250 μA, V_{GS}=0V	-20	-	-	V
Drain Cut-off Current	I_{DSS}	V_{GS}=0V, V_{DS}=-16V	-	-	-1	μA
Gate Leakage Current	I_{GSS}	V_{GS}=±12V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	V_{th}	V_{DS}=V_{GS}, I_D=-250 μA (Note 1)	-0.5	-0.8	-1.5	V
Drain-Source ON Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-2.5A (Note 1)	-	75	90	mΩ
		V_{GS}=-2.5V, I_D=-1.0A (Note 1)	-	125	150	
On-State Drain Current	$I_{D(ON)}$	V_{GS}=-4.5V, V_{DS}=-5V (Note 1)	-7	-	-	A
Forward Transconductance	g_{fs}	V_{DS}=-5V, I_D=-2.5A (Note 1)	-	6	-	S
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=-1.25A (Note 1)	-	-0.81	-1.2	V
Dynamic (Note 3)						
Total Gate Charge	Q_g	V_{DS}=-10V, I_D=-2.5A V_{GS}=-4.5V (Fig.1)	-	3.6	-	nC
Gate-Source Charge	Q_{gs}		-	0.9	-	
Gate-Drain Charge	Q_{gd}		-	0.8	-	
Turn-on Delay time	$t_{d(on)}$	V_{DS}=-10V, I_D=1A V_{GS}=-4.5V R_G=6Ω (Fig.2)	-	7.5	-	ns
Turn-on Rise time	t_r		-	10.9	-	
Turn-off Delay time	$t_{d(off)}$		-	27.3	-	
Turn-off Fall time	t_f		-	22.5	-	
Input Capacitance	C_{iss}	V_{DS}=-20V, V_{GS}=0V f = 1.0MHz	-	380	-	pF
Output Capacitance	C_{oss}		-	100	-	
Reverse Trancefer Capacitance	C_{rss}		-	60	-	

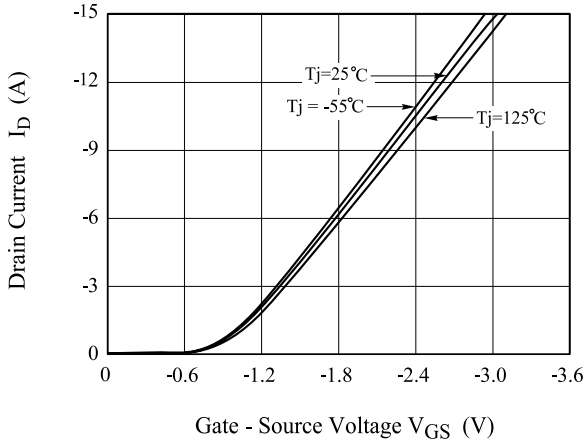
Note 1) Pulse test : Pulse width≤300μs, Duty Cycle≤2%.

Note 2) Guaranteed by design, not subject to production testing.

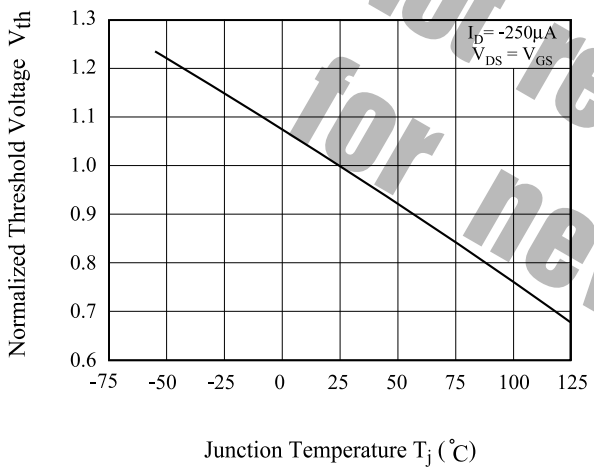
I_D - V_{DS}



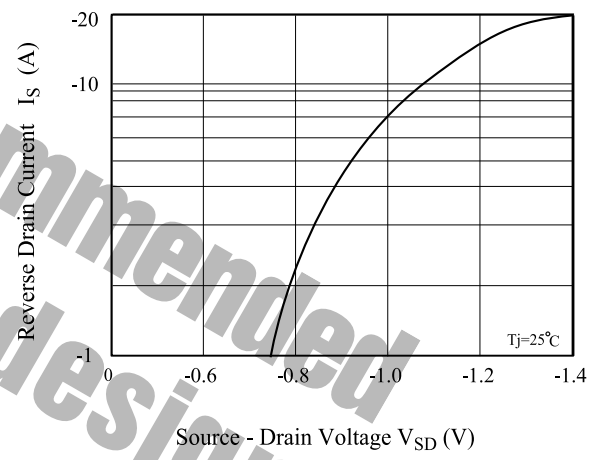
I_D - V_{GS}



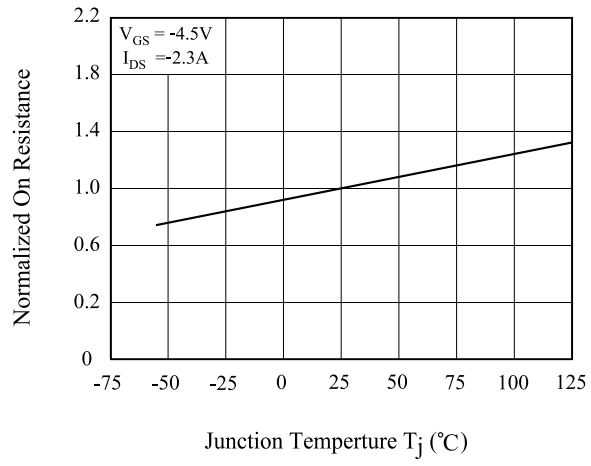
V_{th} - T_j



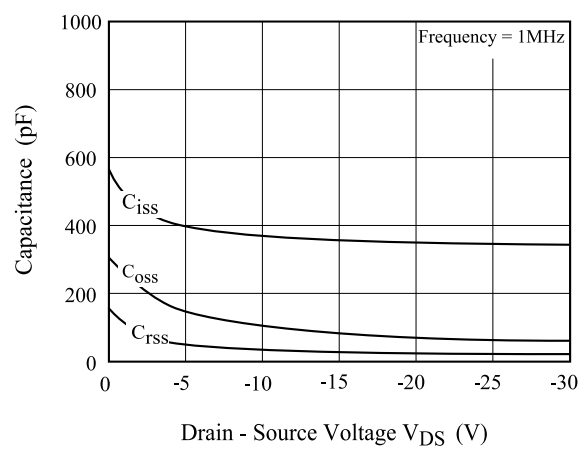
I_S - V_{SD}



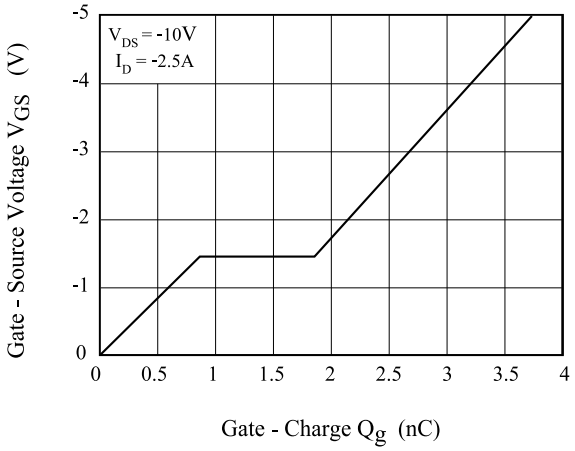
$R_{DS(ON)}$ - T_j



C - V_{DS}



Q_g - V_{GS}



R_{th}

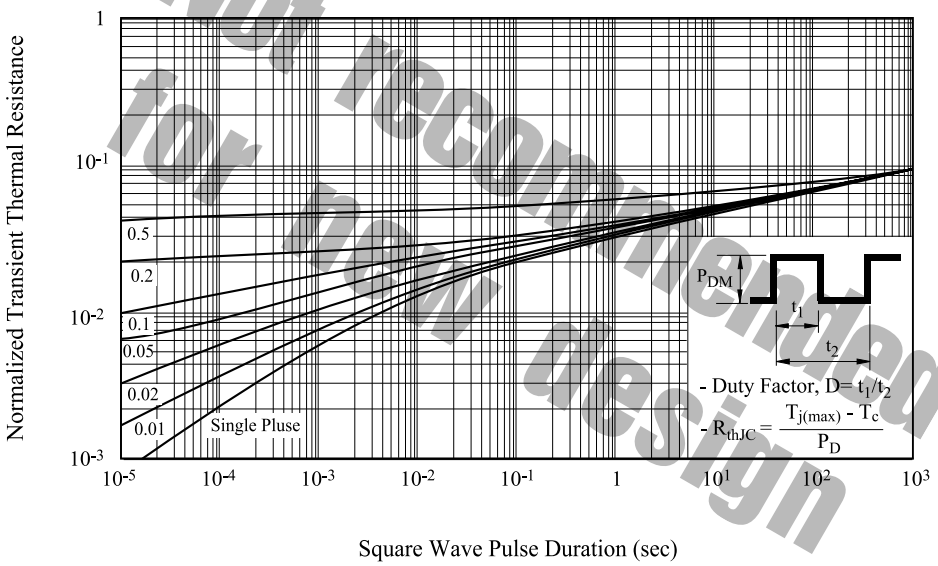
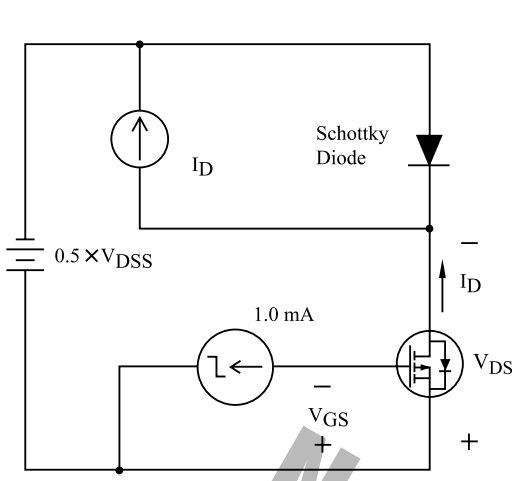


Fig. 1 Gate Charge



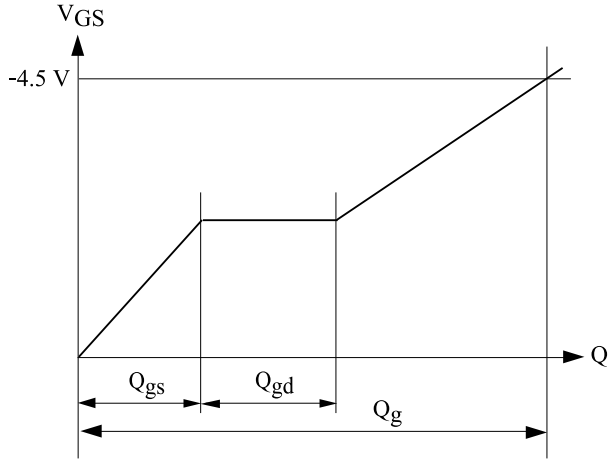


Fig. 2 Resistive Load Switching