KF80N08P/F

N CHANNEL MOS FIELD EFFECT TRANSISTOR

General Description

It s mainly suitable for low voltage applications such as automotive, DC/DC converters and a load switch in battery powered applications

FEATURES

· V_{DSS}= 75V, I_D= 80A

· Drain-Source ON Resistance :

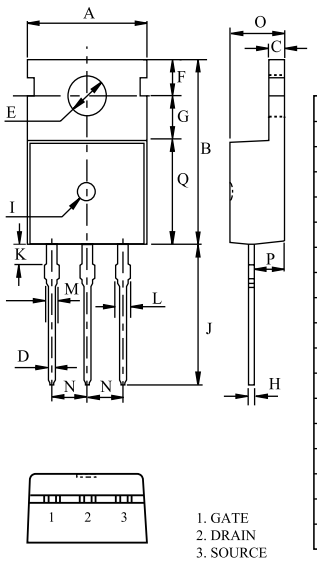
$R_{DS(ON)}$=10mΩ(Max.) @V_{GS} = 10V

MAXIMUM RATING (Tc=25℃)

CHARACTERISTIC		SYMBOL	RATING KF80N08P	RATING KF80N08F	UNIT
Drain-Source Voltage		V_{DSS}	75		V
Gate-Source Voltage		V_{GSS}	±20		V
Drain Current	@T_C=25℃	I_D	80	56	A
	@T_C=100℃		76	39	
	Pulsed (Note1)	I_{DP}	320	224	
Single Pulsed Avalanche Energy (Note 2)		E_{AS}	1200		mJ
Repetitive Avalanche Energy (Note 1)		E_{AR}	18		mJ
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4.5		V/ns
Drain Power Dissipation	Tc=25℃	P_D	230	62.5	W
	Derate above 25℃		1.54	0.42	W/℃
Maximum Junction Temperature		T_j	175		℃
Storage Temperature Range		T_{stg}	-55 175		℃
Thermal Characteristics					
Thermal Resistance, Junction-to-Case		R_{thJC}	0.65	2.4	℃/W
Thermal Resistance, Junction-to-Ambient		R_{thJA}	62.5	62.5	℃/W

* : Drain current limited by maximum junction temperature.

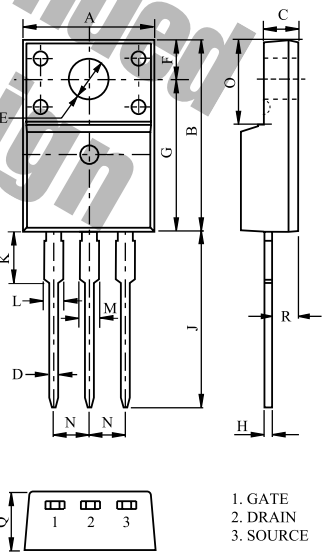
KF80N08P



DIM	MILLIMETERS
A	9.9 ± 0.2
B	15.95 MAX
C	1.3+0.1/-0.05
D	0.8 ± 0.1
E	ø3.6 ± 0.2
F	2.8 ± 0.1
G	3.7
H	0.5+0.1/-0.05
I	ø1.5
J	13.08 ± 0.3
K	1.46
L	1.4 ± 0.1
M	1.27 ± 0.1
N	2.54 ± 0.2
O	4.5 ± 0.2
P	2.4 ± 0.2
Q	9.2 ± 0.2

TO-220AB

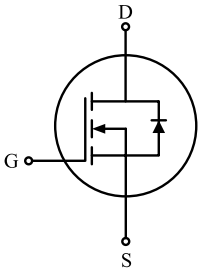
KF80N08F



DIM	MILLIMETERS
A	10.16 ± 0.2
B	15.87 ± 0.2
C	2.54 ± 0.2
D	0.8 ± 0.1
E	ø3.18 ± 0.1
F	3.3 ± 0.1
G	12.57 ± 0.2
H	0.5 ± 0.1
J	13.0 ± 0.5
K	3.23 ± 0.1
L	1.47 MAX
M	1.47 MAX
N	2.54 ± 0.2
O	6.68 ± 0.2
Q	4.7 ± 0.2
R	2.76 ± 0.2

TO-220IS (1)

PIN CONNECTION



ELECTRICAL CHARACTERISTICS (Tc=25℃)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250 μA, V_{GS}=0V	75	-	-	V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_j$	I_D=250 μA, Referenced to 25℃	-	0.11	-	V/℃
Drain Cut-off Current	I_{DSS}	V_{DS}=75V, V_{GS}=0V,	-	-	10	μA
Gate Threshold Voltage	V_{th}	V_{DS}=V_{GS}, I_D=250 μA	2	-	4	V
Gate Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain-Source ON Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=40A	-	8.5	10.0	mΩ
Dynamic						
Total Gate Charge	Q_g	V_{DS}=60V, I_D=80A V_{GS}=10V (Note4,5)	-	107	-	nC
Gate-Source Charge	Q_{gs}		-	20	-	
Gate-Drain Charge	Q_{gd}		-	47	-	
Turn-on Delay time	$t_{d(on)}$	V_{DD}=37.5V I_D=80A R_G=25Ω (Note4,5)	-	63	-	ns
Turn-on Rise time	t_r		-	228	-	
Turn-off Delay time	$t_{d(off)}$		-	217	-	
Turn-off Fall time	t_f		-	150	-	
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	-	3860	-	pF
Output Capacitance	C_{oss}		-	840	-	
Reverse Transfer Capacitance	C_{rss}		-	175	-	
Source-Drain Diode Ratings						
Continuous Source Current	I_S	V_{GS}<V_{th}	-	-	80	A
Pulsed Source Current	I_{SP}		-	-	320	
Diode Forward Voltage	V_{SD}	I_S=80A, V_{GS}=0V	-	-	1.5	V
Reverse Recovery Time	t_{rr}	I_S=80A, V_{GS}=0V, dIs/dt=100A/μs	-	114	-	ns
Reverse Recovery Charge	Q_{rr}		-	610	-	μC

Note 1) Repetivity rating : Pulse width limited by junction temperature.

Note 2) L =138 μH, I_S=80A, V_{DD}=50V, R_G=25Ω, Starting T_j=25℃.

Note 3) I_S≤7.0A, dI/dt≤200A/μs, V_{DD}≤BV_{DSS}, Starting T_j=25℃.

Note 4) Pulse Test : Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

Note 5) Essentially independent of operating temperature.

Marking

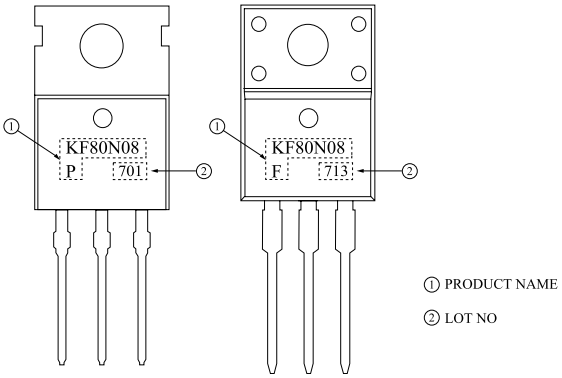


Fig1. I_D - V_{DS}

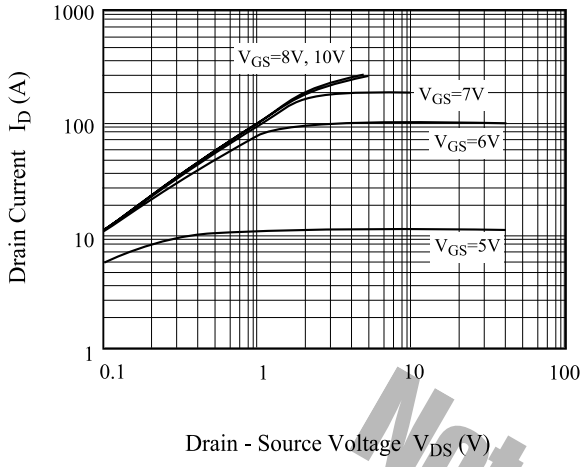


Fig2. I_D - V_{GS}

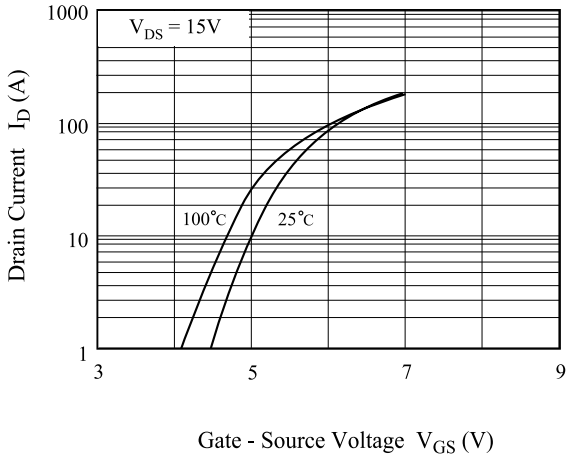


Fig3. BV_{DSS} - Tj

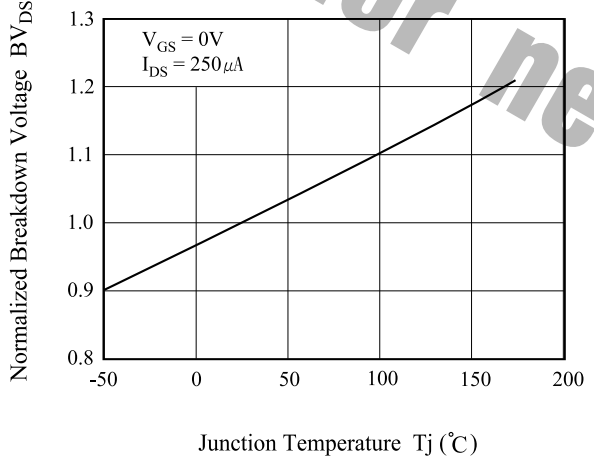


Fig4. $R_{DS(ON)}$ - I_D

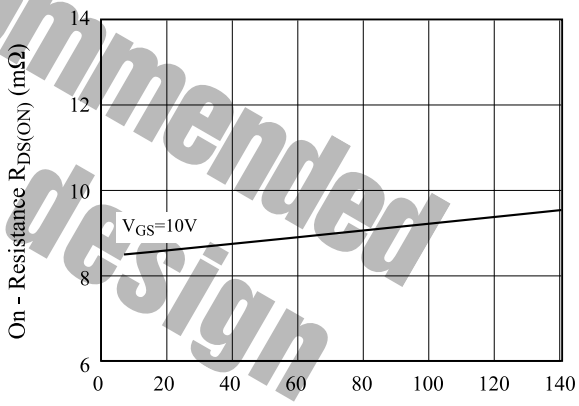


Fig5. I_S - V_{SD}

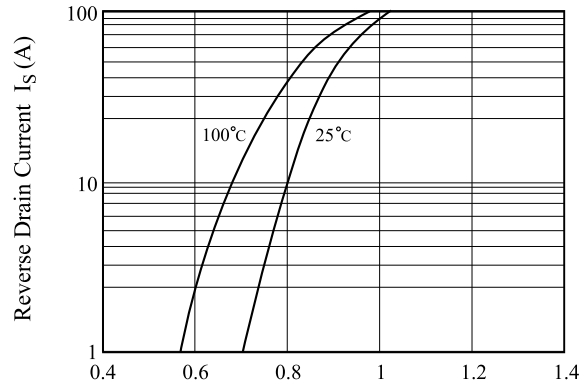


Fig6. $R_{DS(ON)}$ - T_C

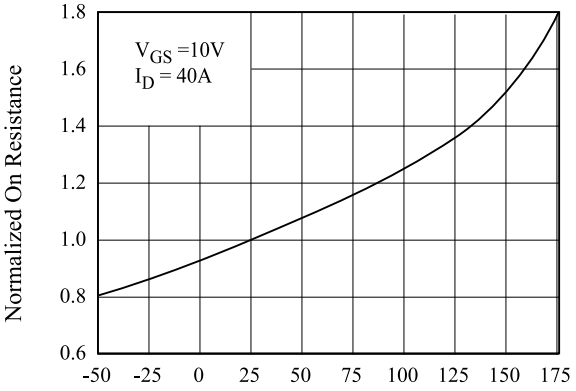


Fig 7. C - V_{DS}

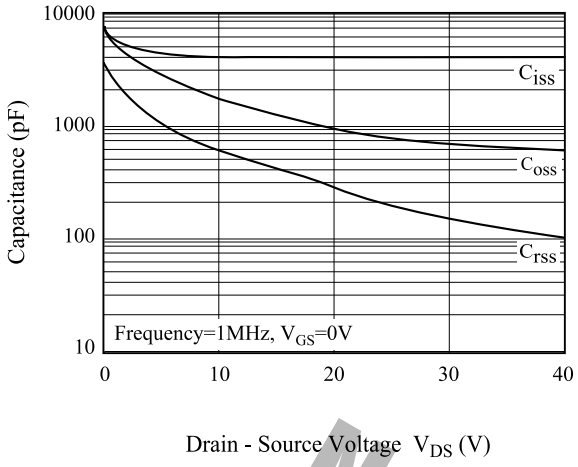


Fig8. Q_g- V_{GS}

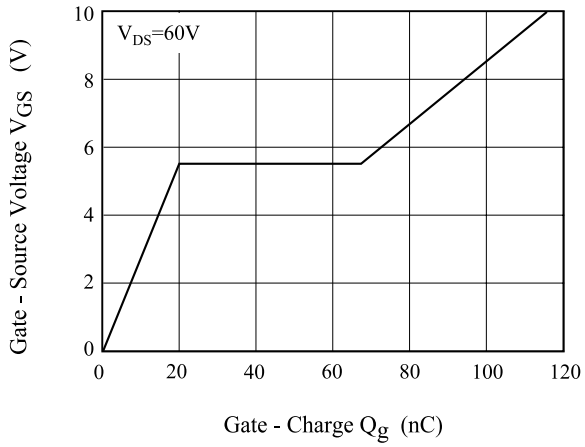


Fig9. Safe Operation Area

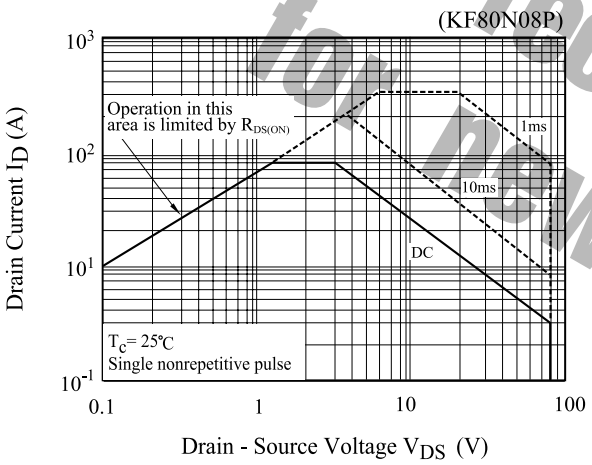


Fig10. Safe Operation Area

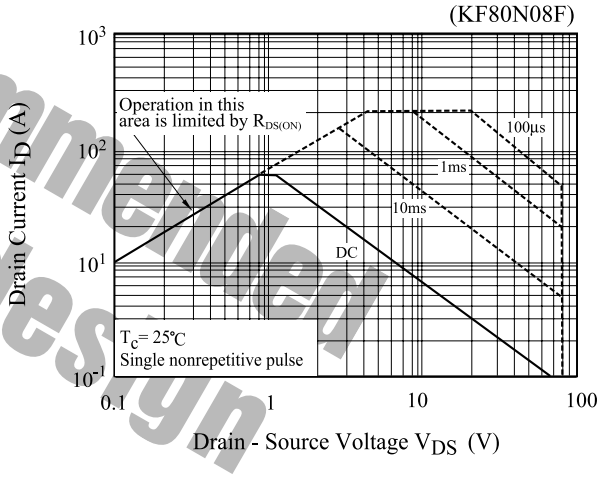


Fig11. I_D - T_j

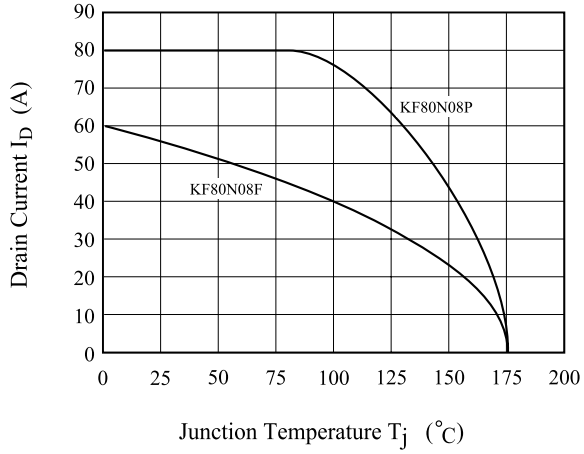


Fig12. Transient Thermal Response Curve

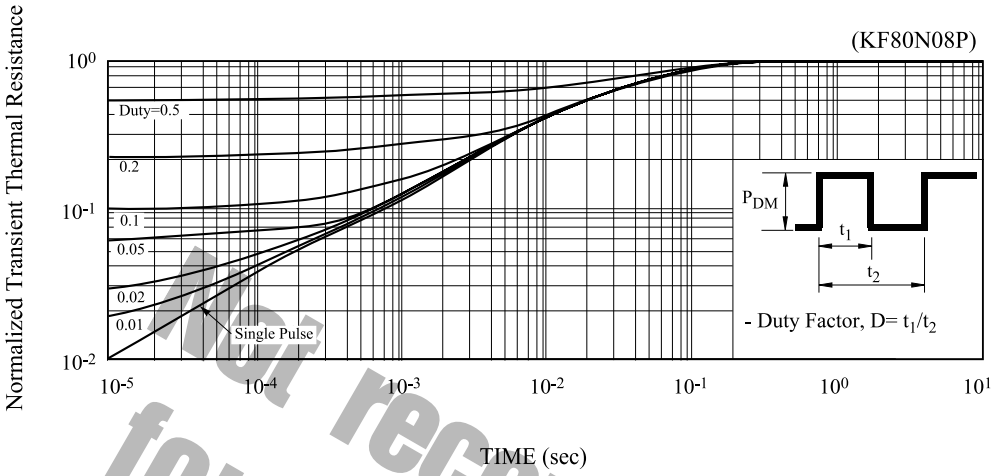


Fig13. Transient Thermal Response Curve

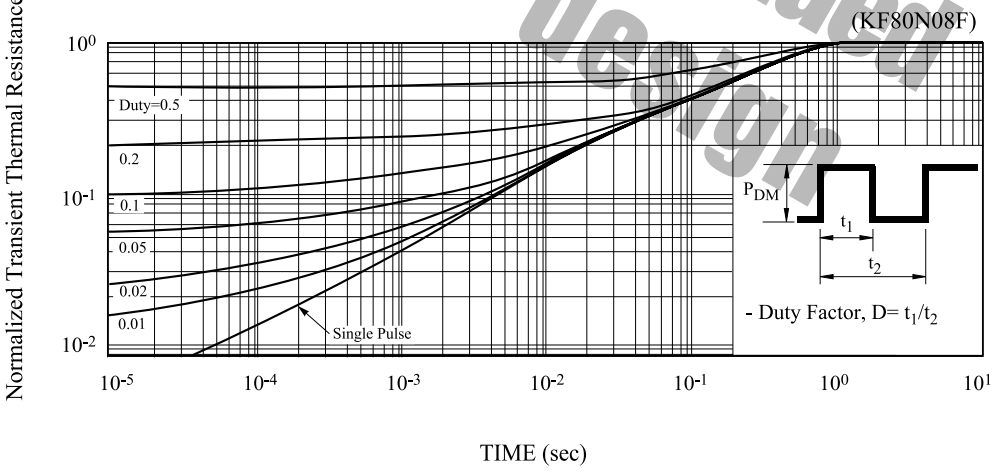
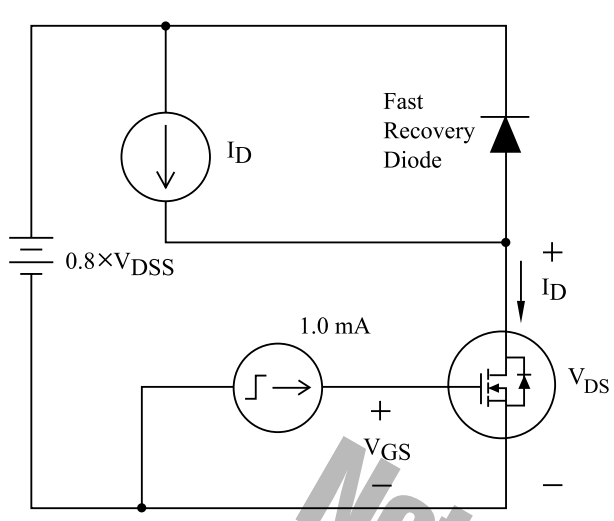


Fig14. Gate Charge



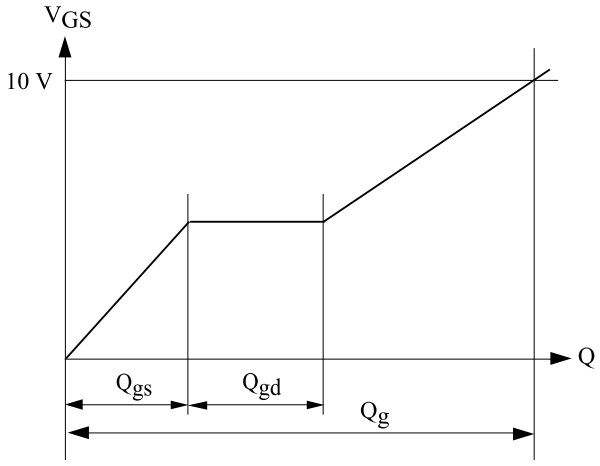
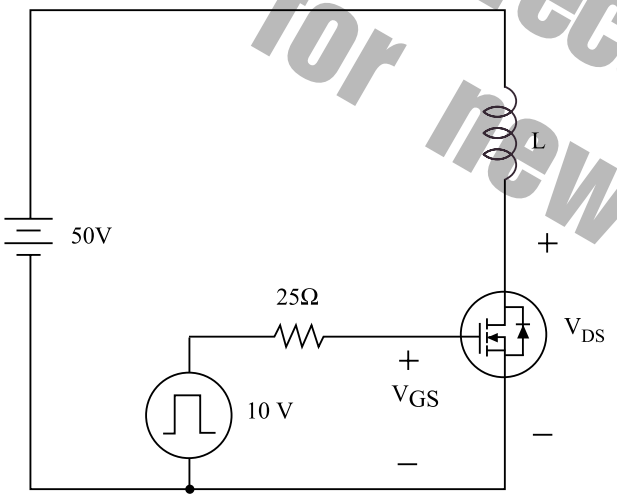


Fig15. Single Pulsed Avalanche Energy



$$E_{AS}= \frac{1}{2} LI_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

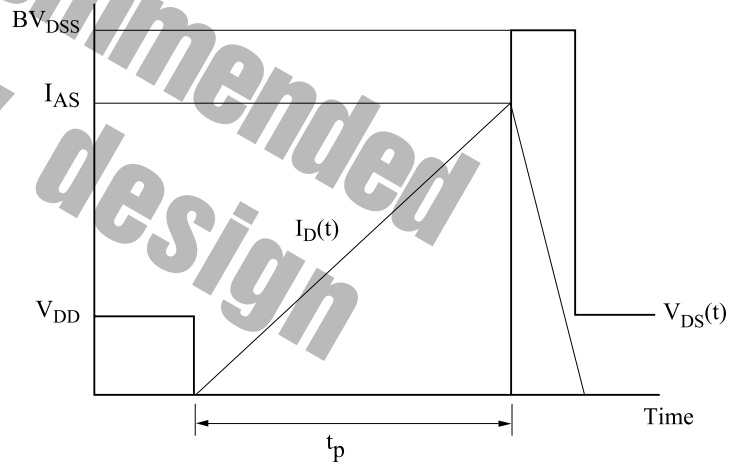
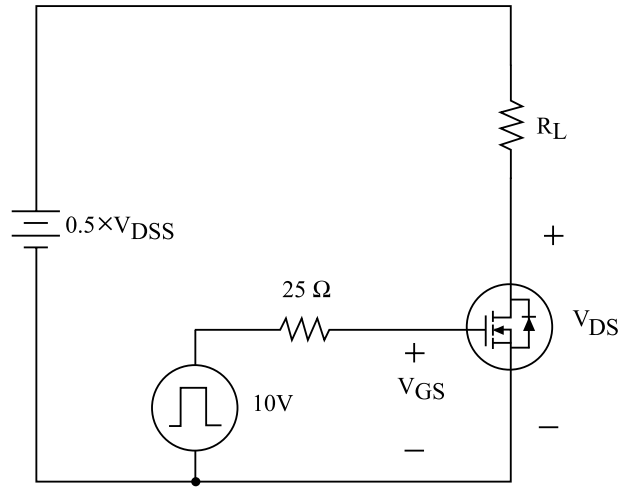


Fig16. Resistive Load Switching



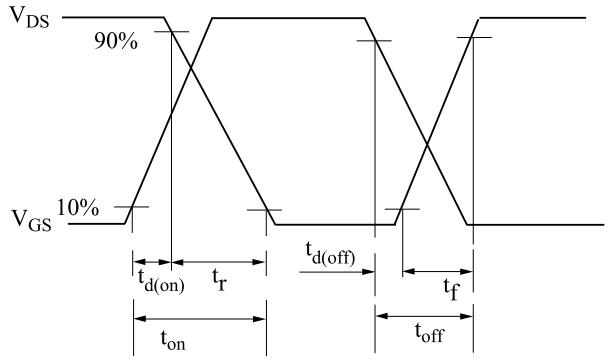


Fig17. Source - Drain Diode Reverse Recovery and dv /dt