

# FDMC4435BZ

## P-Channel Power Trench® MOSFET -30 V, -18 A, 20 mΩ

### Features

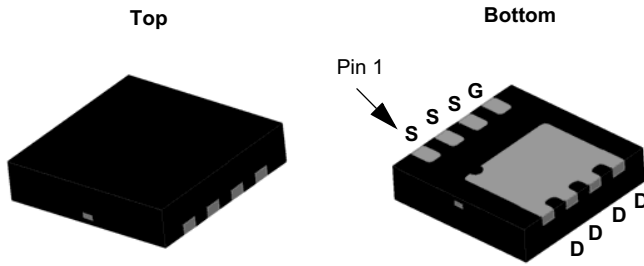
- Max  $r_{DS(on)}$  = 20 mΩ at  $V_{GS} = -10$  V,  $I_D = -8.5$  A
- Max  $r_{DS(on)}$  = 37 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -6.3$  A
- Extended  $V_{GSS}$  range (-25 V) for battery applications
- High performance trench technology for extremely low  $r_{DS(on)}$
- High power and current handling capability
- HBM ESD protection level >7 kV typical (Note 4)
- 100% UIL Tested
- Termination is Lead-free and RoHS Compliant

### General Description

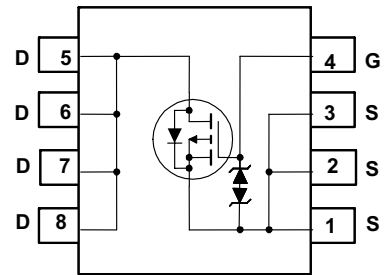
This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

### Applications

- High side in DC - DC Buck Converters
- Notebook battery power management
- Load switch in Notebook



MLP 3.3x3.3



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	-30	V
$V_{GS}$	Gate to Source Voltage	±25	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25$ °C	-18	A
	-Continuous (Silicon limited) $T_C = 25$ °C	-32	
	-Continuous $T_A = 25$ °C (Note 1a)	-8.5	
	-Pulsed	-50	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	24	mJ
$P_D$	Power Dissipation $T_C = 25$ °C	31	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC4435BZ	FDMC4435BZ	MLP 3.3X3.3	13 "	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-22		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^\circ\text{C}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 25\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -250\text{ }\mu\text{A}$	-1.0	-1.9	-3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		5.3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\text{ V}$ , $I_D = -8.5\text{ A}$		15	20	m $\Omega$
		$V_{GS} = -4.5\text{ V}$ , $I_D = -6.3\text{ A}$		23	37	
		$V_{GS} = -10\text{ V}$ , $I_D = -8.5\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		21	28	
$g_{FS}$	Forward Transconductance	$V_{DD} = -5\text{ V}$ , $I_D = -8.5\text{ A}$		24		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = -15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		1540	2045	pF
$C_{oss}$	Output Capacitance			295	395	pF
$C_{rss}$	Reverse Transfer Capacitance			260	385	pF
$R_g$	Gate Resistance		$f = 1\text{ MHz}$		5	

**Switching Characteristics**

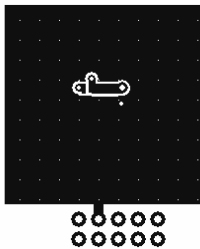
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15\text{ V}$ , $I_D = -8.5\text{ A}$ , $V_{GS} = -10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		10	20	ns	
$t_r$	Rise Time			6	12	ns	
$t_{d(off)}$	Turn-Off Delay Time			34	55	ns	
$t_f$	Fall Time			20	36	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to } -10\text{ V}$		33	46	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to } -4.5\text{ V}$	$V_{DD} = -15\text{ V}$ , $I_D = -8.5\text{ A}$		17	24	nC
$Q_{gs}$	Gate to Source Charge				5		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				9		nC

**Drain-Source Diode Characteristics**

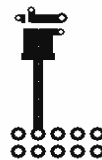
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = -8.5\text{ A}$ (Note 2)		0.92	1.5	V
		$V_{GS} = 0\text{ V}$ , $I_S = -1.9\text{ A}$ (Note 2)		0.75	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = -8.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		22		ns
$Q_{rr}$	Reverse Recovery Charge			11		nC

NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $53\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b.  $125\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width  $< 300\text{ }\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3.  $E_{AS}$  of 24 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = -7\text{ A}$ ,  $V_{DD} = -27\text{ V}$ ,  $V_{GS} = -10\text{ V}$ . 100% test at  $L = 3\text{ mH}$ ,  $I_{AS} = -4\text{ A}$ .

4. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

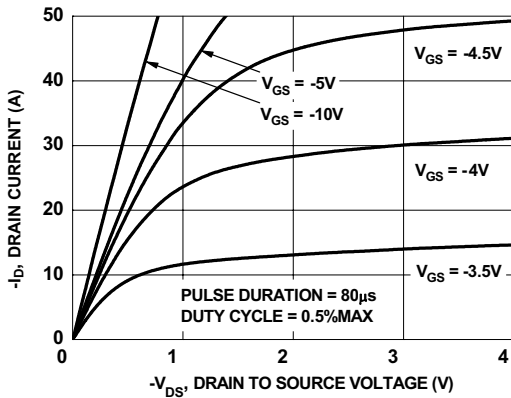


Figure 1. On-Region Characteristics

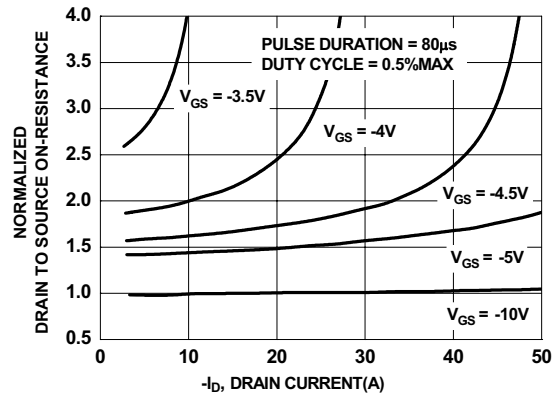


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

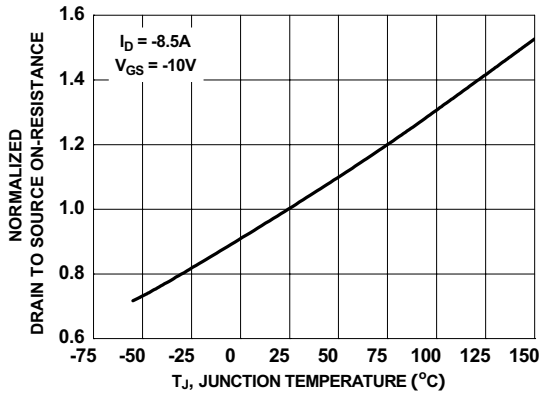


Figure 3. Normalized On-Resistance vs Junction Temperature

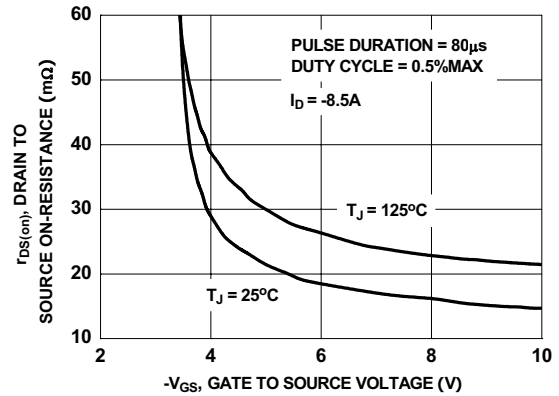


Figure 4. On-Resistance vs Gate to Source Voltage

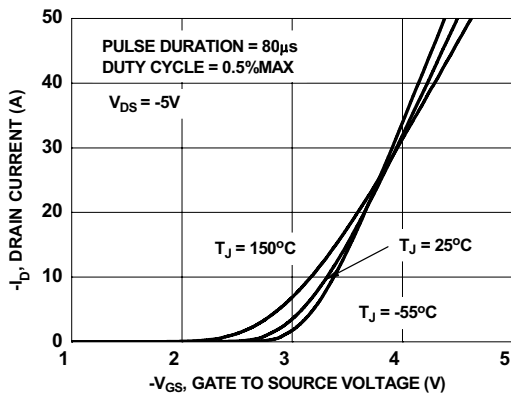


Figure 5. Transfer Characteristics

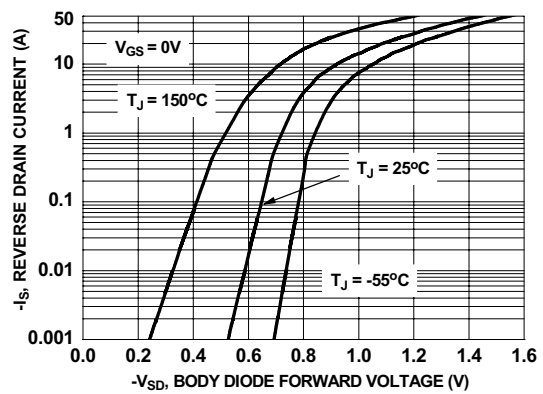
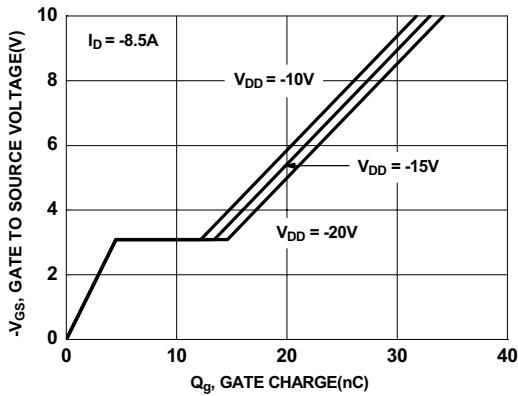
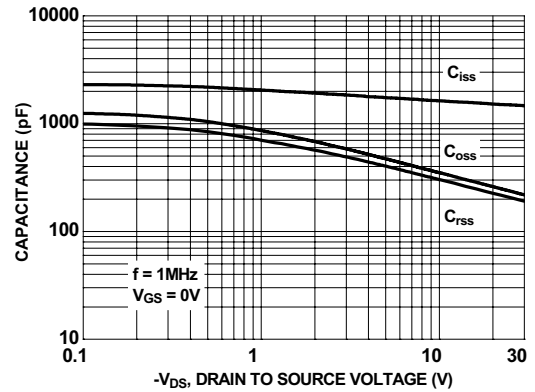


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

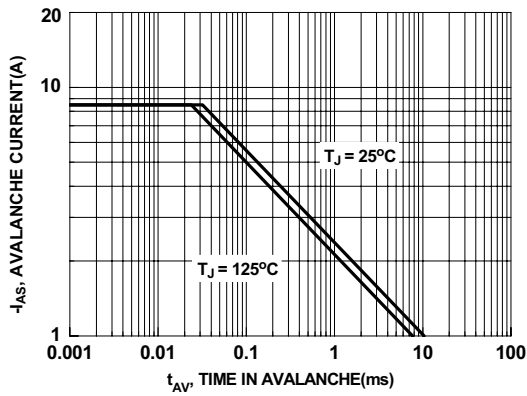
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



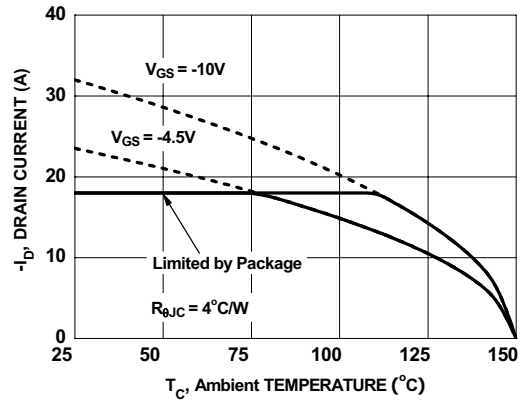
**Figure 7. Gate Charge Characteristics**



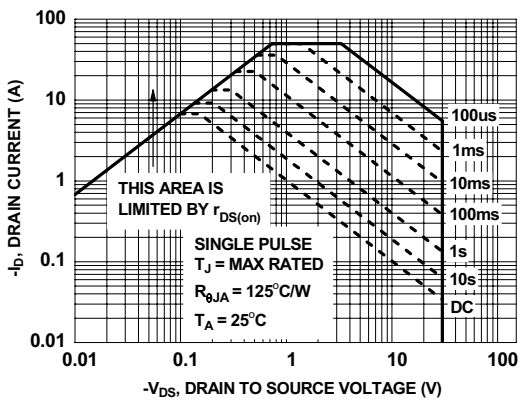
**Figure 8. Capacitance vs Drain to Source Voltage**



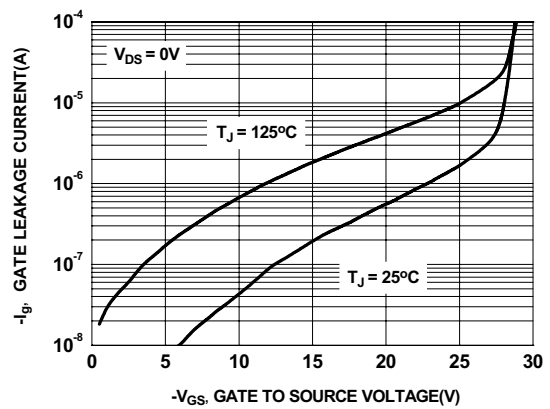
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**



**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Igss vs Vgss**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

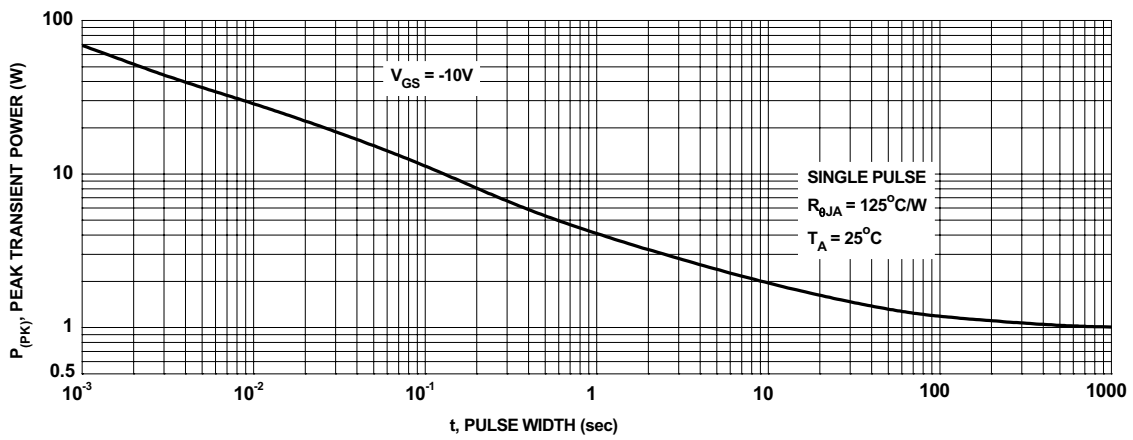


Figure 13. Single Pulse Maximum Power Dissipation

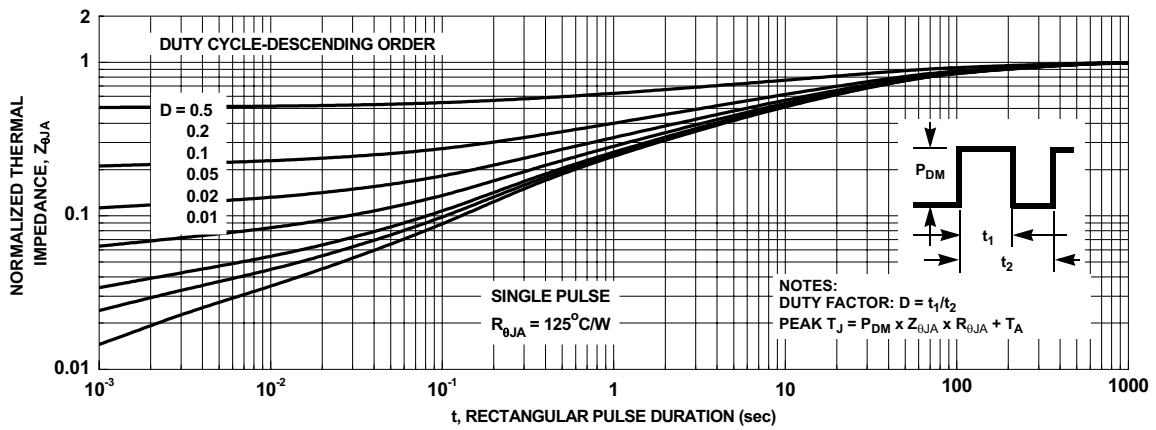
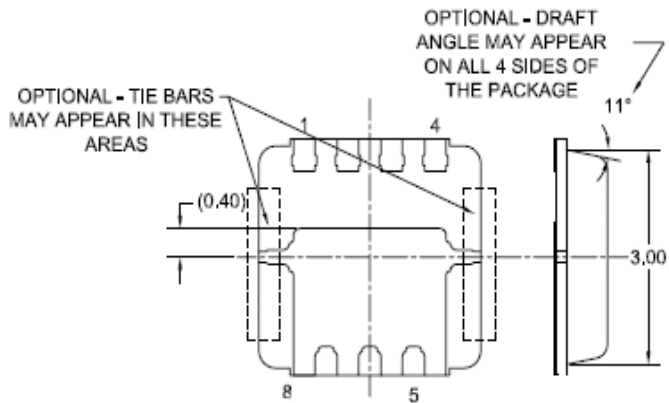
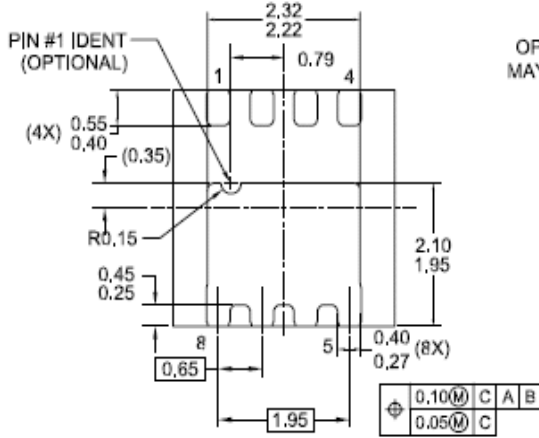
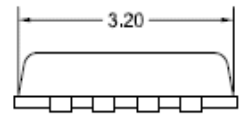
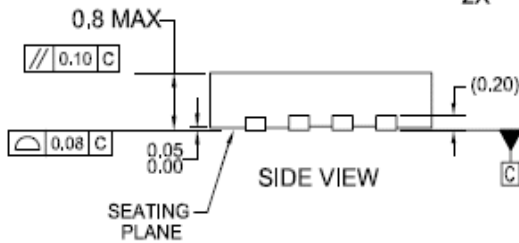
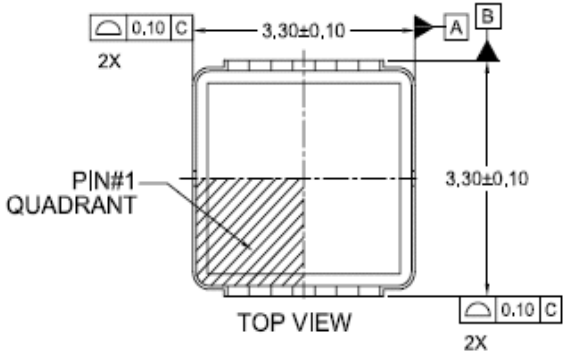
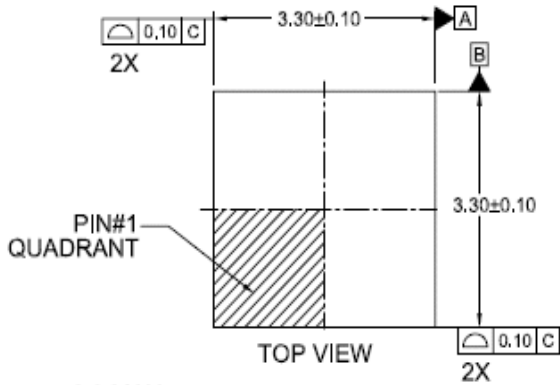


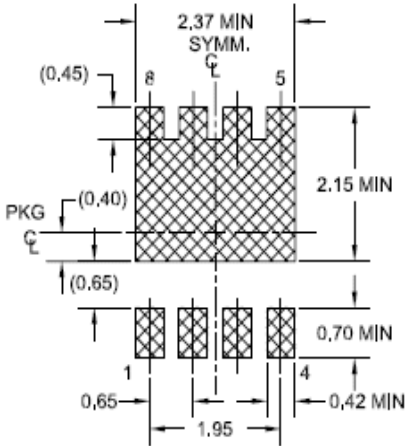
Figure 14. Transient Thermal Response Curve

**Dimensional Outline and Pad Layout**



**BOTTOM VIEW (OPTION A)**

**BOTTOM VIEW (OPTION B)**








**NOTES:**

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MQ-240.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- D. DIMENSIONS DOES NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.
- E. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
- F. DRAWING FILENAME; MKT-MLP08Wrev1.
- G. OPTION A - SAWN MLP.  
OPTION B - PUNCH MLP.



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Dual Cool™	MegaBuck™	Saving our world, 1mW/W/kW at a time™	
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EfficientMax™	MicroFET™	SmartMax™	
ESBC™	MicroPak™	SMART START™	
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**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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