FAIRCHILD SEMICONDUCTOR®

June 2010

SupreMOS™

FCI25N60N_F102

N-Channel MOSFET

600V, 25A, 0.125Ω

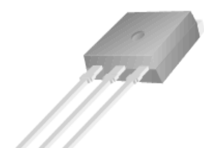
Features

- $R_{DS(on)}$ = 0.107Ω (Typ.)@ V_{GS} = 10V, I_D = 12.5A
- Ultra Low Gate Charge (Typ. Qg = 57nC)
- Low Effective Output Capacitance
- 100% Avalanche Tested
- RoHS Compliant

Description

The SupreMOS MOSFET, Fairchild's next generation of high voltage super-junction MOSFETs, employs a deep trench filling process that differentiates it from preceding multi-epi based technologies. By utilizing this advanced technology and precise process control, SupreMOS provides world class Rsp, superior switching performance and ruggedness.

This SupreMOS MOSFET fits the industry's AC-DC SMPS requirements for PFC, server/telecom power, FPD TV power, ATX power, and industrial power applications.



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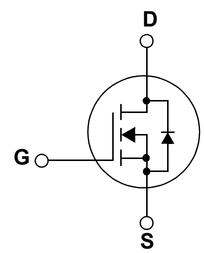


MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol	Parameter		FCI25N60N_F102	Units
V_{DSS}	Drain to Source Voltage		600	V
V_{GSS}	Gate to Source Voltage		±30	V
I_D	Drain Current	Continuous (T_C = 25°C)	25	A
		Continuous (T_C = 100°C)	16	
I_{DM}	Drain Current	Pulsed (Note 1)	75	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		861	mJ
I_{AR}	Avalanche Current		8.3	A
E_{AR}	Repetitive Avalanche Energy		2.2	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		20	V/ns
	MOSFET dv/dt		100	
P_D	Power Dissipation	(T_C = 25°C)	216	W
		Derate above 25°C	1.72	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FCI25N60N_F102	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.58	°C/W
$R_{\theta CS}$	Thermal Resistance, Case to Heat Sink (Typical)	0.5	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

Package Marking and Ordering Information $T_C = 25^oC$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCI25N60N	FCI25N60N_F102	I2PAK	-	-	50

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 1mA$, $V_{GS} = 0V, T_J = 25^oC$	600	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 1mA$, Referenced to 25^oC	-	0.74	-	$V/^oC$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 480V$, $V_{GS} = 0V$	-	-	10	μA
		$V_{DS} = 480V$, $T_J = 125^oC$	-	-	100	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30V$, $V_{DS} = 0V$	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10V$, $I_D = 12.5A$	-	0.107	0.125	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20V$, $I_D = 12.5A$	-		-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 100V$, $V_{GS} = 0V$ f = 1MHz	-	2520	3352	pF
C_{oss}	Output Capacitance		-	103	137	pF
C_{rss}	Reverse Transfer Capacitance		-	3.2	5	pF
C_{oss}	Output Capacitance	$V_{DS} = 380V$, $V_{GS} = 0V$, f = 1MHz	-	55	-	pF
C_{oss}eff.	Effective Output Capacitance	$V_{DS} = 0V$ to $480V$, $V_{GS} = 0V$	-	262	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380V$, $I_D = 12.5A$, $V_{GS} = 10V$ (Note 4)	-	57	74	nC
Q_{gs}	Gate to Source Gate Charge		-	10	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	18	-	nC
ESR	Equivalent Series Resistance (G-S)	Drain Open, f=1MHz	-	1	-	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380V$, $I_D = 12.5A$ $R_G = 4.7\Omega$ (Note 4)	-	21	52	ns
t_r	Turn-On Rise Time		-	22	54	ns
$t_{d(off)}$	Turn-Off Delay Time		-	68	146	ns
t_f	Turn-Off Fall Time		-	5	20	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	25	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	75	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V$, $I_{SD} = 12.5A$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V$, $I_{SD} = 12.5A$ $dI_F/dt = 100A/\mu s$	-	370	-	ns
Q_{rr}	Reverse Recovery Charge		-	7	-	μC

Notes:
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $I_{AS} = 8.3A$, $R_G = 25\Omega$, Starting $T_J = 25°C$
3. $I_{SD} \le 25A$, $di/dt \le 200A/\mu s$, $V_{DD} \le 380V$, Starting $T_J = 25°C$
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

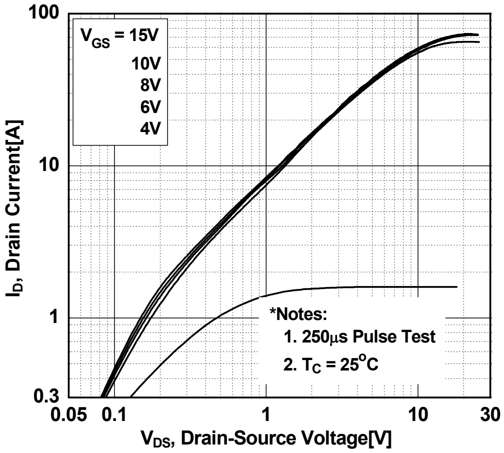


Figure 2. Transfer Characteristics

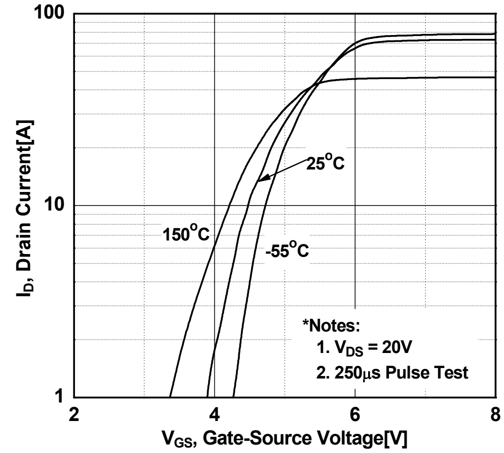


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

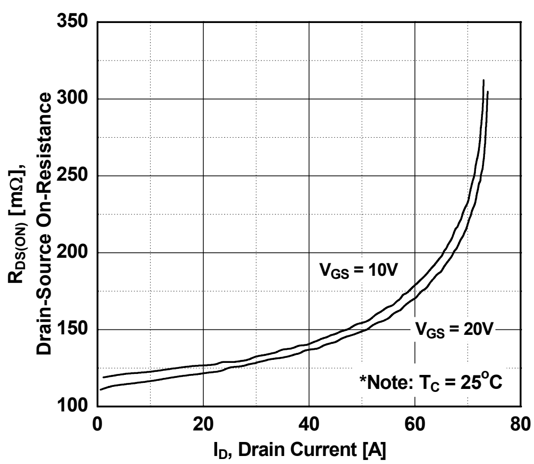


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

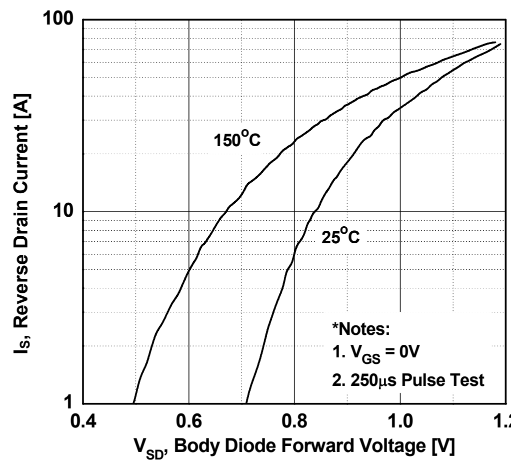


Figure 5. Capacitance Characteristics

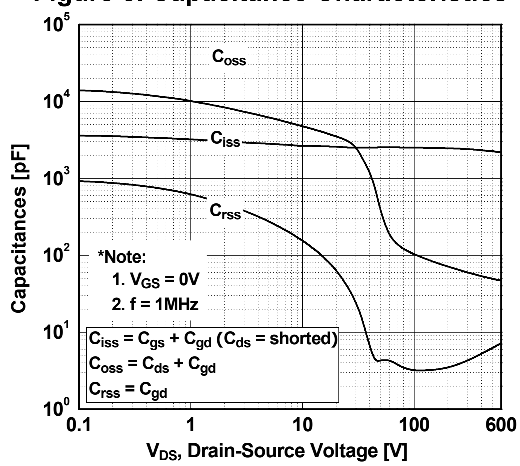
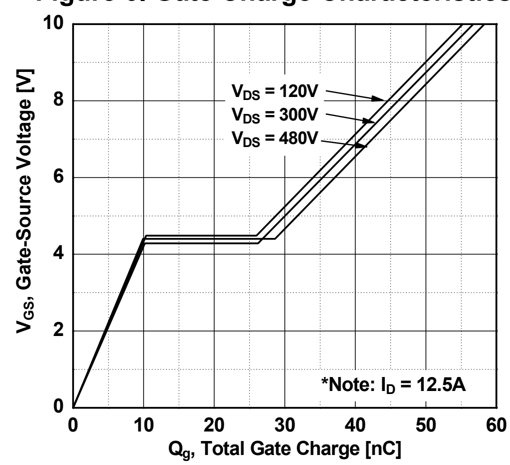


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

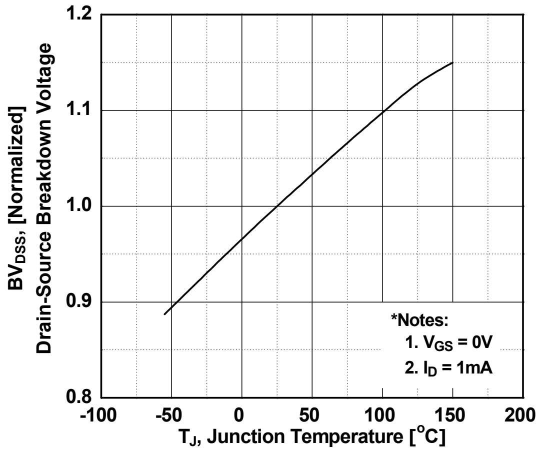


Figure 8. On-Resistance Variation vs. Temperature

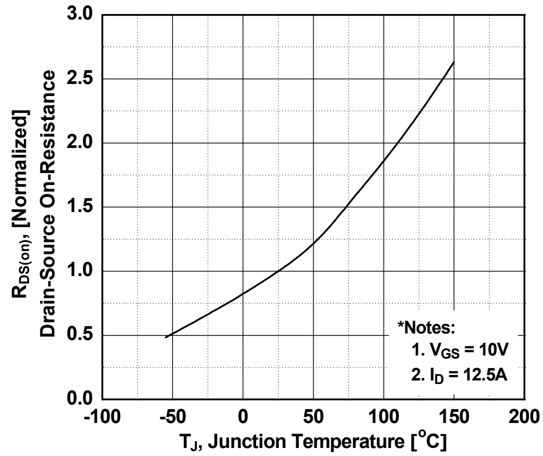


Figure 9. Maximum Safe Operating Area

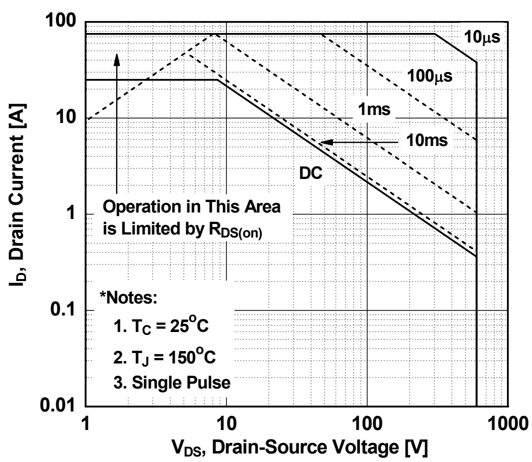


Figure 10. Maximum Drain Current vs. Case Temperature

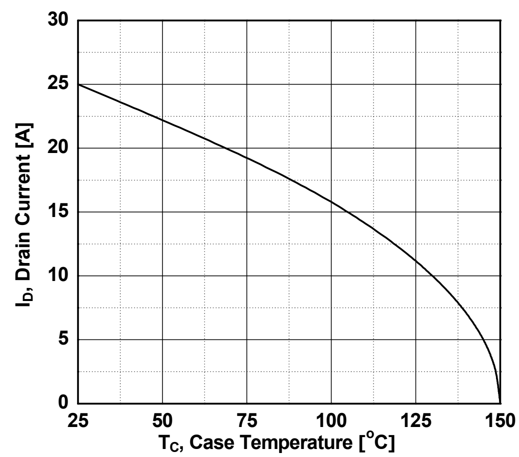
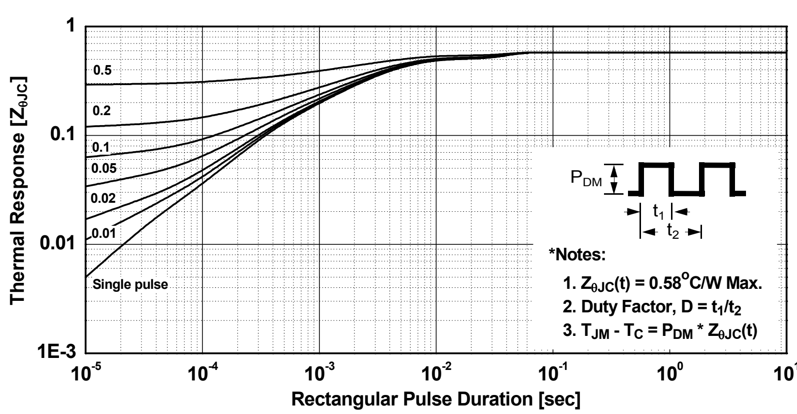
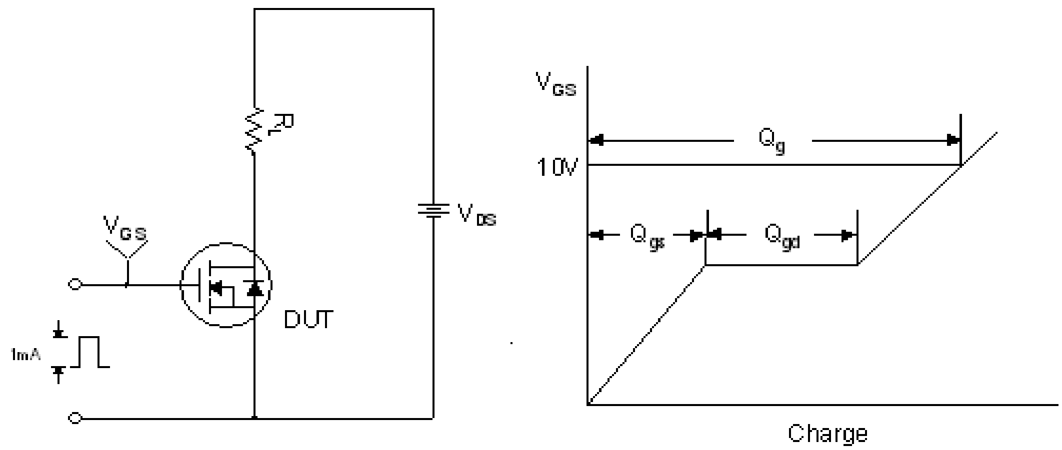


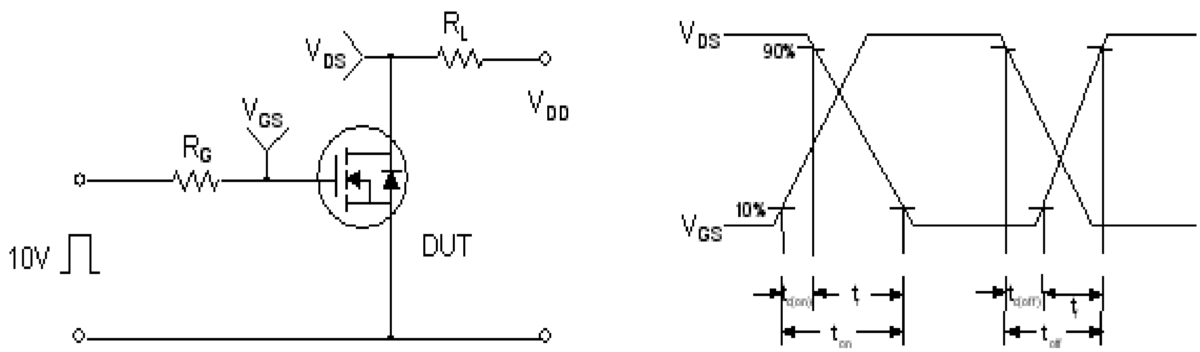
Figure 11. Transient Thermal Response Curve



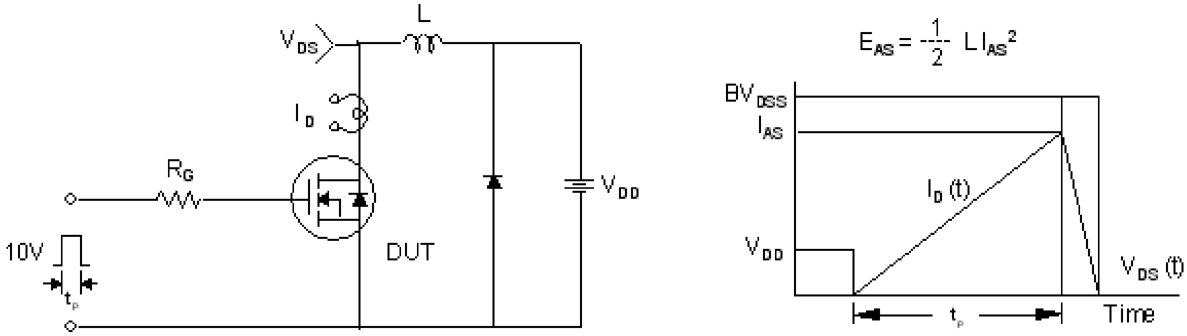
Gate Charge Test Circuit & Waveform



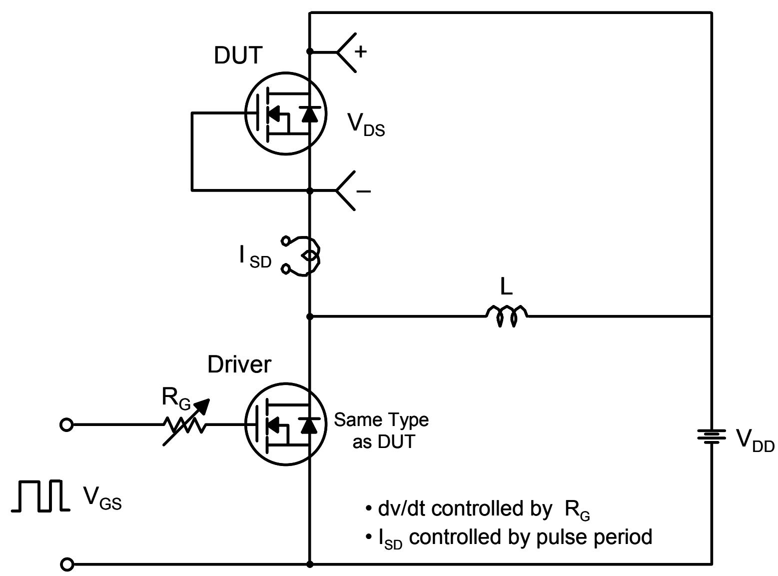
Resistive Switching Test Circuit & Waveforms

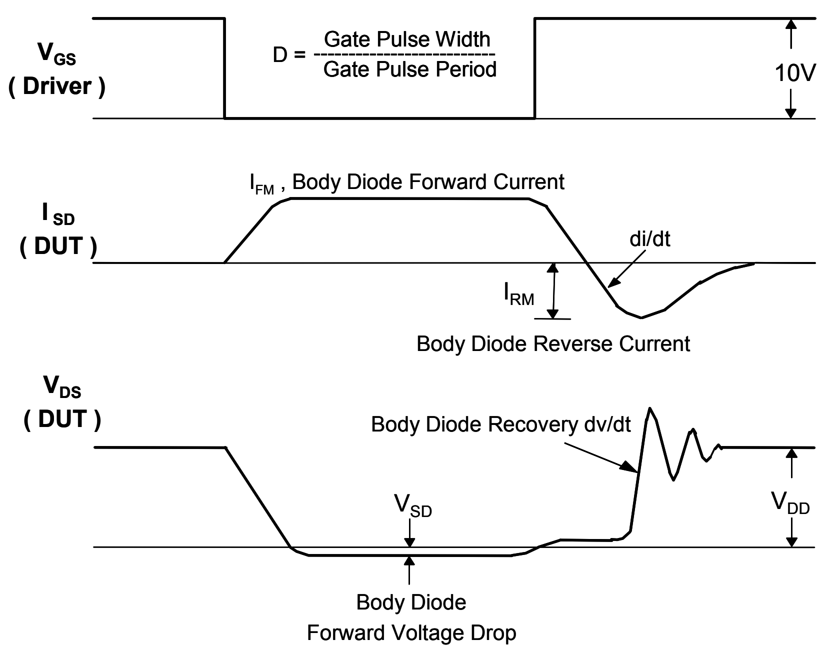


Unclamped Inductive Switching Test Circuit & Waveforms



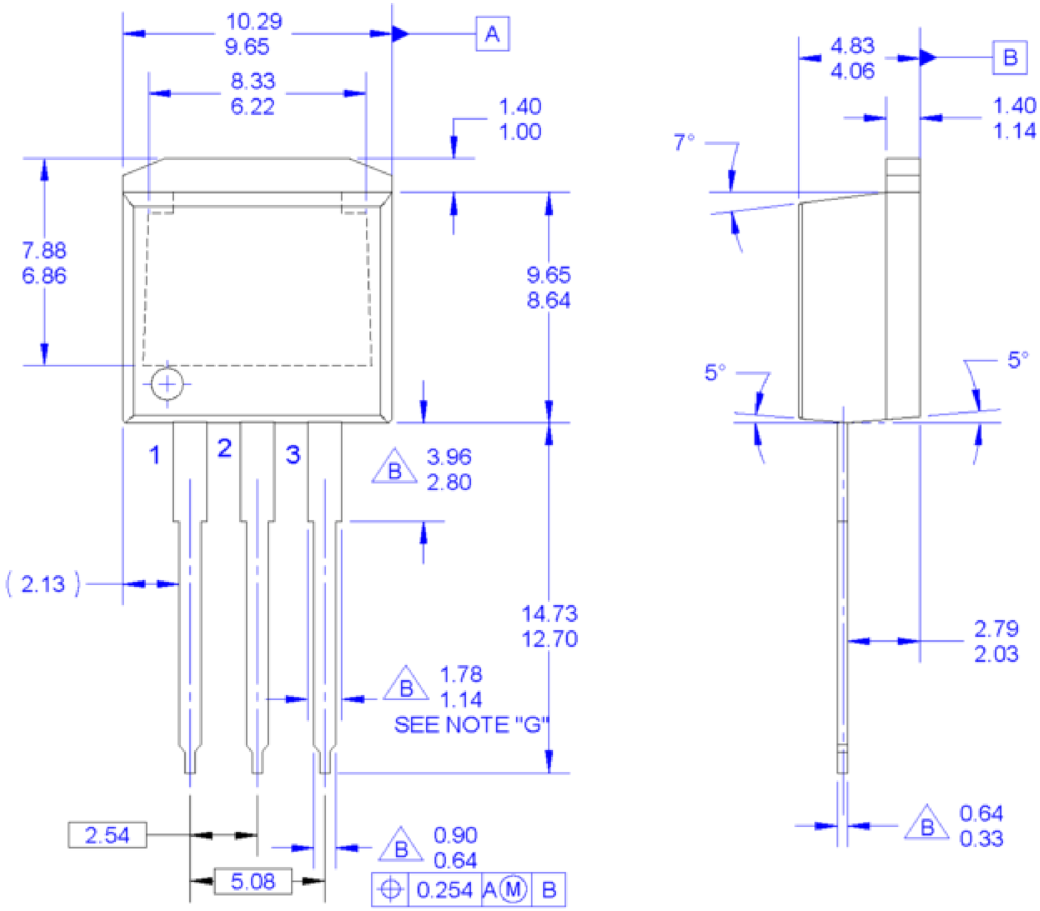
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Mechanical Dimensions

TO-262-3L



NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
B. DOES NOT COMPLY JEDEC STD. VALUE.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.
H. DRAWING FILE NAME: TO262A03REV5

Dimensions in Millimeters

FAIRCHILD SEMICONDUCTOR®

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I48