

FCD7N60 / FCU7N60

600V N-Channel MOSFET

Features

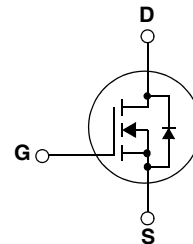
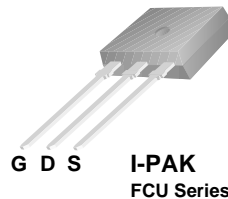
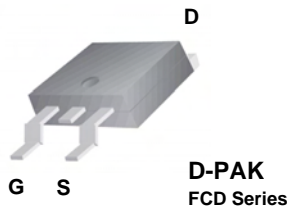
- 650V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{ds(on)} = 0.53\Omega$
- Ultra low gate charge (typ. $Q_g = 23\text{nC}$)
- Low effective output capacitance (typ. $C_{oss,eff} = 60\text{pF}$)
- 100% avalanche tested
- RoHS Compliant



Description

SuperFET™ is, Fairchild's proprietary, new generation of high voltage MOSFET family that is utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance.

This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET is very suitable for various AC/DC power conversion in switching mode operation for system miniaturization and higher efficiency.



Absolute Maximum Ratings

Symbol	Parameter	FCD7N60/FCU7N60	Unit
V_{DSS}	Drain-Source Voltage	600	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	7 4.4	A A
I_{DM}	Drain Current - Pulsed (Note 1)	21	A
V_{GSS}	Gate-Source voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	230	mJ
I_{AR}	Avalanche Current (Note 1)	7	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	8.3	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	20	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C	83 0.67	W W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FCD7N60/FCU7N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	83	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCD7N60	FCD7N60TM	D-PAK	380mm	16mm	2500
FCD7N60	FCD7N60TF	D-PAK	380mm	16mm	2000
FCU7N60	FCU7N60	I-PAK	-	-	70

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA, T _J = 25°C	600	--	--	V
		V _{GS} = 0V, I _D = 250μA, T _J = 150°C	--	650	--	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250μA, Referenced to 25°C	--	0.6	--	V/°C
BV _{DS}	Drain-Source Avalanche Breakdown Voltage	V _{GS} = 0V, I _D = 7A	--	700	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 600V, V _{GS} = 0V	--	--	1	μA
		V _{DS} = 480V, T _C = 125°C	--	--	10	μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30V, V _{DS} = 0V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30V, V _{DS} = 0V	--	--	-100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	3.0	--	5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10V, I _D = 3.5A	--	0.53	0.6	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40V, I _D = 3.5A (Note 4)	--	6	--	S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz	--	710	920	pF
C _{oss}	Output Capacitance		--	380	500	pF
C _{riss}	Reverse Transfer Capacitance		--	34	--	pF
C _{oss}	Output Capacitance	V _{DS} = 480V, V _{GS} = 0V, f = 1.0MHz	--	22	29	pF
C _{oss eff.}	Effective Output Capacitance	V _{DS} = 0V to 400V, V _{GS} = 0V	--	60	--	pF
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = 300V, I _D = 7A R _G = 25Ω	--	35	80	ns
t _r	Turn-On Rise Time		--	55	120	ns
t _{d(off)}	Turn-Off Delay Time		--	75	160	ns
t _f	Turn-Off Fall Time		(Note 4, 5)	--	32	75
Q _g	Total Gate Charge	V _{DS} = 480V, I _D = 7A V _{GS} = 10V	--	23	30	nC
Q _{gs}	Gate-Source Charge		--	4.2	5.5	nC
Q _{gd}	Gate-Drain Charge		(Note 4, 5)	--	11.5	--
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	7	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	21	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0V, I _S = 7A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _S = 7A di _F /dt = 100A/μs (Note 4)	--	360	--	ns
Q _{rr}	Reverse Recovery Charge		--	4.5	--	μC

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I_{AS} = 3.5A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. I_{SD} ≤ 7A, di/dt ≤ 1200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature

Typical Performance Characteristics

Figure 1. On-Region Characteristics

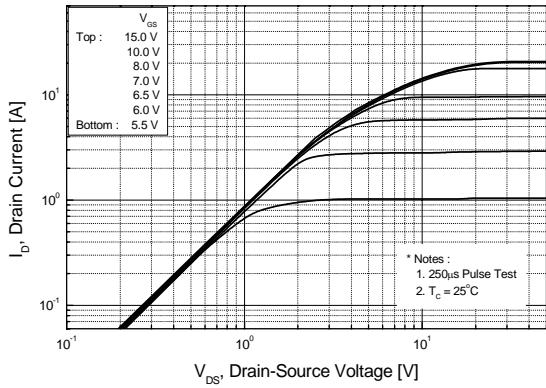


Figure 2. Transfer Characteristics

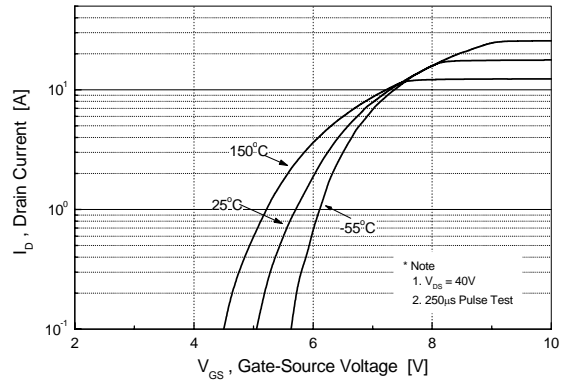


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

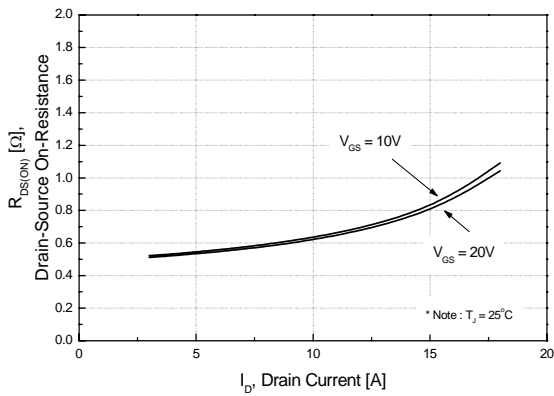


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

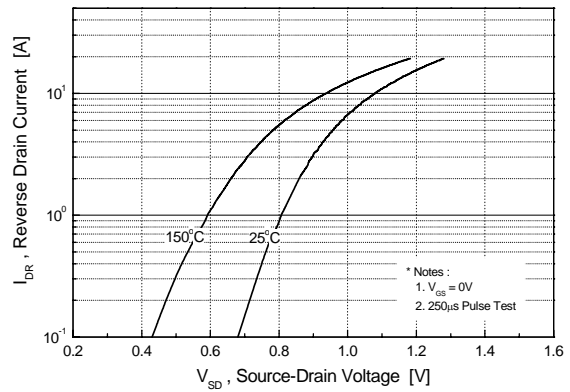


Figure 5. Capacitance Characteristics

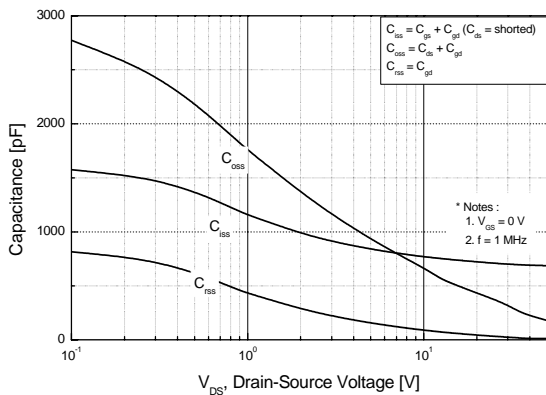
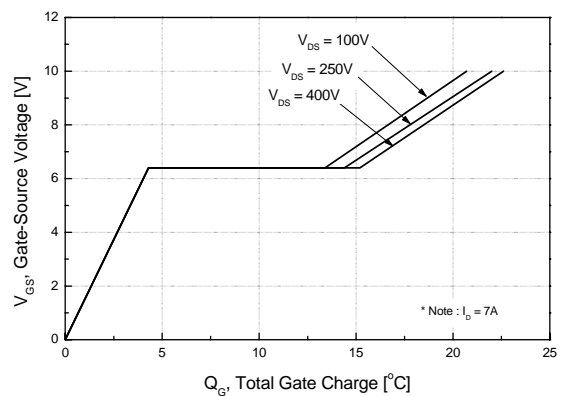


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

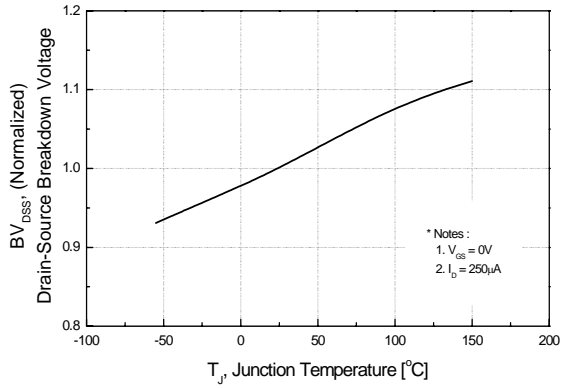


Figure 8. On-Resistance Variation vs. Temperature

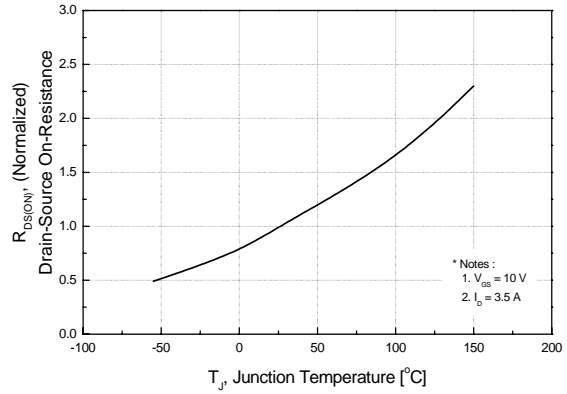


Figure 9. Maximum Safe Operating Area

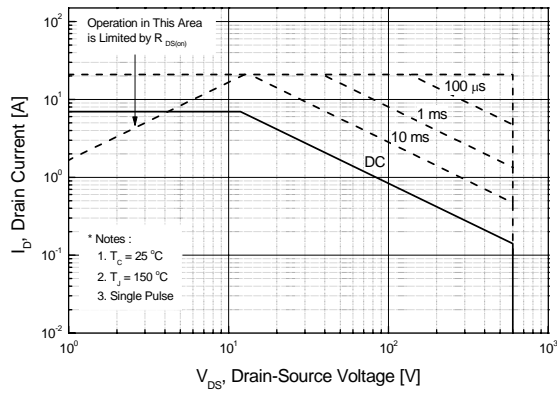


Figure 10. Maximum Drain Current vs. Case Temperature

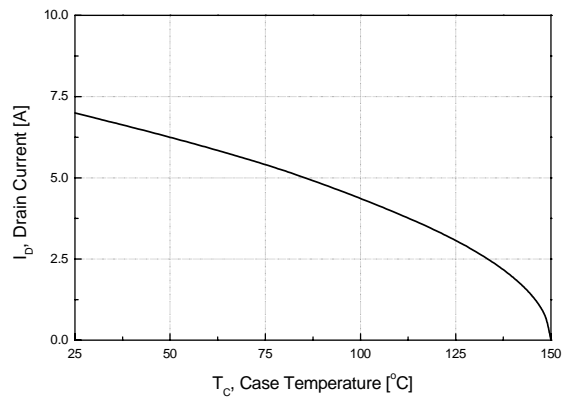
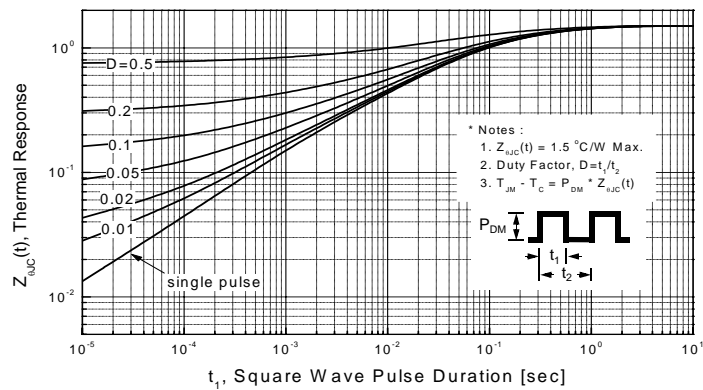
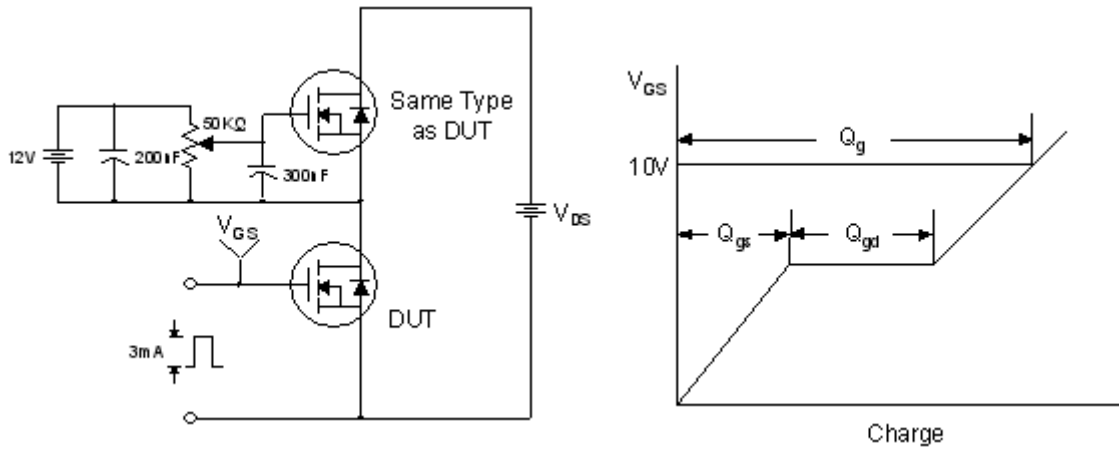


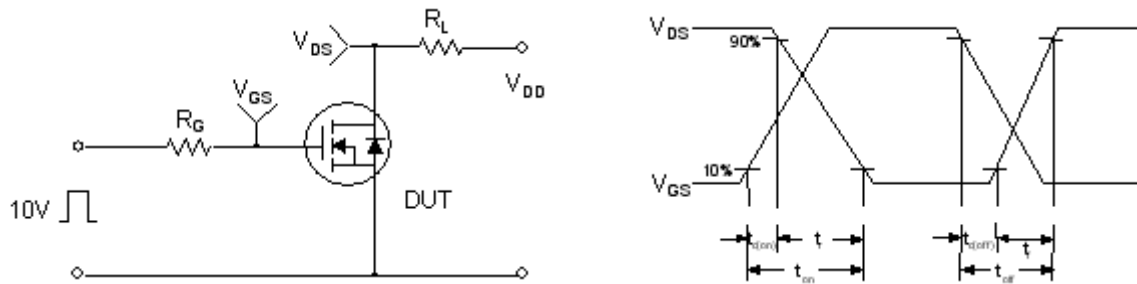
Figure 11. Transient Thermal Response Curve



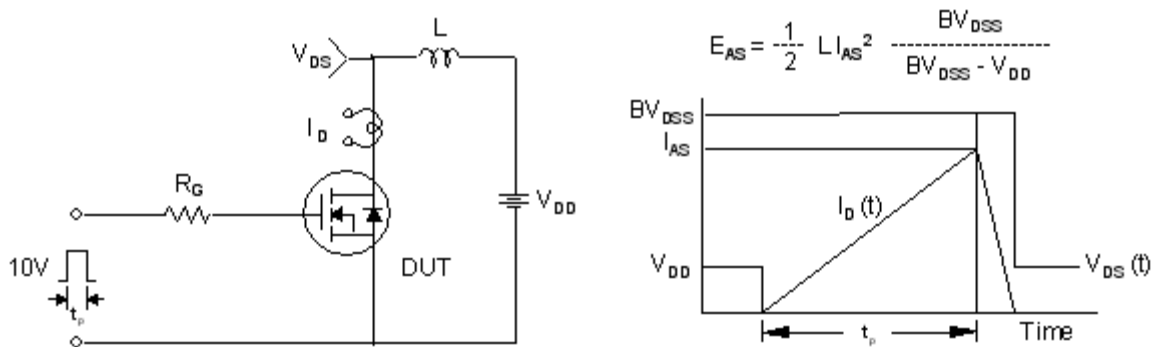
Gate Charge Test Circuit & Waveform



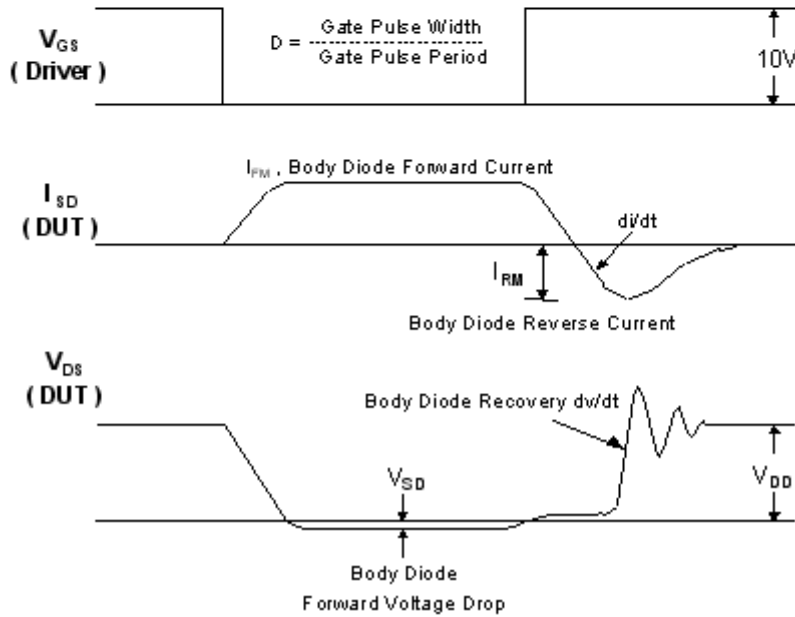
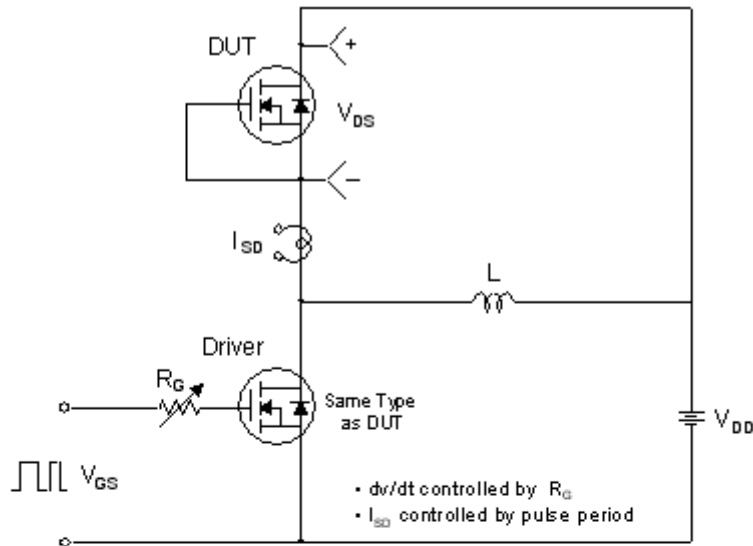
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

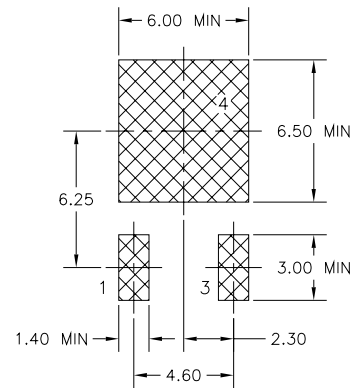
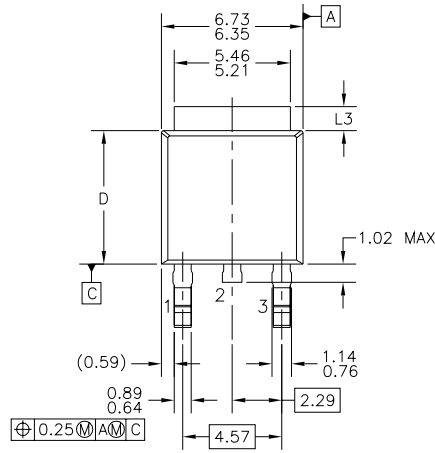


Peak Diode Recovery dv/dt Test Circuit & Waveforms

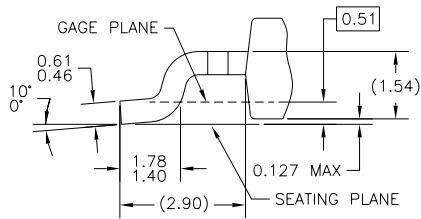
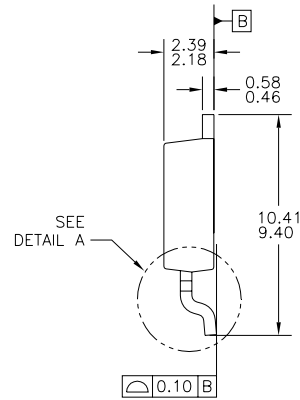
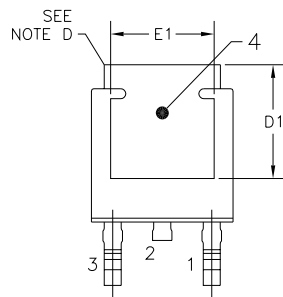


Mechanical Dimensions

D-PAK



LAND PATTERN RECOMMENDATION



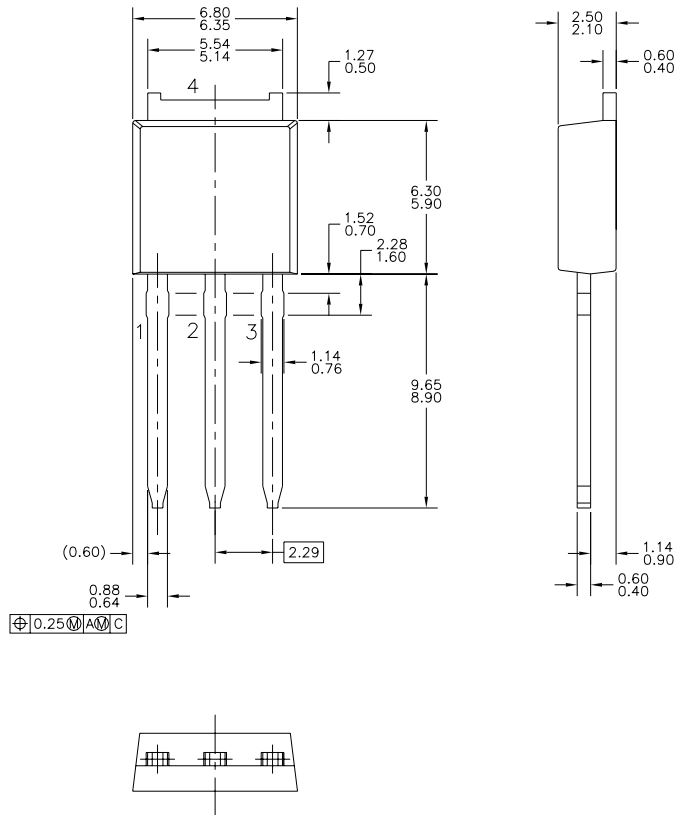
DETAIL A
(ROTATED -90°)
SCALE: 12X

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) DIMENSIONS L3, D, E1 & D1 TABLE:
- | | OPTION AA | OPTION AB |
|----|-----------|-----------|
| L3 | 0.89-1.27 | 1.52-2.03 |
| D | 5.97-6.22 | 5.33-5.59 |
| E1 | 4.32 MIN | 3.81 MIN |
| D1 | 5.21 MIN | 4.57 MIN |
- F) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Dimensions in Millimeters

Package Dimensions (Continued)

I-PAK



Dimensions in Millimeters



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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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