

FDB088N08

N-Channel PowerTrench® MOSFET

75V, 85A, 8.8mΩ

Features

- $R_{DS(on)} = 7.3 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10V, I_D = 75A$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- 100% Internal Rg Screening for Easy Paralleling Operation
- RoHS Compliant

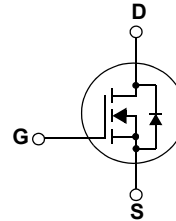
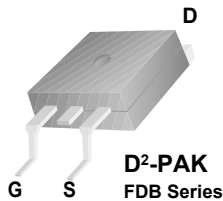


Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Application

- DC to DC Convertors / Synchronous Rectification



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted*

Symbol	Parameter	FDB088N08	Units
V_{DSS}	Drain to Source Voltage	75	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$, Silicon Limited)	85*
		- Continuous ($T_C = 100^\circ\text{C}$, Silicon Limited)	60
		- Continuous ($T_C = 25^\circ\text{C}$, Package Limited)	120
I_{DM}	Drain Current - Pulsed (Note 1)	340	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	309	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	10	V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	160
		- Derate above 25°C	1.06
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A.

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.94	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

Package Marking and Ordering Information $T_C = 25^\circ\text{C}$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB088N08	FDB088N08	D2-PAK	330mm	24mm	800

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}, T_C = 25^\circ\text{C}$	75	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.07	-	$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 75\text{V}, V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 75\text{V}, T_C = 150^\circ\text{C}$	-	-	500	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 75\text{A}$	-	7.3	8.8	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 37.5\text{A}$ (Note 4)	-	300	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	4960	6595	pF
C_{oss}	Output Capacitance		-	355	470	pF
C_{rss}	Reverse Transfer Capacitance		-	200	300	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 60\text{V}, I_D = 75\text{A}$ $V_{GS} = 10\text{V}$ (Note 4, 5)	-	91	118	nC
Q_{gs}	Gate to Source Gate Charge		-	22	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	28	-	nC
R_G	Gate Resistance	$f = 1\text{MHz}$	-	-	4	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 37.5\text{V}, I_D = 75\text{A}$ $R_{GEN} = 25\Omega, V_{GS} = 10\text{V}$ (Note 4, 5)	-	45	100	ns
t_r	Turn-On Rise Time		-	158	326	ns
$t_{d(off)}$	Turn-Off Delay Time		-	244	498	ns
t_f	Turn-Off Fall Time		-	102	214	ns

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	85	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	340	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 75\text{A}$	-	-	1.25	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 75\text{A}$	-	41.1	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\text{A}/\mu\text{s}$ (Note 4)	-	80.7	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L = 0.11\text{mH}, I_{AS} = 75\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 75\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

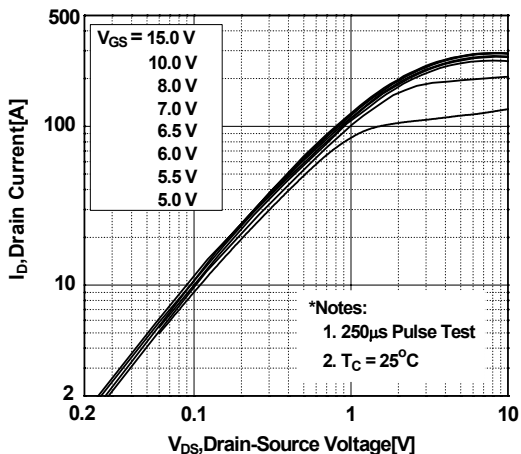


Figure 2. Transfer Characteristics

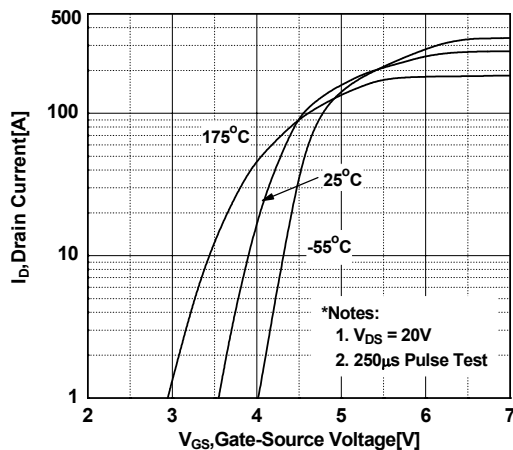


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

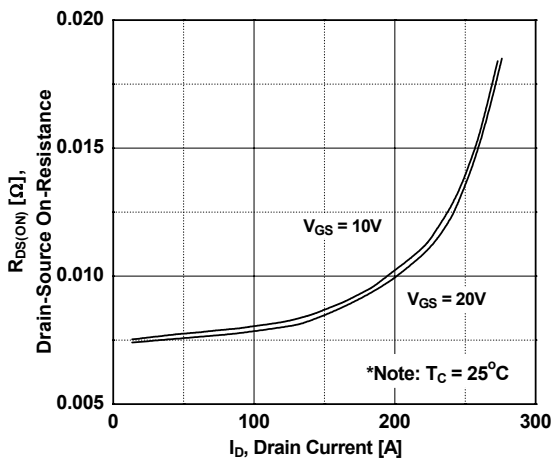


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

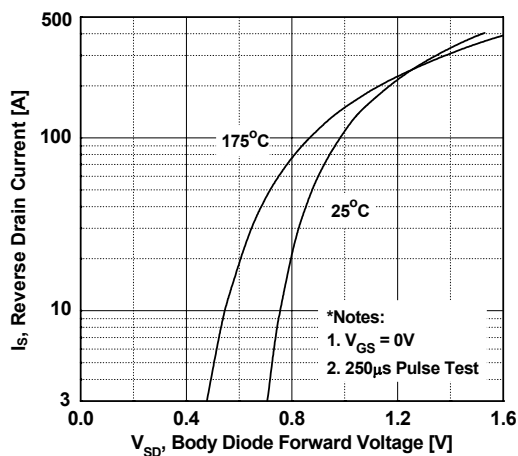


Figure 5. Capacitance Characteristics

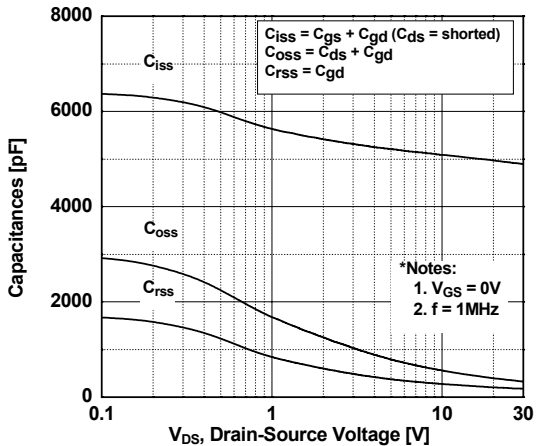
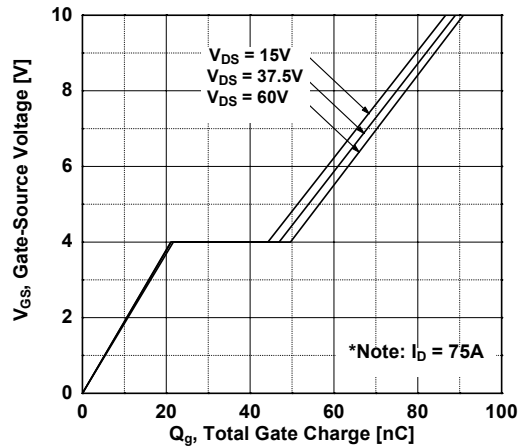


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

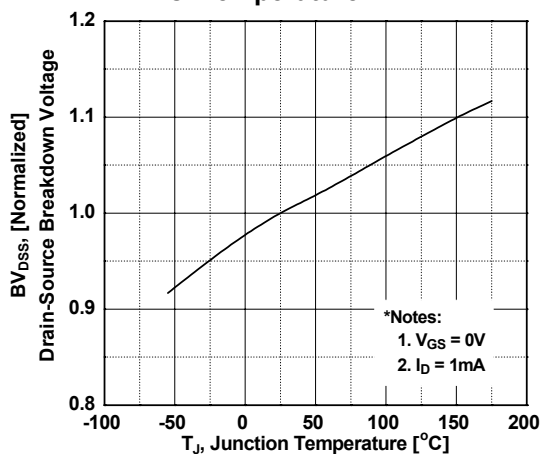


Figure 8. On-Resistance Variation vs. Temperature

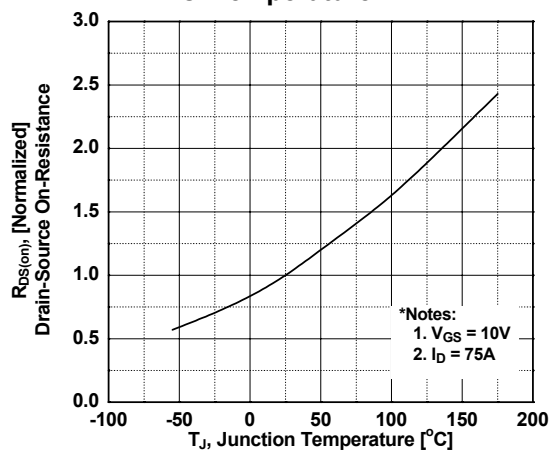


Figure 9. Maximum Safe Operating Area

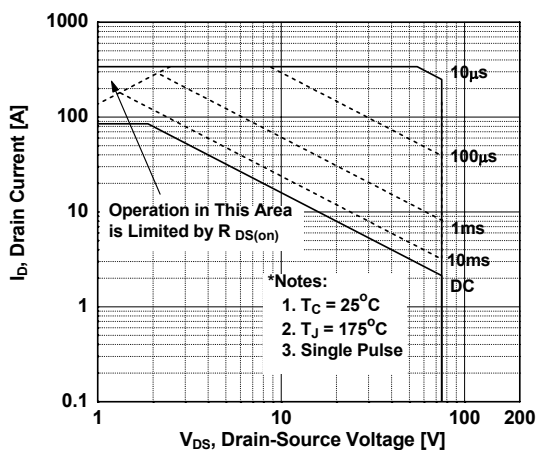


Figure 10. Maximum Drain Current vs. Case Temperature

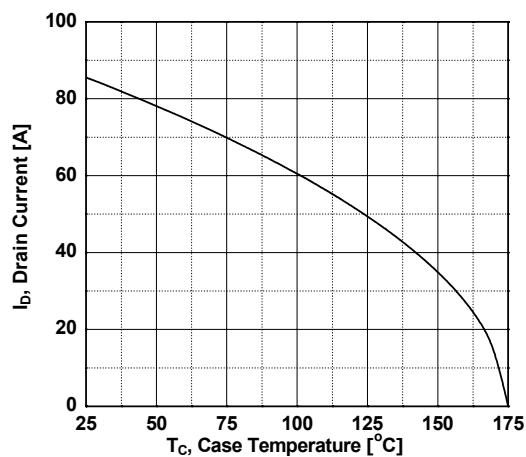
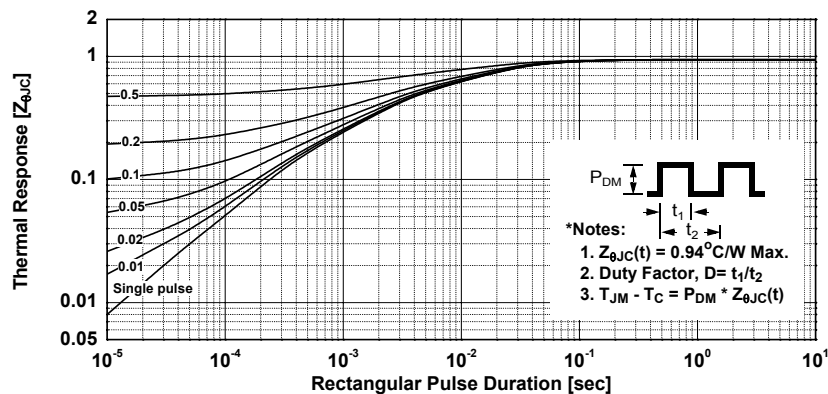
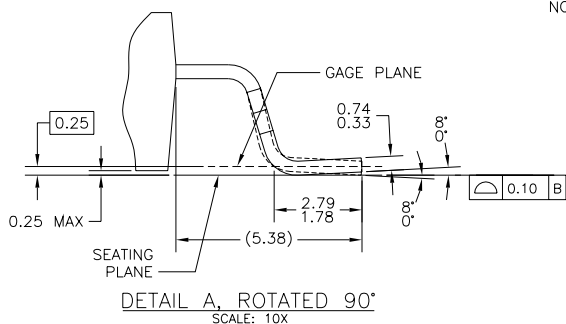
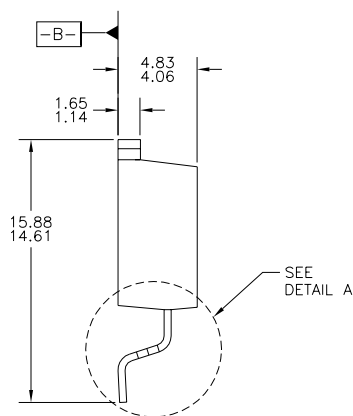
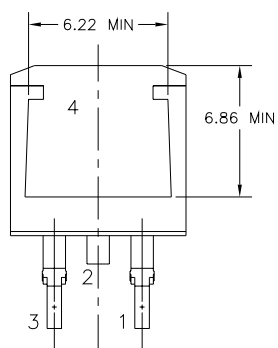
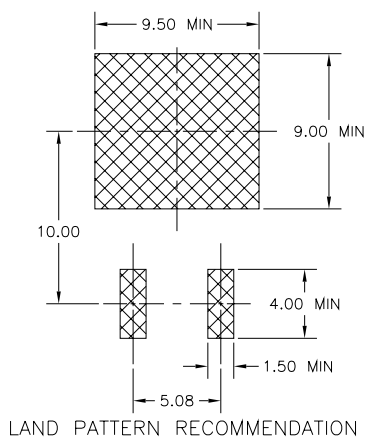
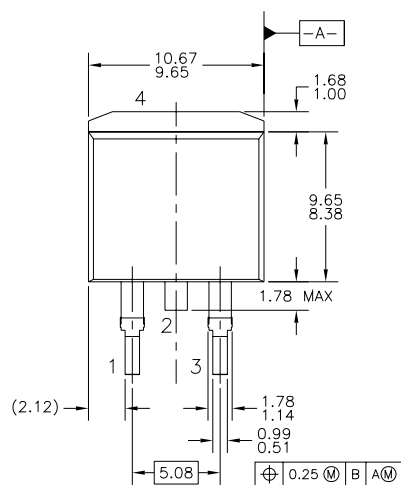


Figure 11. Transient Thermal Response Curve



Mechanical Dimensions

D2-PAK



- NOTES: UNLESS OTHERWISE SPECIFIED
- ALL DIMENSIONS ARE IN MILLIMETERS.
 - REFERENCE JEDEC, TO-263, ISSUE D, VARIATION AB, DATED JULY 2003.
 - DIMENSIONING AND TOLERANCING PER ANSI Y14.5M - 1982.
 - LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
 - PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

T0263A02REVD

Dimensions in Millimeters



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