

**40V DUAL P-CHANNEL ENHANCEMENT MODE MOSFET**

**Product Summary**

$V_{(BR)DSS}$	$R_{DS(on) Max}$	$I_D$ $T_A = 25^\circ C$ (Notes 4 & 6)
-40V	50mΩ @ $V_{GS} = -10V$	-5.2A
	79mΩ @ $V_{GS} = -4.5V$	-4.1A

**Description and Applications**

This MOSFET has been designed to minimize the on-state resistance and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

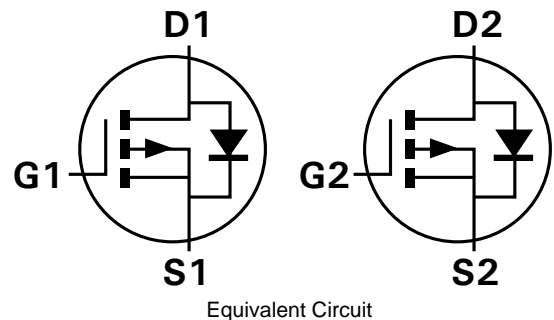
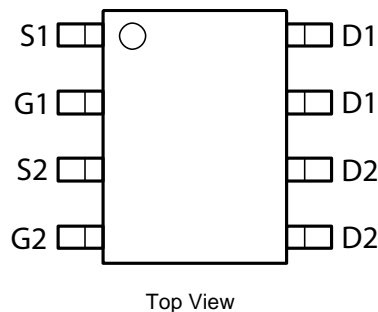
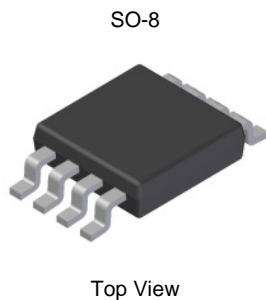
- Motor control
- Backlighting
- DC-DC Converters
- Power management functions

**Features and Benefits**

- Low on-resistance
- Fast switching speed
- “Lead-Free”, RoHS Compliant (Note 1)
- Halogen and Antimony Free, “Green” Device (Note 1)
- Qualified to AEC-Q101 Standards for High Reliability

**Mechanical Data**

- Case: SO-8
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0 (Note 1)
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See diagram below
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208
- Weight: 0.074 grams (approximate)

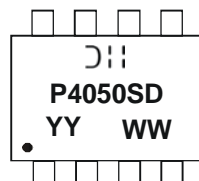


**Ordering Information** (Note 1)

Product	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
DMP4050SSD-13	P4050SD	13	12	2,500

Note: 1. Diodes, Inc. defines “Green” products as those which are RoHS compliant and contain no halogens or antimony compounds; further information about Diodes Inc.’s “Green” Policy can be found on our website. For packaging details, go to our website.

**Marking Information**



D = Manufacturer's Marking  
P4050SD = Product Type Marking Code  
YYWW = Date Code Marking  
YY = Year (ex: 09 = 2009)  
WW = Week (01-53)

**Maximum Ratings** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

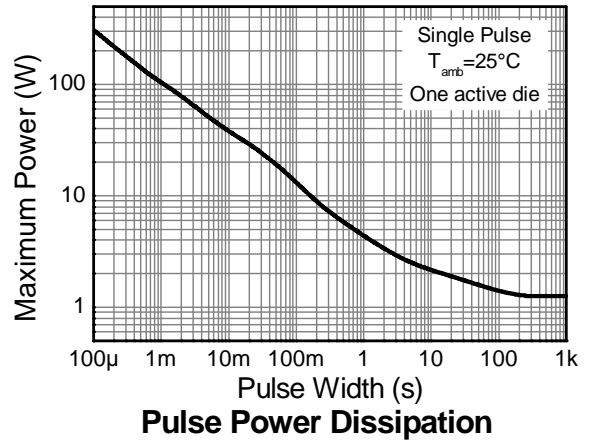
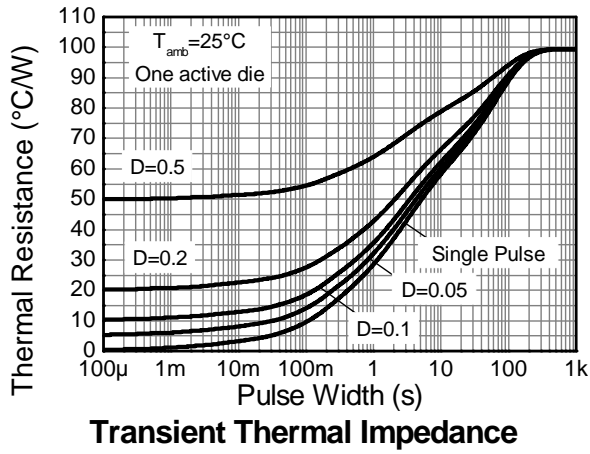
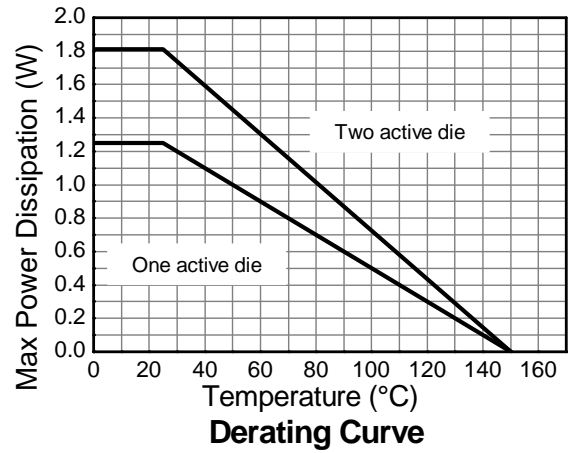
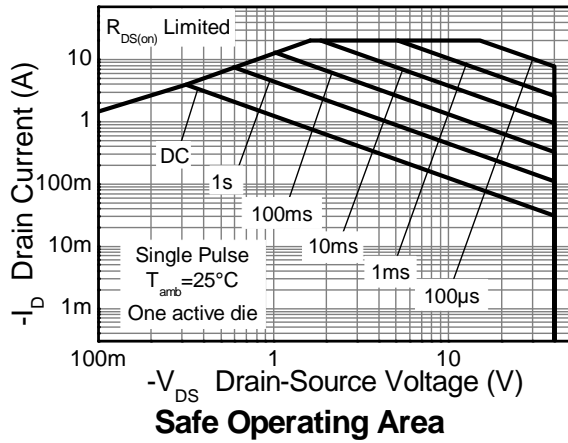
Characteristic			Symbol	Value	Unit
Drain-Source voltage			$V_{DSS}$	-40	V
Gate-Source voltage			$V_{GS}$	$\pm 20$	V
Continuous Drain current	$V_{GS} = 10\text{V}$	(Notes 4 & 6)	$I_D$	-5.2	A
		$T_A = 70^\circ\text{C}$ (Notes 4 & 6)		-4.2	
		(Notes 3 & 6)		-4.0	
Pulsed Drain current	$V_{GS} = 10\text{V}$	(Notes 5 & 6)	$I_{DM}$	-20.0	A
Continuous Source current (Body diode)			$I_S$	-3.2	A
Pulsed Source current (Body diode)			$I_{SM}$	-20.0	A

**Thermal Characteristics** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

Characteristic		Symbol	Value	Unit
Power dissipation Linear derating factor	(Notes 3 & 6)	$P_D$	1.25	W mW/ $^\circ\text{C}$
			10.0	
	(Notes 3 & 7)		1.8	
	(Notes 4 & 6)		14.3	
Thermal Resistance, Junction to Ambient	(Notes 3 & 6)	$R_{\theta JA}$	2.14	$^\circ\text{C/W}$
	(Notes 3 & 7)		17.2	
	(Notes 4 & 6)		100	
Thermal Resistance, Junction to Lead	(Notes 3 & 7)	$R_{\theta JL}$	70	$^\circ\text{C/W}$
	(Notes 4 & 6)		58	
Operating and storage temperature range		$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

- Notes:
- AEC-Q101  $V_{GS}$  maximum is  $\pm 16\text{V}$ .
  - For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
  - Same as note (3), except the device is measured at  $t \leq 10$  sec.
  - Same as note (3), except the device is pulsed with  $D = 0.02$  and pulse width 300 $\mu\text{s}$ . The pulse current is limited by the maximum junction temperature.
  - For a dual device with one active die.
  - For a device with two active die running at equal power.
  - Thermal resistance from junction to solder-point (at the end of the drain lead).

**Thermal Characteristics**

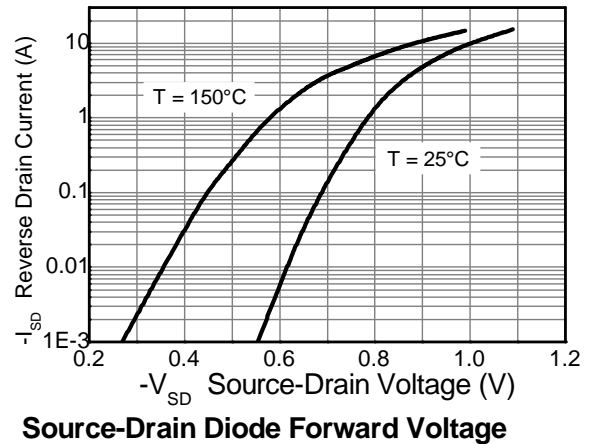
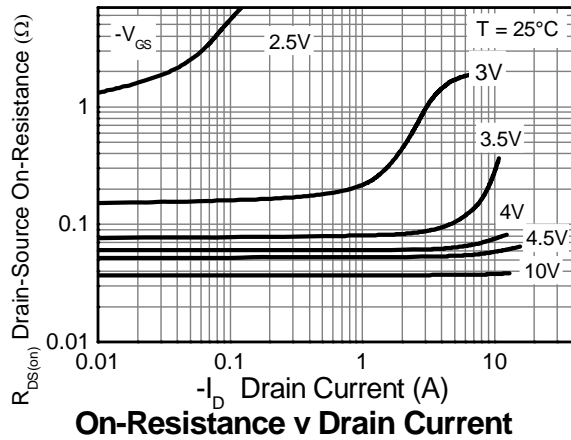
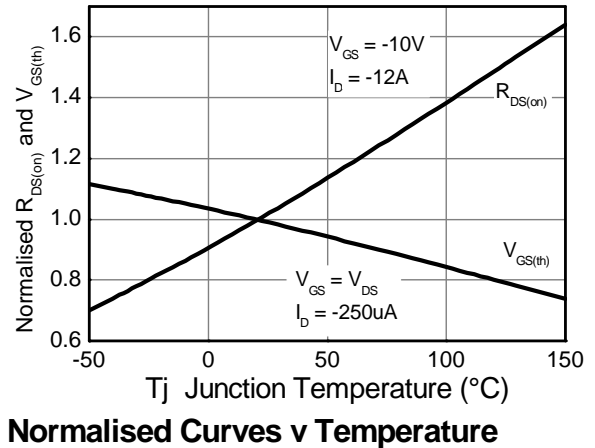
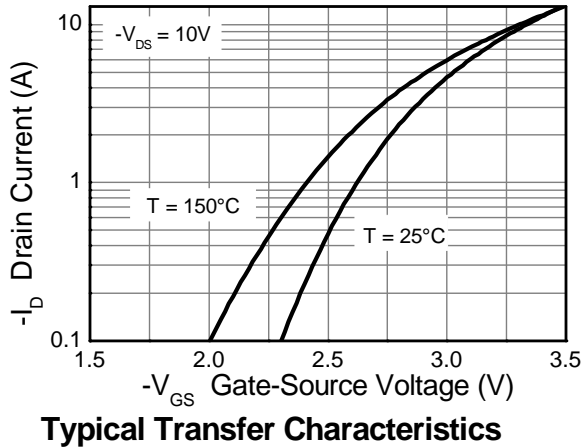
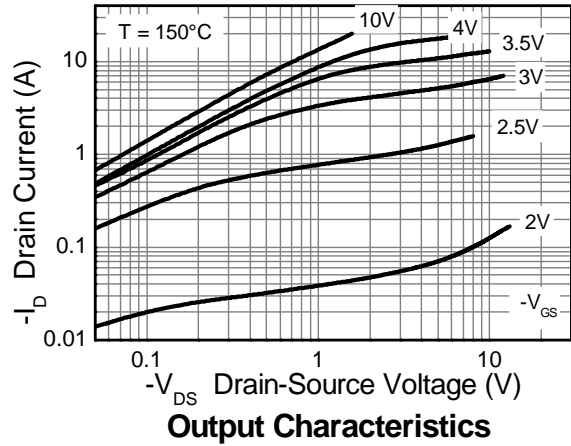
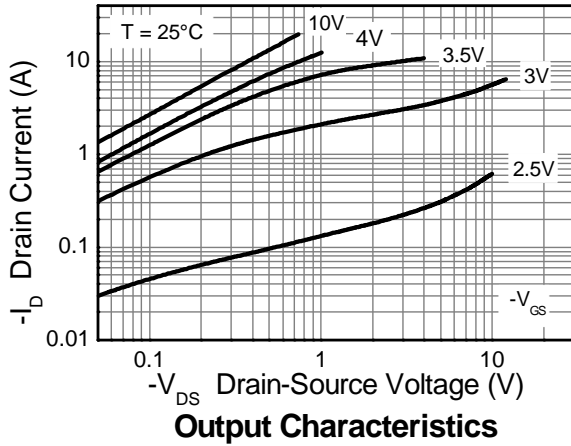


**Electrical Characteristics** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

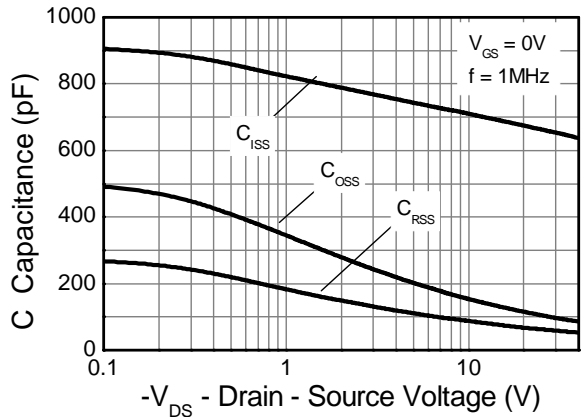
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	-40	—	—	V	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$
Zero Gate Voltage Drain Current	$I_{DSS}$	—	—	-0.5	$\mu\text{A}$	$V_{DS} = -40\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	$I_{GSS}$	—	—	$\pm 100$	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(th)}$	-1.0	—	-3.0	V	$I_D = -250\mu\text{A}, V_{DS} = V_{GS}$
Static Drain-Source On-Resistance (Note 9)	$R_{DS(on)}$	—	0.038	0.050	$\Omega$	$V_{GS} = -10\text{V}, I_D = -6\text{A}$
			0.055	0.079		$V_{GS} = -4.5\text{V}, I_D = -5\text{A}$
Forward Transconductance (Notes 9 & 10)	$g_{fs}$	—	14	—	S	$V_{DS} = -15\text{V}, I_D = -6\text{A}$
Diode Forward Voltage (Note 9)	$V_{SD}$	—	-0.86	-1.2	V	$I_S = -6\text{A}, V_{GS} = 0\text{V}$
Reverse recovery time (Note 10)	$t_{rr}$	—	18	—	ns	$I_S = -2\text{A}, di/dt = 100\text{A}/\mu\text{s}$
Reverse recovery charge (Note 10)	$Q_{rr}$	—	12.7	—	nC	
<b>DYNAMIC CHARACTERISTICS (Note 10)</b>						
Input Capacitance	$C_{iss}$	—	674	—	pF	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output Capacitance	$C_{oss}$	—	115	—	pF	
Reverse Transfer Capacitance	$C_{rss}$	—	67.7	—	pF	
Total Gate Charge (Note 11)	$Q_g$	—	6.9	—	nC	$V_{GS} = -4.5\text{V}$
Total Gate Charge (Note 11)	$Q_g$	—	13.9	—	nC	$V_{GS} = -10\text{V}$
Gate-Source Charge (Note 11)	$Q_{gs}$	—	2	—	nC	
Gate-Drain Charge (Note 11)	$Q_{gd}$	—	3.4	—	nC	
Turn-On Delay Time (Note 11)	$t_{D(on)}$	—	1.9	—	ns	$V_{DD} = -20\text{V}, V_{GS} = -10\text{V}$ $I_D = -1\text{A}, R_G \cong 6.0\Omega$
Turn-On Rise Time (Note 11)	$t_r$	—	3.1	—	ns	
Turn-Off Delay Time (Note 11)	$t_{D(off)}$	—	31.5	—	ns	
Turn-Off Fall Time (Note 11)	$t_f$	—	12.6	—	ns	

- Notes:
9. Measured under pulsed conditions. Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$
  10. For design aid only, not subject to production testing.
  11. Switching characteristics are independent of operating junction temperatures.

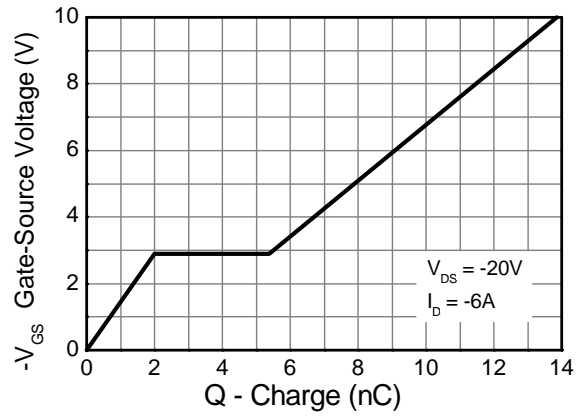
**Typical Characteristics**



**Typical Characteristics - continued**

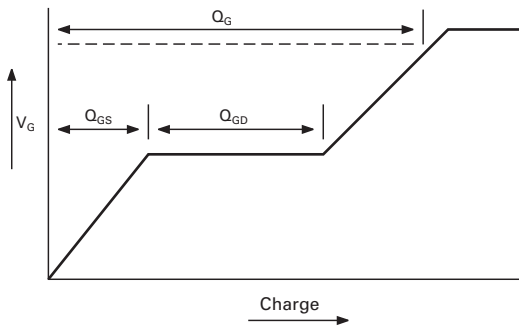


**Capacitance v Drain-Source Voltage**

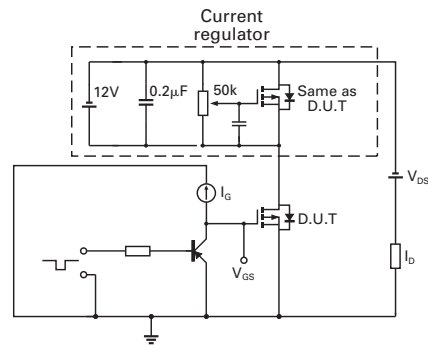


**Gate-Source Voltage v Gate Charge**

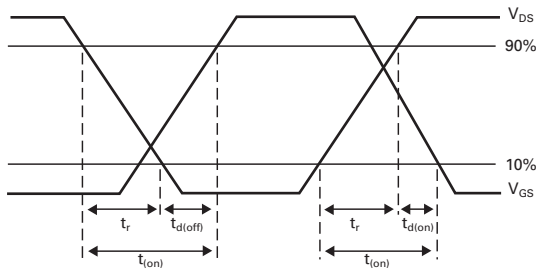
**Test Circuits**



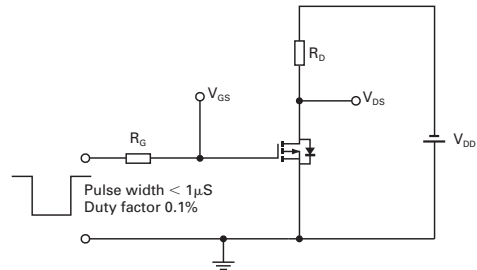
**Basic gate charge waveform**



**Gate charge test circuit**

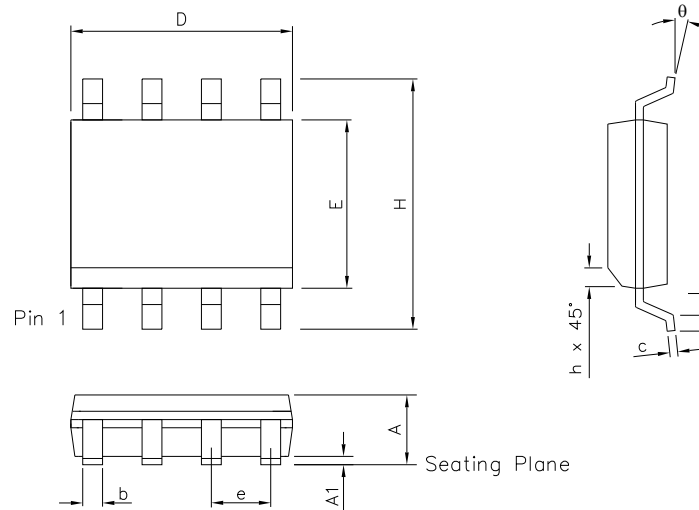


**Switching time waveforms**



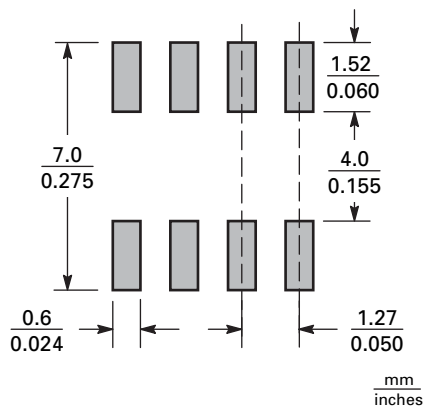
**Switching time test circuit**

**Package Outline Dimensions**



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75	e	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	c	0.008	0.010	0.19	0.25
H	0.228	0.244	5.80	6.20	theta	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27	-	-	-	-	-

**Suggested Pad Layout**



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