Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D T_A = 25°C
-12V	102mΩ @ V_{GS} = -4.5V	-2.6A
	116mΩ @ V_{GS} = -2.5V	-2.4A

Description and Applications

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Battery Management
- Load Switch
- Battery Protection

Features and Benefits

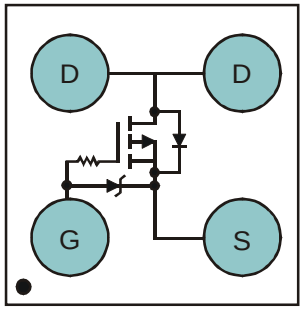
- Low Q_g & Q_{gd}
- Small Footprint
- Low Profile 0.62mm height
- **ESD Protected Up To 3KV**
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: WL-CSP1010H6-4
- Terminal Connections: See Diagram Below
- Weight: 0.005 grams (approximate)

WL-CSP1010H6-4

ESD PROTECTED TO 3kV



Top View
Equivalent Circuit

Ordering Information (Note 3)

Part Number	Case	Packaging
DMP1096UCB4-7	WL-CSP1010H6-4	3000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com.

Marking Information

1W = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: X = 2010)
M = Month (ex: 9 = September)

BW = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: X = 2010)
M = Month (ex: 9 = September)

Date Code Key

Year	2010	2011	2012	2013	2014	2015	2016
Code	X	Y	Z	A	B	C	D

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings @T_A = 25°C unless otherwise specified

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-12	V
Gate-Source Voltage			V_{GSS}	-5	V
Continuous Drain Current (Note 5) V_{GS} = -4.5V	Steady State	T_A = 25°C T_A = 70°C	I_D	-2.6 -2.1	A
Continuous Drain Current (Note 5) V_{GS} = -2.5V	Steady State	T_A = 25°C T_A = 70°C	I_D	-2.4 -1.9	A
Pulsed Drain Current (Note 6)			I_{DM}	-10	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P_D	0.82	W
Thermal Resistance, Junction to Ambient @T_A = 25°C (Note 5)	$R_{\theta JA}$	150	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-12	-	-	V	V_{GS} = 0V, I_D = -250µA
Gate-Source Breakdown Voltage	BV_{GSS}	-6.0	-	-7.0	V	V_{DS} = 0V, I_G = -250µA
Zero Gate Voltage Drain Current T_J = 25°C	I_{DSS}	-	-	-1	µA	V_{DS} = -9.6V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	-	-	-500	nA	V_{GS} = -5V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	-0.4	-0.6	-1.0	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	-	85	102	mΩ	V_{GS} = -4.5V, I_D = -500mA
		-	97	116		V_{GS} = -2.5V, I_D = -500mA
		-	127	152		V_{GS} = -1.5V, I_D = -500mA
Forward Transfer Admittance	$\|Y_{fs}\|$	-	4	-	S	V_{DS} = -6V, I_D = -500mA
Diode Forward Voltage	V_{SD}		-0.6	-1.0	V	V_{GS} = 0V, I_S = -500mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	-	251	-	pF	V_{DS} = -6V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	-	359	-		
Reverse Transfer Capacitance	C_{rss}	-	70	-		
Total Gate Charge	Q_g	-	3.7	-	nC	V_{GS} = -4.5V, V_{DS} = -6V, I_D = -500mA
Gate-Source Charge	Q_{gs}	-	0.4	-		
Gate-Drain Charge	Q_{gd}	-	0.6	-		
Gate Charge at Vth	$Q_{g(th)}$	-	0.2	-		
Turn-On Delay Time	$t_{D(on)}$	-	17.6	-	ns	V_{DS} = -6V, V_{GS} = -2.5V, R_G = 20Ω, I_D = -500mA
Turn-On Rise Time	t_r	-	26.9	-		
Turn-Off Delay Time	$t_{D(off)}$	-	37.5	-		
Turn-Off Fall Time	t_f	-	32.3	-		

Notes: 5. Device mounted on FR-4 PCB with minimum recommended pad layout, single sided.
6. Repetitive rating, pulse width limited by junction temperature.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

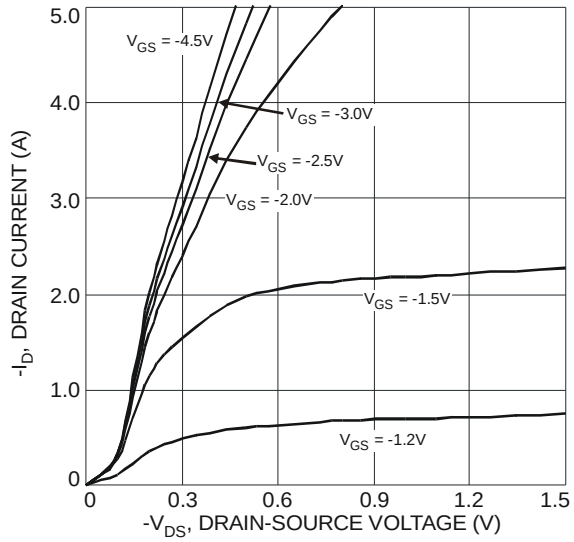


Fig. 1 Typical Output Characteristic

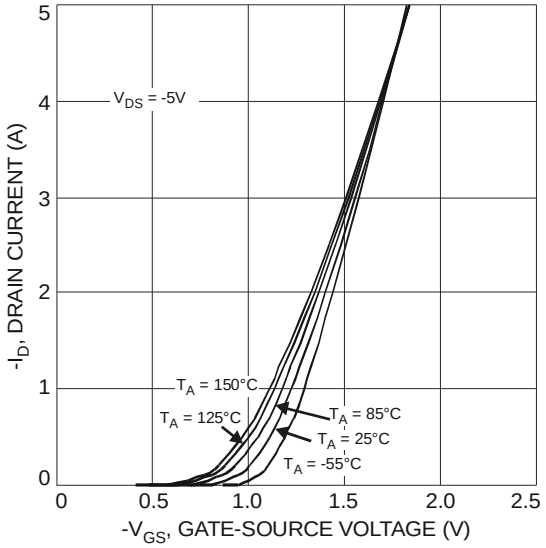


Fig. 2 Typical Transfer Characteristic

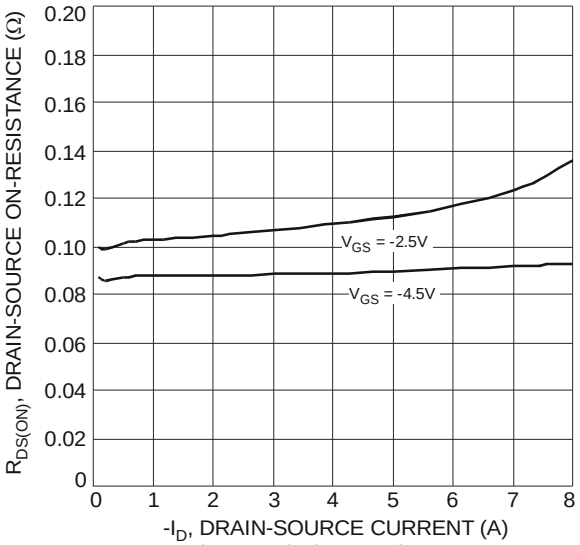


Fig. 3 Typical On-Resistance
vs. Drain Current and Gate Voltage

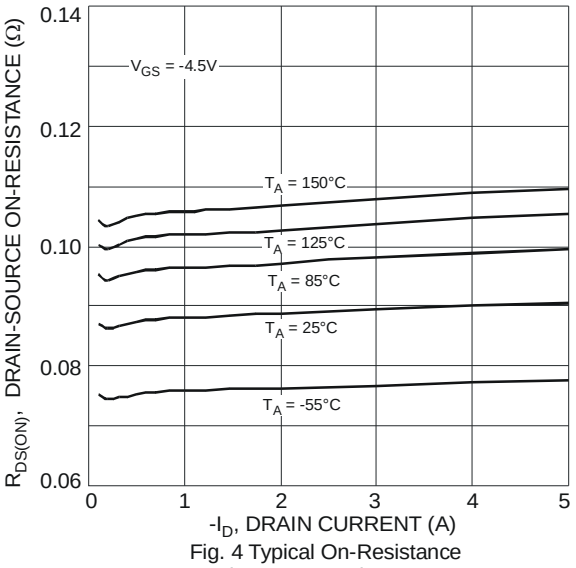


Fig. 4 Typical On-Resistance
vs. Drain Current and Temperature

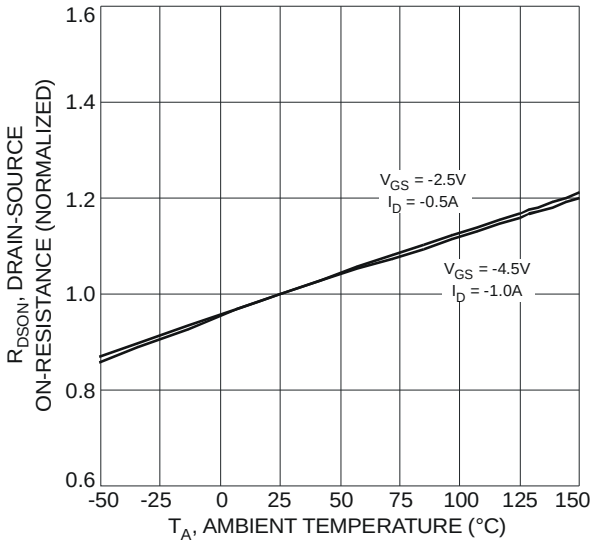


Fig. 5 On-Resistance Variation with Temperature

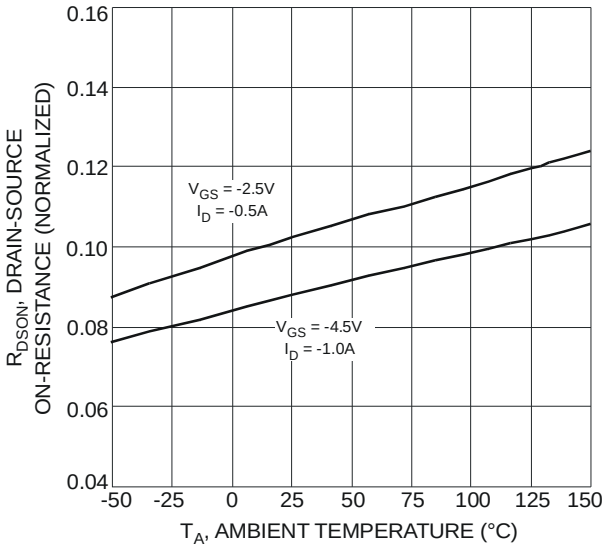


Fig. 6 On-Resistance Variation with Temperature

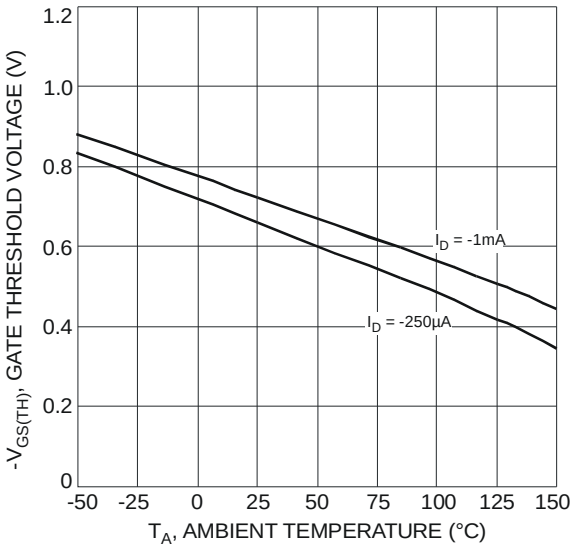


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

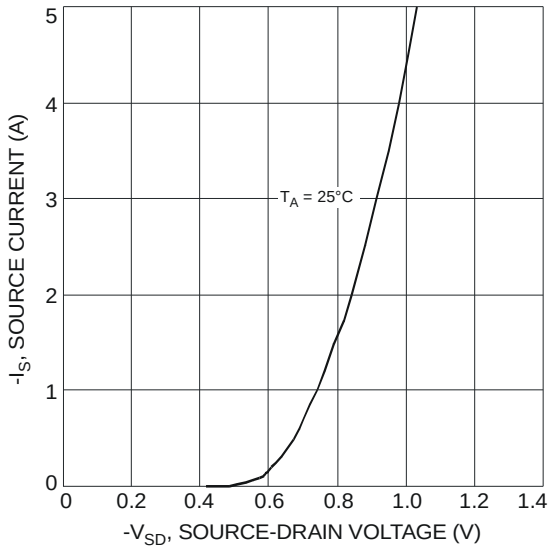


Fig. 8 Diode Forward Voltage vs. Current

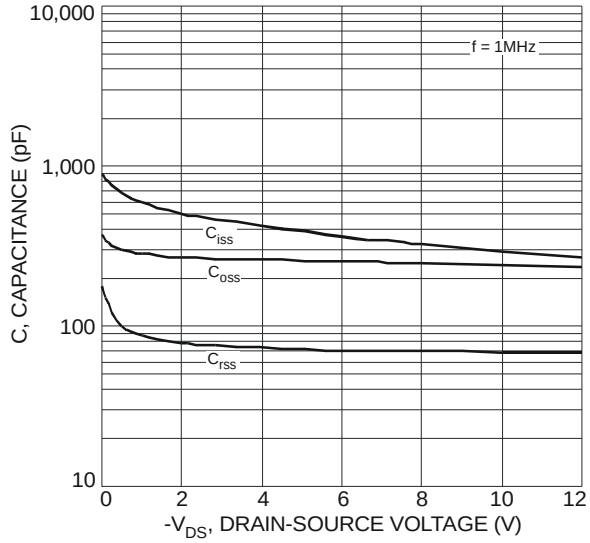


Fig. 9 Typical Total Capacitance

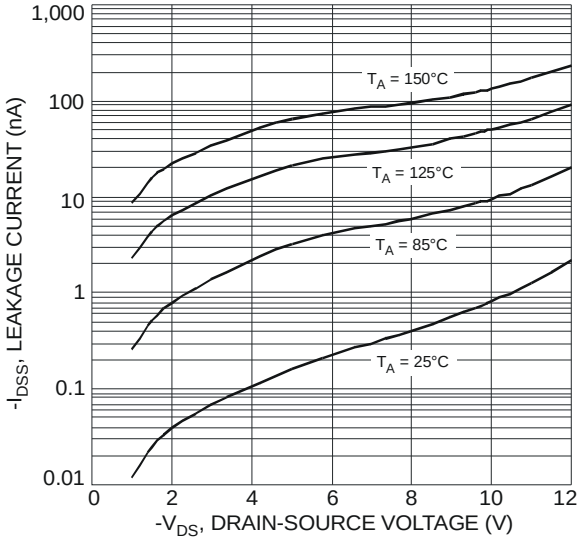


Fig. 10 Typical Leakage Current vs. Drain-Source Voltage

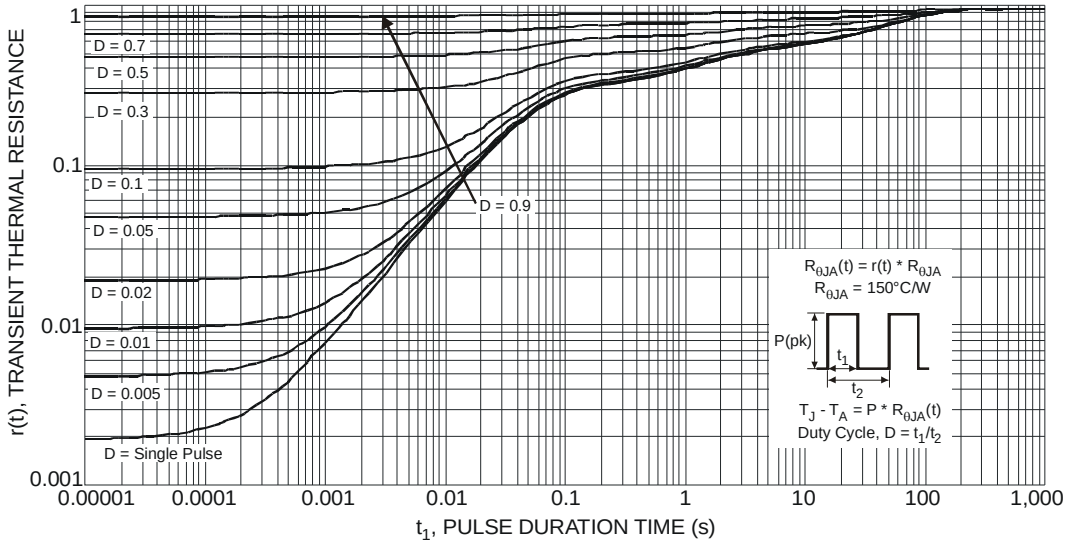
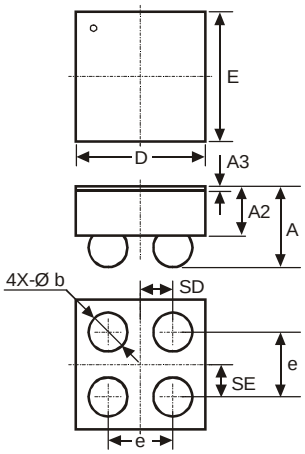


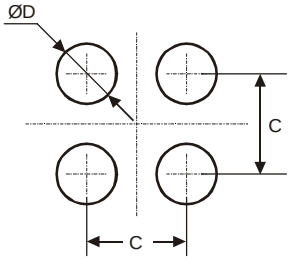
Fig. 11 Transient Thermal Response

Package Outline Dimensions



WL-CSP1010H6-4			
Dim	**Min**	**Max**	**Typ**
D	0.95	1.05	1.00
E	0.95	1.05	1.00
A	–	0.62	–
A2	–	–	0.38
A3	0.015	0.025	0.025
b	0.25	0.35	0.30
e	–	–	0.50
SD	–	–	0.25
SE	–	–	0.25
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
C	0.50
D	0.25

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