

#### N-CHANNEL ENHANCEMENT MODE MOSFET

## **Product Summary**

V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub>	I <sub>D</sub> T <sub>A</sub> = 25°C
-0.7	2.0Ω @ V <sub>GS</sub> = 5.0V	300 mA
50V	2.5Ω @ V <sub>GS</sub> = 2.5V	200 mA

### **Features and Benefits**

- Low On-Resistance
- Very Low Gate Threshold Voltage (1.0V max)
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- ESD Protected Up To 2kV
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 standards for High Reliability

### **Description and Applications**

This new generation 50V N-Channel Enhancement Mode MOSFET has been designed to minimize RDS(on) and yet maintain superior switching performance. This device is ideal for use in Notebook battery power management and Load switch.

- Load switchs
- Level switchs

### **Mechanical Data**

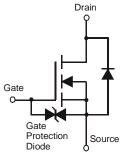
- Case: SOT23
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish Matte Tin annealed over Alloy 42 leadframe.
   Solderable per MIL-STD-202, Method 208
- Terminal Connections: See Diagram
- Weight: 0.008 grams (approximate)



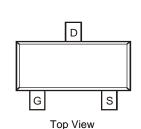


SOT23

Top View







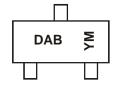
### Ordering Information (Note 4)

Part Number	Qualification	Case	Packaging
DMN5L06K-7	Commercial	SOT23	3000/Tape & Reel
DMN5L06KQ-7	Automotive	SOT23	3000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com

# **Marking Information**



DAB = Product Type Marking Code YM = Date Code Marking Y = Year (ex: T = 2006) M = Month (ex: 9 = September)

Date Code Key

Year	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017
Code	T	U	V	W	X	Y	Z	Α	В	C	D	E
Marrit				_								
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec



## Maximum Ratings @TA = 25°C unless otherwise specified

Charac	teristic	Symbol	Value	Unit
Drain Source Voltage		$V_{DSS}$	50	V
Gate-Source Voltage		$V_{GSS}$	±20	V
Drain Current (Note 5)	Continuous Pulsed (Note 6)	I <sub>D</sub>	300 800	mA

## **Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	$P_{D}$	350	mW
Thermal Resistance, Junction to Ambient	$R_{ hetaJA}$	357	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-65 to +150	°C

# **Electrical Characteristics** @ T<sub>A</sub> = 25°C unless otherwise stated

Characteristic		Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage		BV <sub>DSS</sub>	50		_	V	$V_{GS} = 0V, I_D = 10\mu A$
Zero Gate Voltage Drain Current	@ $T_C = 25^{\circ}C$	I <sub>DSS</sub>	_		60	nA	$V_{DS} = 50V, V_{GS} = 0V$
					1	μΑ	$V_{GS} = \pm 12V$ , $V_{DS} = 0V$
Gate-Body Leakage		IGSS	_	_	500	nA	$V_{GS} = \pm 10V$ , $V_{DS} = 0V$
					50	nA	$V_{GS} = \pm 5V$ , $V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage		$V_{GS(th)}$	0.49	_	1.0	V	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$
			_		3.0		$V_{GS} = 1.8V, I_D = 50mA$
Static Drain-Source On-Resistance		R <sub>DS(ON)</sub>	_	_	2.5	Ω	$V_{GS} = 2.5V, I_D = 50mA$
			_		2.0		$V_{GS} = 5.0V, I_D = 50mA$
On-State Drain Current		I <sub>D(ON)</sub>	0.5	1.4	_	Α	$V_{GS} = 10V, V_{DS} = 7.5V$
Forward Transconductance		Y <sub>fs</sub>	200	_	_	mS	$V_{DS} = 10V, I_{D} = 0.2A$
Source-Drain Diode Forward Voltage		$V_{SD}$	0.5	_	1.4	V	$V_{GS} = 0V, I_{S} = 115mA$
DYNAMIC CHARACTERISTICS							
Input Capacitance		C <sub>iss</sub>	_	_	50	pF	\\ 05\\\\\ 0\\
Output Capacitance		Coss	_		25	pF	$V_{DS} = 25V, V_{GS} = 0V$ f = 1.0MHz
Reverse Transfer Capacitance		C <sub>rss</sub>	_	_	5.0	pF	T = T.UIVIMZ

Notes:

- 5. Device mounted on FR-4 PCB
- 6. Pulse width ≤10mS, Duty Cycle ≤1%.
  7. Short duration pulse test used to minimize self-heating effect.

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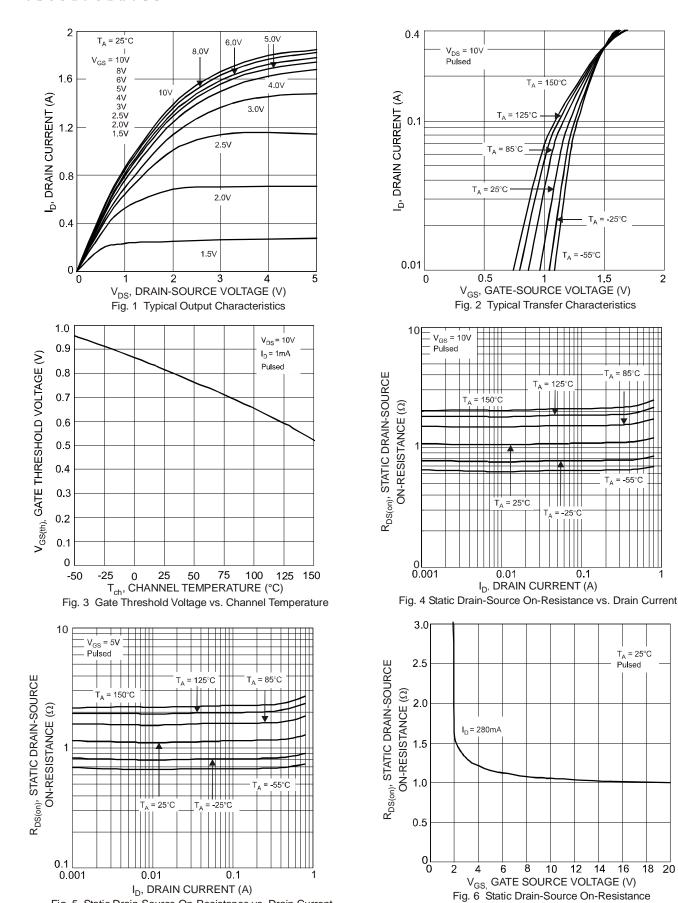


Fig. 5 Static Drain-Source On-Resistance vs. Drain Current

vs. Gate-Source Voltage



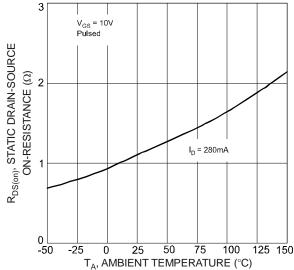


Fig. 7 Static Drain-Source On-State Resistance vs. Ambient Temperature

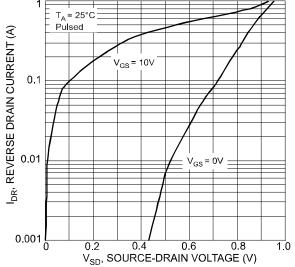
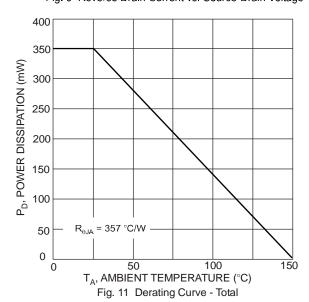


Fig. 9 Reverse Drain Current vs. Source-Drain Voltage



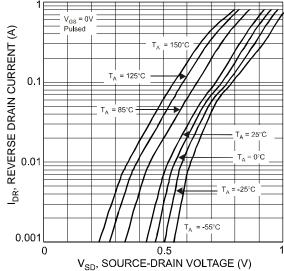


Fig. 8 Reverse Drain Current vs. Source-Drain Voltage

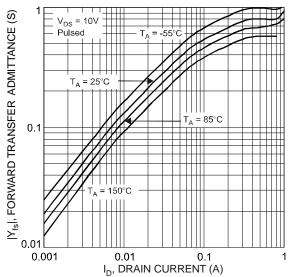
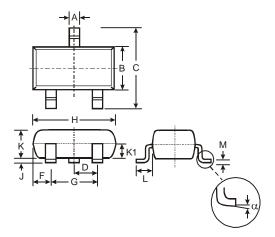


Fig.10 Forward Transfer Admittance vs. Drain Current

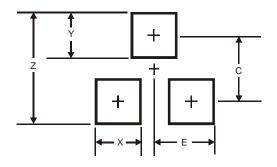


# **Package Outline Dimensions**



	SOT23						
Dim	Min	Max	Тур				
Α	0.37	0.51	0.40				
В	1.20	1.40	1.30				
С	2.30	2.50	2.40				
D	0.89	1.03	0.915				
F	0.45	0.60	0.535				
G	1.78	2.05	1.83				
Н	2.80	3.00	2.90				
J	0.013	0.10	0.05				
K	0.903	1.10	1.00				
K1	-	-	0.400				
L	0.45	0.61	0.55				
М	0.085	0.18	0.11				
α	0°	8°	-				
All Dimensions in mm							

# **Suggested Pad Layout**



Dimensions	Value (in mm)
Z	2.9
Х	0.8
Y	0.9
С	2.0
Е	1.35



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