

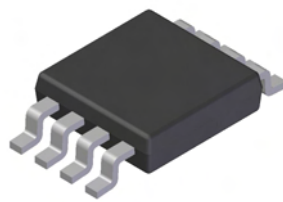
## Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$ max	$I_D$ max $T_A = 25^\circ\text{C}$ (Note 5)
40V	31m $\Omega$ @ $V_{GS} = 10\text{V}$	7.0A
	50m $\Omega$ @ $V_{GS} = 4.5\text{V}$	5.6A

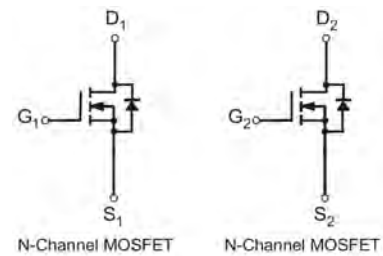
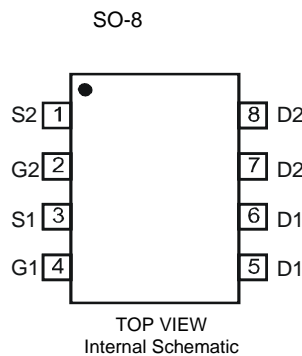
## Description and Applications

This MOSFET has been designed to minimize the on-state resistance ( $R_{DS(on)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Motor control
- Backlighting
- Power Management Functions
- DC-DC Converters



TOP VIEW



## Features and Benefits

- Low On-Resistance
- Low Input/Output Leakage
- **Lead Free By Design/RoHS Compliant (Note 1)**
- **"Green" Device (Note 2)**
- **Qualified to AEC-Q101 standards for High Reliability**

## Mechanical Data

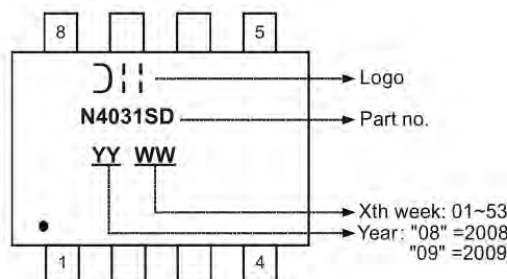
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See diagram
- Terminals: Finish — Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.072 grams (approximate)

## Ordering Information (Note 3)

Part Number	Case	Packaging
DMN4031SSD-13	SO-8	2500/Tape & Reel

- Notes:
1. No purposefully added lead.
  2. Diodes Inc.'s "Green" policy can be found on our website at <http://www.diodes.com>.
  3. For packaging details, go to our website at <http://www.diodes.com>.

## Marking Information



**Maximum Ratings** @T<sub>A</sub> = 25°C unless otherwise specified

Characteristic				Symbol	Value	Units
Drain-Source Voltage				V <sub>DSS</sub>	40	V
Gate-Source Voltage				V <sub>GSS</sub>	±20	V
Continuous Drain Current (Note 4)	V <sub>GS</sub> = 10V	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	5.2	A
			T <sub>A</sub> = 70°C		4.1	
Continuous Drain Current (Note 4)	V <sub>GS</sub> = 4.5V	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	4.3	A
			T <sub>A</sub> = 70°C		3.4	
Continuous Drain Current (Note 5)	V <sub>GS</sub> = 10V	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	7.0	A
			T <sub>A</sub> = 70°C		5.6	
Continuous Drain Current (Note 5)	V <sub>GS</sub> = 4.5V	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	5.8	A
			T <sub>A</sub> = 70°C		4.7	
Pulsed Drain Current (Note 6)				I <sub>DM</sub>	20	A

**Thermal Characteristics** @T<sub>A</sub> = 25°C unless otherwise specified

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 4)	P <sub>D</sub>	1.42	W
Thermal Resistance, Junction to Ambient @T <sub>A</sub> = 25°C (Note 4)	R <sub>θJA</sub>	88	°C/W
Total Power Dissipation (Note 5)	P <sub>D</sub>	2.6	W
Thermal Resistance, Junction to Ambient @T <sub>A</sub> = 25°C (Note 5)	R <sub>θJA</sub>	48	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** T<sub>A</sub> = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	40	-	-	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 10mA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	-	-	1	µA	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	1.6	2.4	3.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250µA
On-state drain current	I <sub>D(ON)</sub>	20	-	-	A	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 5A
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	-	19	31	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 6A
		-	44	50		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 5A
Forward Transfer Admittance	Y <sub>fs</sub>	-	11	-	S	V <sub>DS</sub> = 5V, I <sub>D</sub> = 6A
Diode Forward Voltage	V <sub>SD</sub>	-	0.74	1.0	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 1A
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>iss</sub>	-	945	-	pF	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	-	69	-	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	-	58	-	pF	
Gate resistance	R <sub>g</sub>	-	1.45	-	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1.0MHz
Total Gate Charge (V <sub>GS</sub> = 4.5V)	Q <sub>g</sub>	-	8.4	-	nC	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 20V, I <sub>D</sub> = 12A
Total Gate Charge (V <sub>GS</sub> = 10V)	Q <sub>g</sub>	-	18.6	-	nC	
Gate-Source Charge	Q <sub>gs</sub>	-	3.3	-	nC	
Gate-Drain Charge	Q <sub>gd</sub>	-	2.2	-	nC	
Turn-On Delay Time	T <sub>D(on)</sub>	-	6.4	-	ns	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 20V, R <sub>L</sub> = 1.6Ω, R <sub>G</sub> = 3Ω
Turn-On Rise Time	T <sub>r</sub>	-	9.7	-	ns	
Turn-Off Delay Time	T <sub>D(off)</sub>	-	19.8	-	ns	
Turn-Off Fall Time	T <sub>f</sub>	-	3.1	-	ns	

- Notes:
- Device mounted on FR-4 PCB, with minimum recommended pad layout. The value in any given application depends on user's specific board design
  - Device mounted on 1" x 1" FR-4PCB with high coverage 1 oz. Copper, single sided.
  - Repetitive rating, pulse width limited by junction temperature.
  - Short duration pulse test used to minimize self-heating effect
  - Guaranteed by design. No subject to production testing.

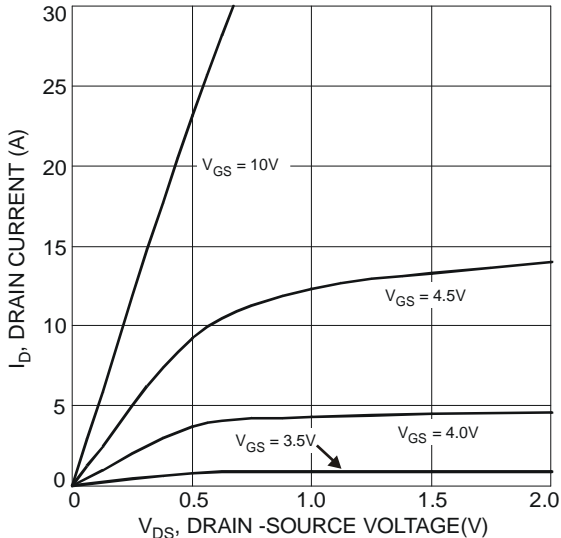


Fig. 1 Typical Output Characteristics

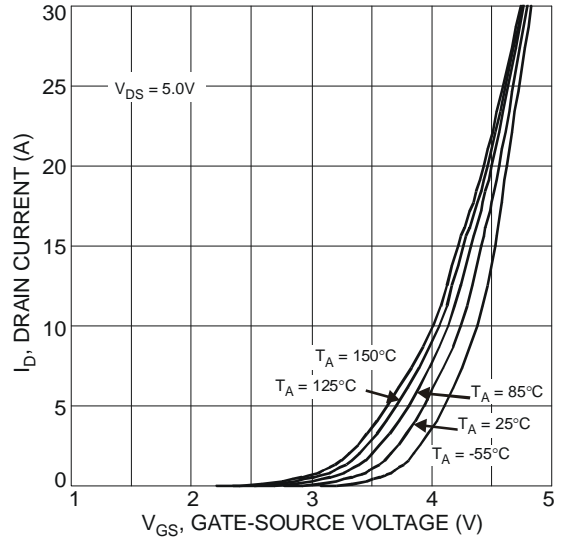


Fig. 2 Typical Transfer Characteristics

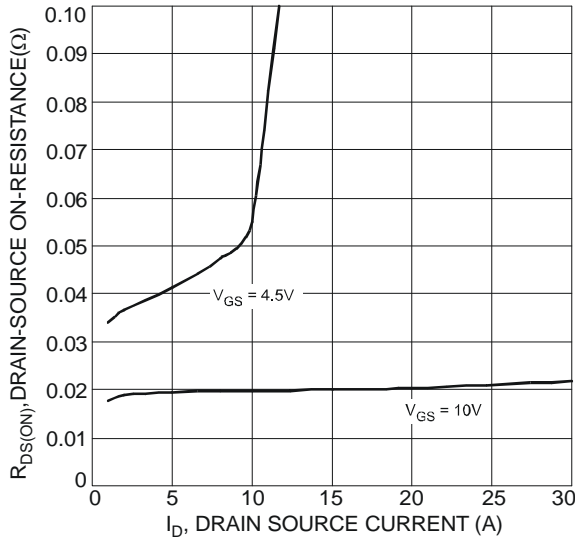


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

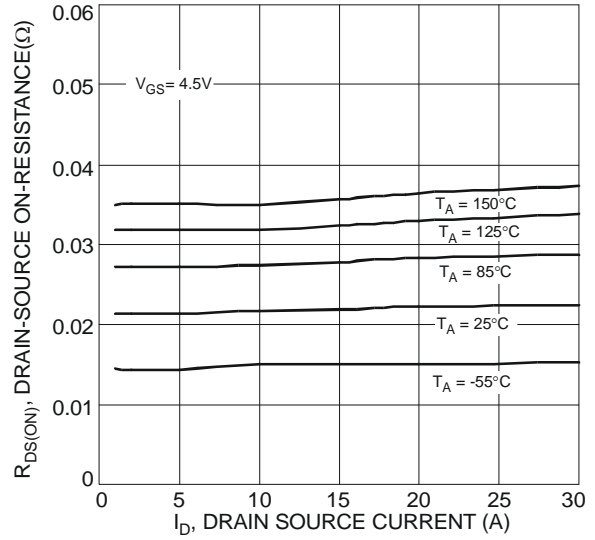


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

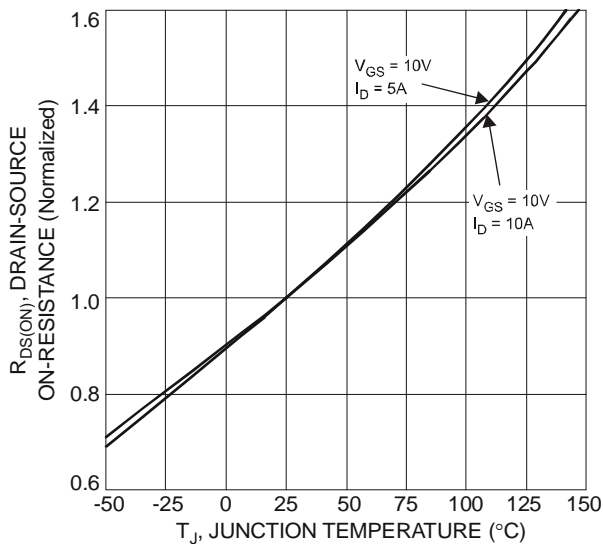


Fig. 5 On-Resistance Variation with Temperature

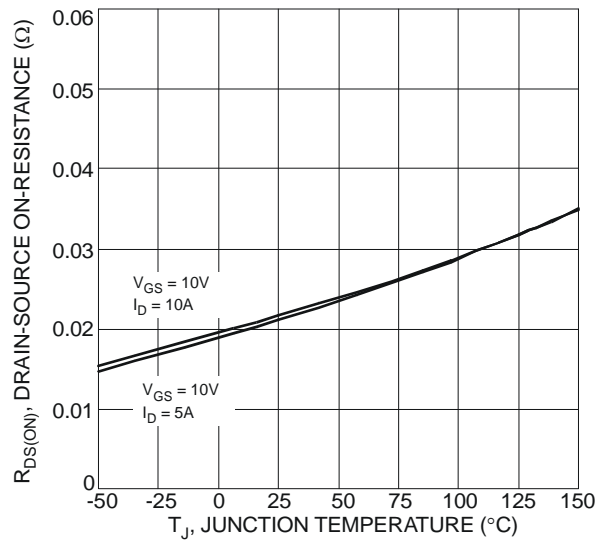


Fig. 6 On-Resistance Variation with Temperature

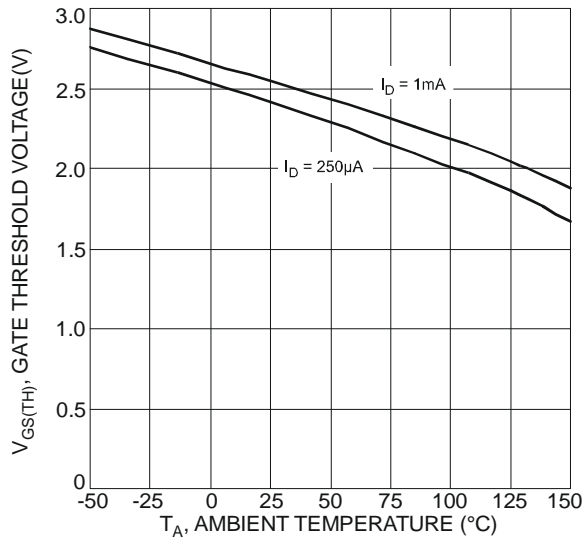


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

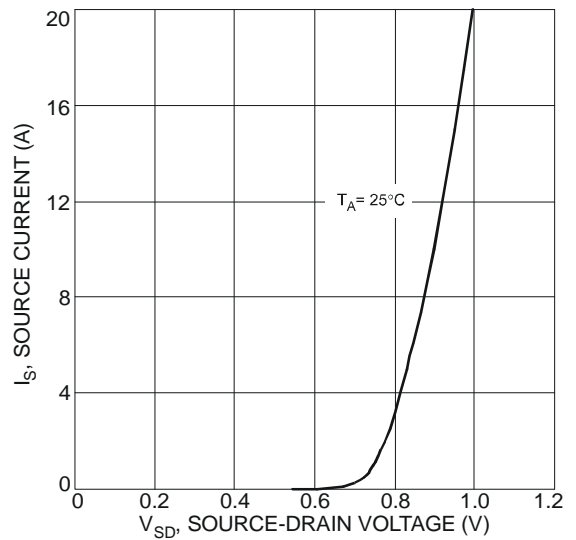


Fig. 8 Diode Forward Voltage vs. Current

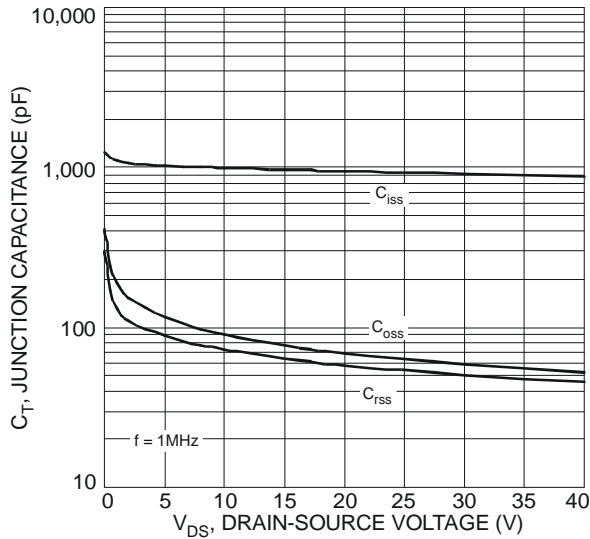


Fig. 9 Typical Junction Capacitance

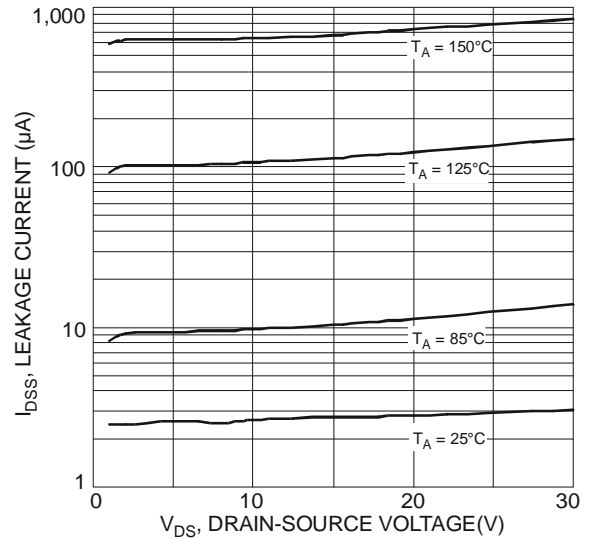


Fig. 10 Typical Drain-Source Leakage Current vs. Voltage

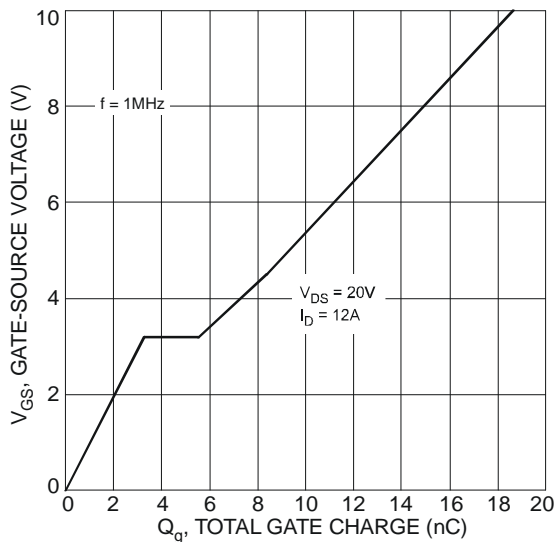


Fig. 11 Gate-Charge Characteristics

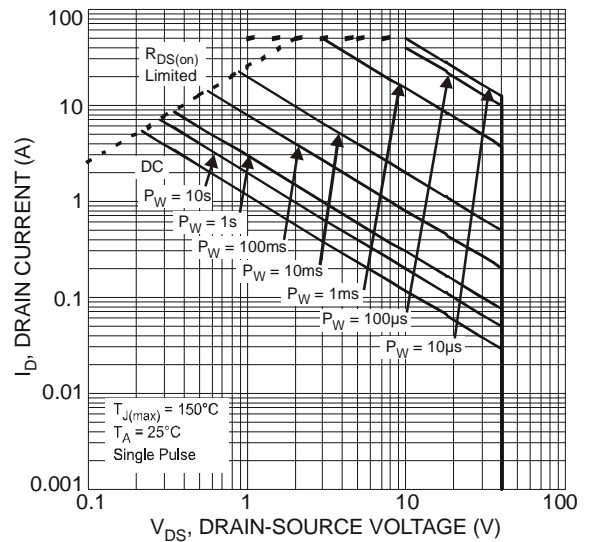
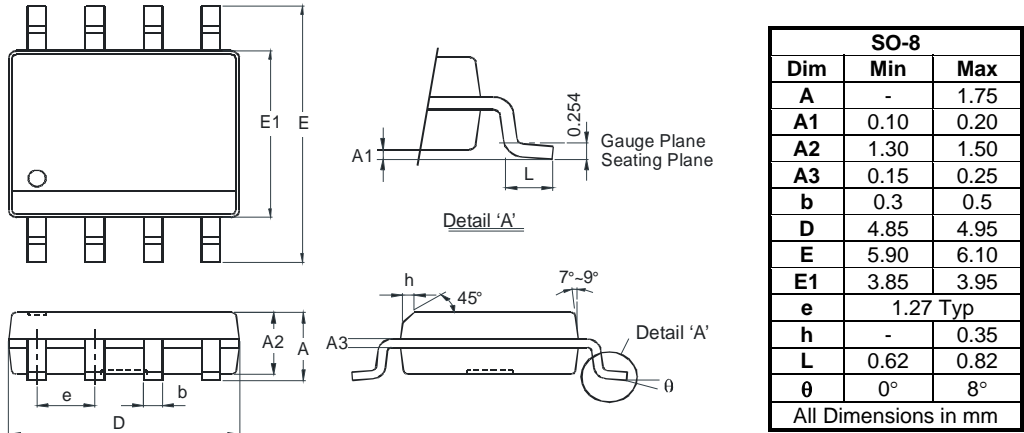
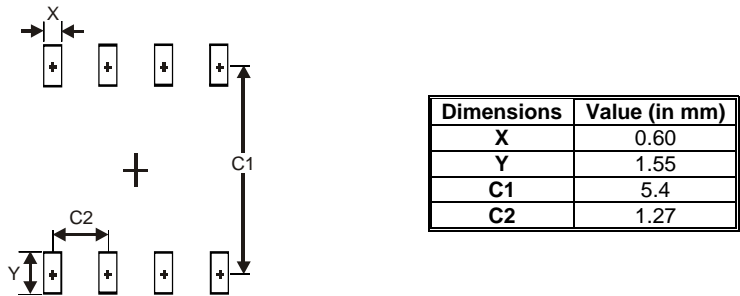


Fig. 12 SOA, Safe Operation Area

**Package Outline Dimensions**



**Suggested Pad Layout**



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