

# TPC6902

High-Speed Switching Applications  
MOS Gate Drive Applications

NPN and PNP transistors are mounted on a compact and slim package.

High DC current gain : NPN  $h_{FE} = 200$  to  $500$  ( $I_C = 0.2$  A)  
: PNP  $h_{FE} = 200$  to  $500$  ( $I_C = -0.2$  A)

Low collector-emitter saturation voltage  
: NPN  $V_{CE(sat)} = 0.14$  V (max)  
: PNP  $V_{CE(sat)} = -0.2$  V (max)

High-speed switching : NPN  $t_f = 45$  ns (typ.)  
: PNP  $t_f = 40$  ns (typ.)

### Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating		Unit	
		NPN	PNP		
Collector-base voltage	$V_{CBO}$	60	- 30	V	
Collector-emitter voltage	$V_{CEX}$	50	- 30	V	
	$V_{CEO}$	30	- 30	V	
Emitter-base voltage	$V_{EBO}$	7	- 7	V	
Collector current (Note 1)	DC	$I_C$	2.0	- 1.7	A
	Pulse	$I_{CP}$	8.0	- 8.0	A
Base current	$I_B$	0.5	- 0.5	A	
Collector power dissipation (t=10 s) (Note 2)	Single-device operation	$P_C$	1.0	W	
Collector power dissipation (DC) (Note 2)	Single-device operation	$P_C$	0.7	W	
	Single-device value at dual operation	$P_C$	0.6		
Thermal resistance, junction to ambient (t=10 s) (Note 2)	Single-device operation	$R_{th(j-a)}$	125	°C/W	
Thermal resistance, junction to ambient (DC) (Note 2)	Single-device operation	$R_{th(j-a)}$	178	°C/W	
	Single-device value at dual operation	$R_{th(j-a)}$	208		
Junction temperature	$T_j$	150		°C	
Storage temperature range	$T_{stg}$	-55 to 150		°C	

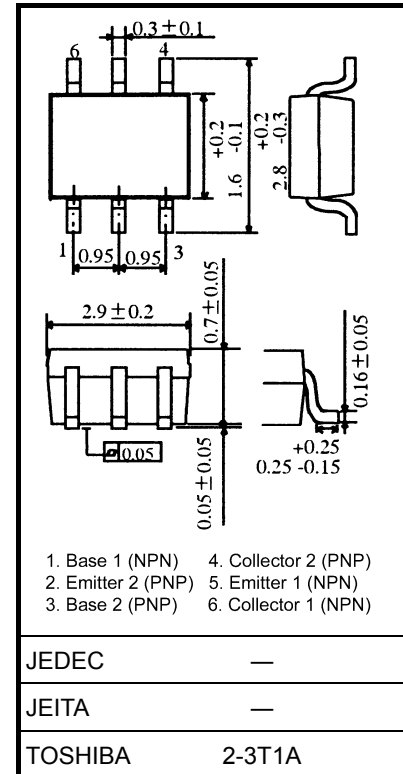
Note 1: Ensure that the junction temperature does not exceed 150°C.

Note 2: Mounted on an FR4 board (glass epoxy, 1.6 mm thick, Cu area: 645 mm<sup>2</sup>)

Note 3: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

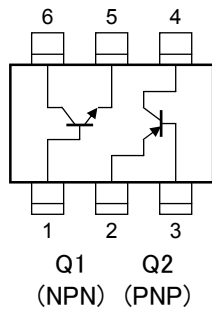
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Unit: mm

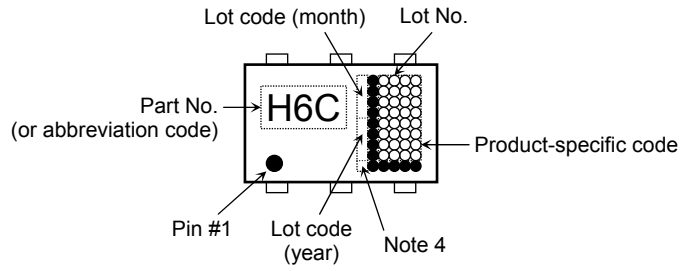


Weight: 0.011 g (typ.)

**Figure 1. Circuit configuration (top view)**



**Figure 2. Marking**



Note 4: A dot marking identifies the indication of product Labels.

[[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.

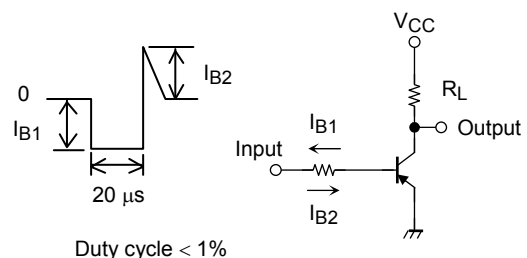
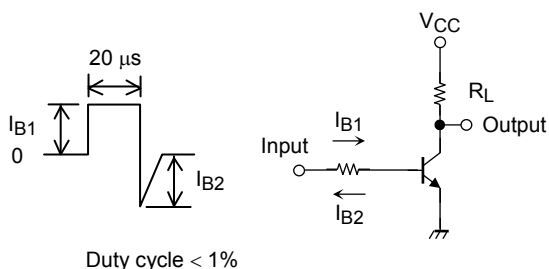
The RoHS is the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

## Electrical Characteristics (Ta = 25°C) : NPN

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit	
Collector cut-off current	$I_{CBO}$	$V_{CB} = 60\text{ V}, I_E = 0$	—	—	100	nA	
Emitter cut-off current	$I_{EBO}$	$V_{EB} = 7\text{ V}, I_C = 0$	—	—	100	nA	
Collector-emitter breakdown voltage	$V_{(BR)CEO}$	$I_C = 10\text{ mA}, I_B = 0$	30	—	—	V	
DC current gain	$h_{FE} (1)$	$V_{CE} = 2\text{ V}, I_C = 0.2\text{ A}$	200	—	500		
	$h_{FE} (2)$	$V_{CE} = 2\text{ V}, I_C = 0.6\text{ A}$	125	—	—		
	$h_{FE} (3)$	$V_{CE} = 2\text{ V}, I_C = 2\text{ A}$	50	—	—		
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = 0.6\text{ A}, I_B = 20\text{ mA}$	—	—	0.14	V	
Base-emitter saturation voltage	$V_{BE(sat)}$	$I_C = 0.6\text{ A}, I_B = 20\text{ mA}$	—	—	1.1	V	
Collector output capacitance	$C_{ob}$	$V_{CB} = 10\text{ V}, I_E = 0, f = 1\text{ MHz}$	—	14	—	pF	
Switching time	Rise time	$t_r$	See Figure 1 circuit diagram. $V_{CC} \approx 18\text{ V}, R_L = 30\ \Omega$ $I_{B1} = I_{B2} = 20\text{ mA}$	—	45	—	ns
	Storage time	$t_{stg}$		—	580	—	
	Fall time	$t_f$		—	45	—	

## Electrical Characteristics (Ta = 25°C) : PNP

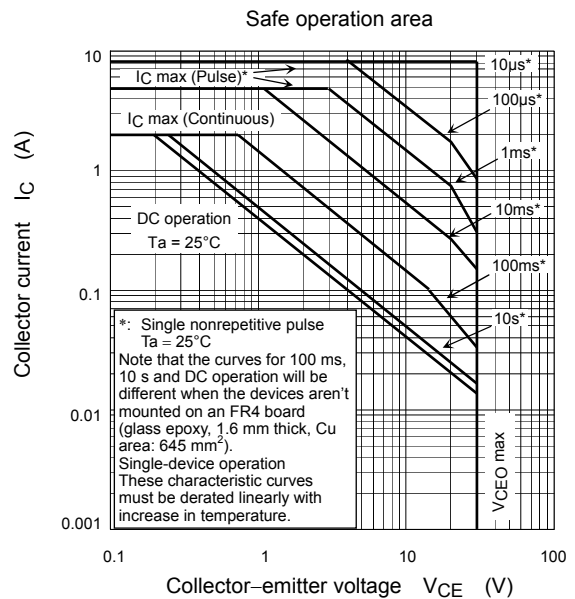
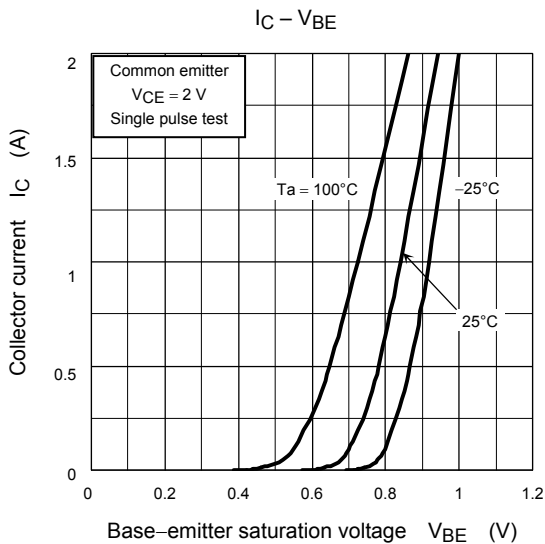
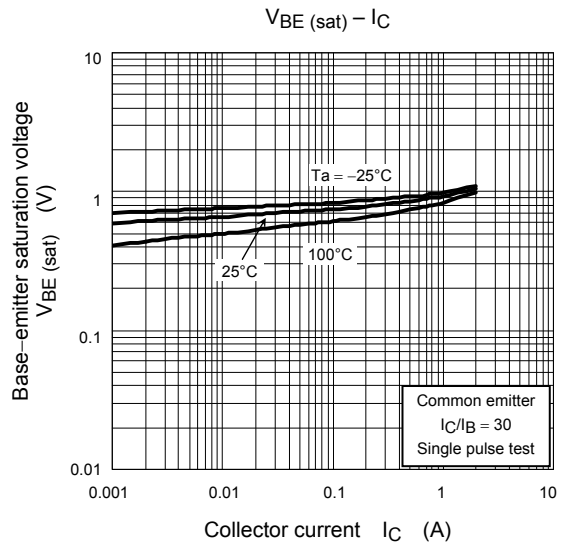
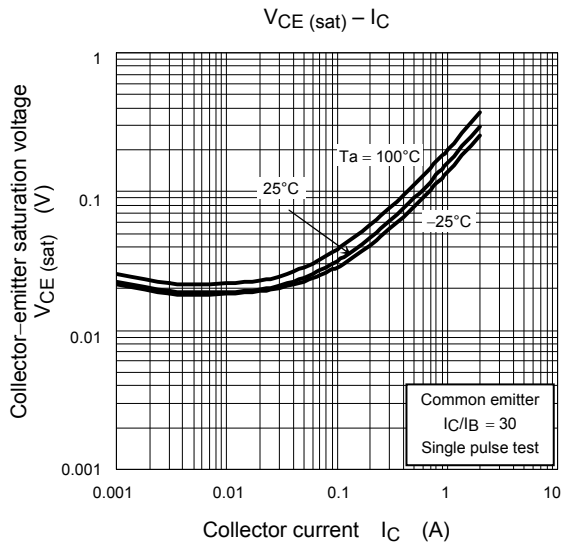
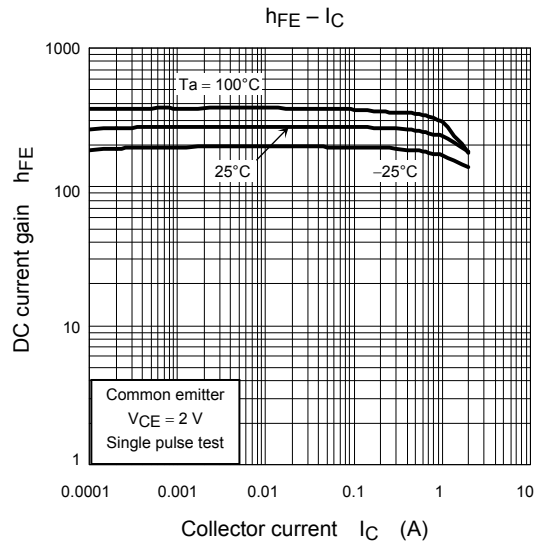
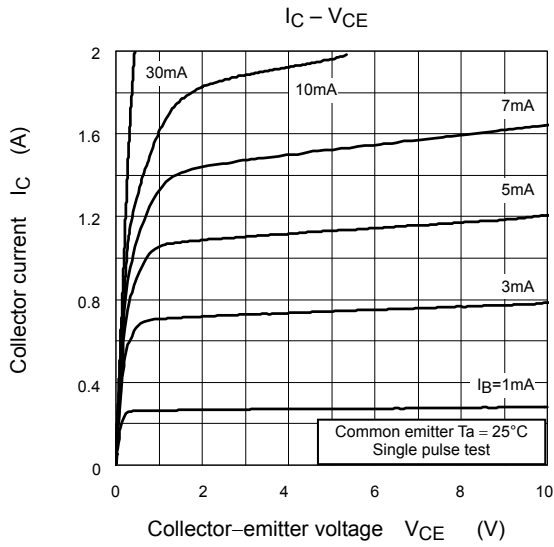
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit	
Collector cut-off current	$I_{CBO}$	$V_{CB} = -30\text{ V}, I_E = 0$	—	—	-100	nA	
Emitter cut-off current	$I_{EBO}$	$V_{EB} = -7\text{ V}, I_C = 0$	—	—	-100	nA	
Collector-emitter breakdown voltage	$V_{(BR)CEO}$	$I_C = -10\text{ mA}, I_B = 0$	-30	—	—	V	
DC current gain	$h_{FE} (1)$	$V_{CE} = -2\text{ V}, I_C = -0.2\text{ A}$	200	—	500		
	$h_{FE} (2)$	$V_{CE} = -2\text{ V}, I_C = -0.6\text{ A}$	125	—	—		
	$h_{FE} (3)$	$V_{CE} = -2\text{ V}, I_C = -2\text{ A}$	50	—	—		
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = -0.6\text{ A}, I_B = -20\text{ mA}$	—	—	-0.2	V	
Base-emitter saturation voltage	$V_{BE(sat)}$	$I_C = -0.6\text{ A}, I_B = -20\text{ mA}$	—	—	-1.1	V	
Collector output capacitance	$C_{ob}$	$V_{CB} = -10\text{ V}, I_E = 0, f = 1\text{ MHz}$	—	16.5	—	pF	
Switching time	Rise time	$t_r$	See Figure 2 circuit diagram. $V_{CC} \approx -18\text{ V}, R_L = 30\ \Omega$ $I_{B1} = I_{B2} = 20\text{ mA}$	—	40	—	ns
	Storage time	$t_{stg}$		—	280	—	
	Fall time	$t_f$		—	40	—	



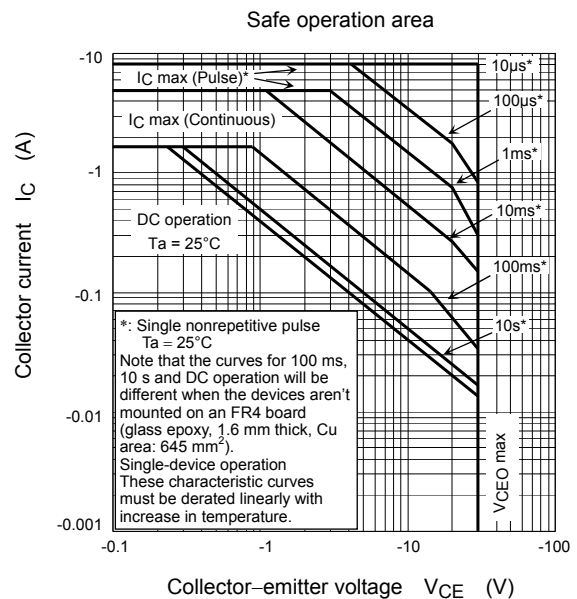
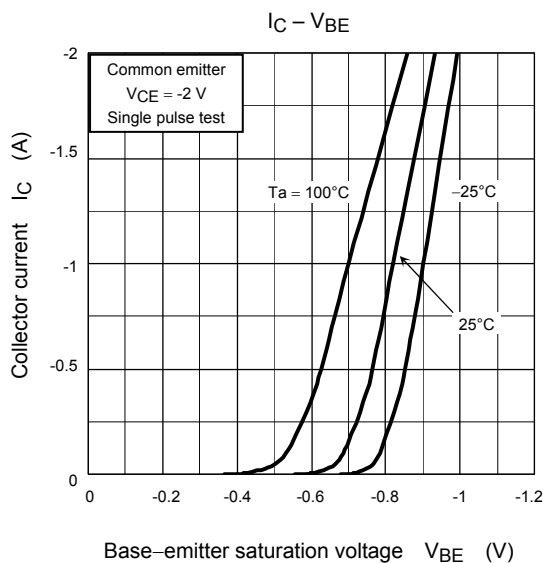
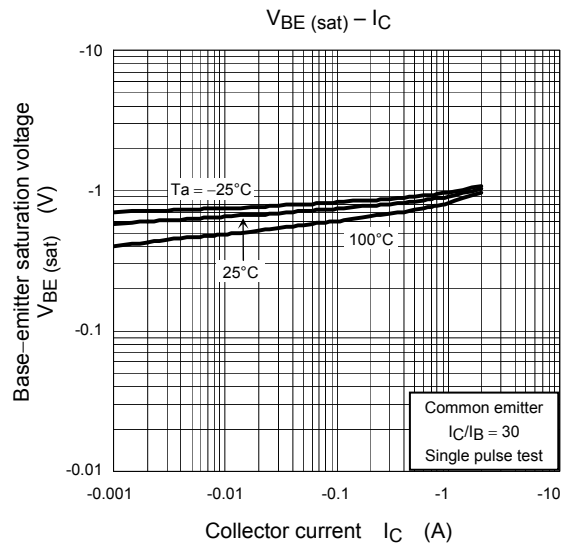
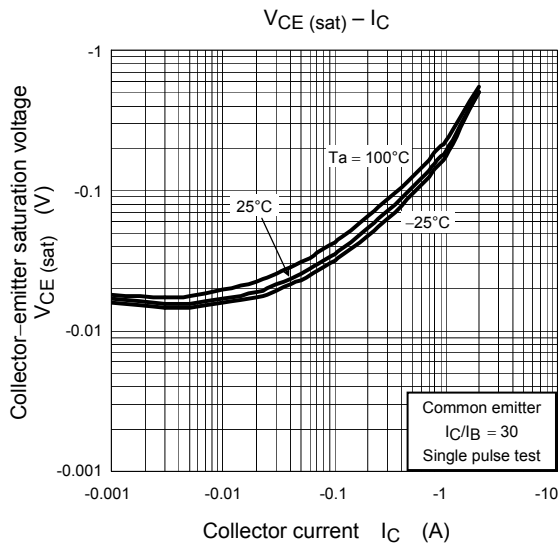
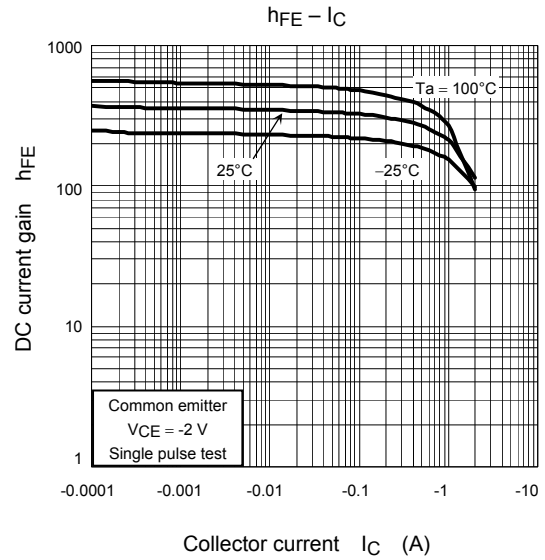
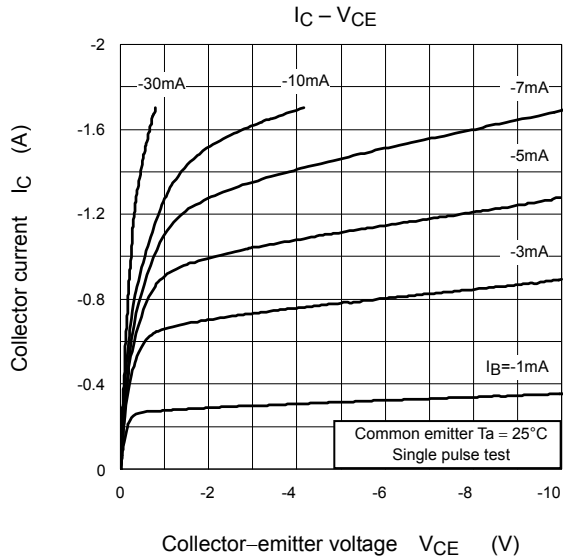
**Figure 1 Switching Time Test Circuit & Timing Chart (NPN)**

**Figure 2 Switching Time Test Circuit & Timing Chart (PNP)**

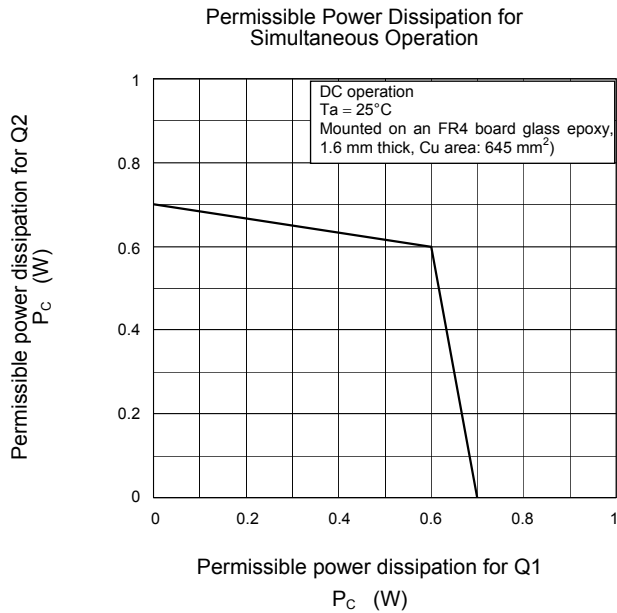
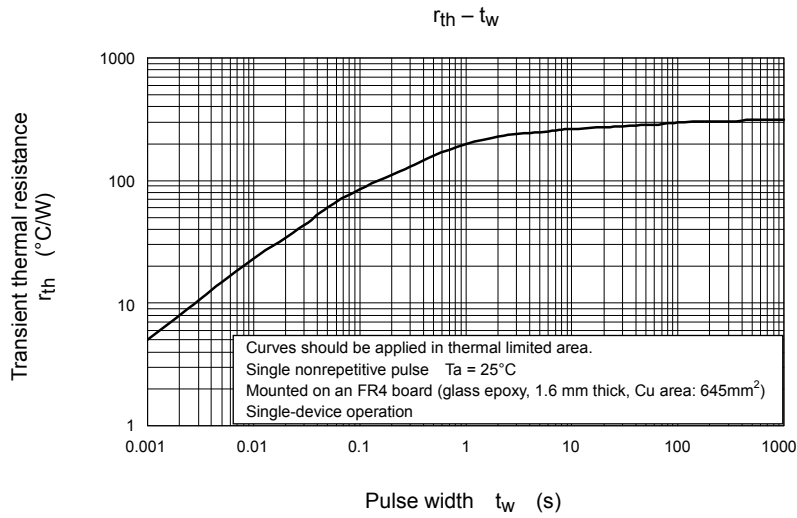
## NPN



## PNP



Common



Collector power dissipation at the single-device operation is 0.7W max.  
 Collector power dissipation at the single-device value at dual operation is 0.6W max.  
 Collector power dissipation at the dual operation is set to 1.2W max.

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