TOSHIBA Multi-Chip Transistor Silicon NPN / PNP Epitaxial Type

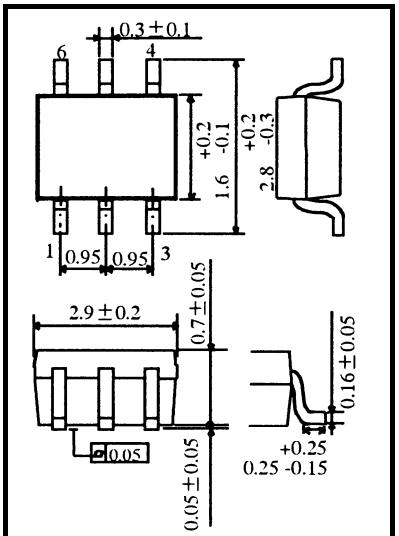
TPC6901A

High-Speed Switching Applications

MOS Gate Drive Applications

- NPN and PNP transistors are mounted on a compact and slim package.
- High DC current gain : NPN h_{FE} = 400 to 1000
  : PNP h_{FE} = 200 to 500
- Low collector-emitter saturation voltage
  : NPN $V_{CE\ (sat)}$ = 0.17 V (max)
  : PNP $V_{CE\ (sat)}$ = −0.23 V (max)
- High-speed switching : NPN t_f = 85 ns (typ.)
  : PNP t_f = 70 ns (typ.)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-3T1A

Weight: 0.011 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

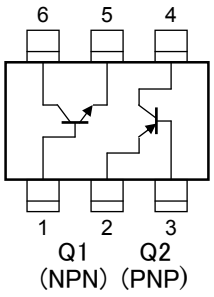
Characteristics		Symbol	Rating		Unit
			NPN	PNP	
Collector-base voltage		V_{CBO}	100	−50	V
Collector-emitter voltage		V_{CEX}	80	−50	V
Collector-emitter voltage		V_{CEO}	50	−50	V
Emitter-base voltage		V_{EBO}	7	−7	V
Collector current	DC (Note 1)	I_C	1.0	−0.7	A
	Pulse (Note 1)	I_{CP}	5.0	−5.0	A
Base current		I_B	0.1	−0.1	A
Collector power dissipation (t=10 s)	Single-device operation	P_C (Note 2)	500		mW
Collector power dissipation (DC)	Single-device operation	P_C (Note 2)	400		mW
	Single-device value at dual operation	P_C (Note 2)	330		
Thermal resistance, junction to ambient (t=10 s)	Single-device operation	$R_{th\ (j\text{-}a)}$ (Note 2)	250		°C/W
Thermal resistance, junction to ambient (DC)	Single-device operation	$R_{th\ (j\text{-}a)}$ (Note 2)	312		°C/W
	Single-device value at dual operation	$R_{th\ (j\text{-}a)}$ (Note 2)	378		
Junction temperature		T_j	150		°C
Storage temperature range		T_{stg}	−55 to 150		°C

Note 1: Please use devices on condition that the junction temperature is below 150°C.

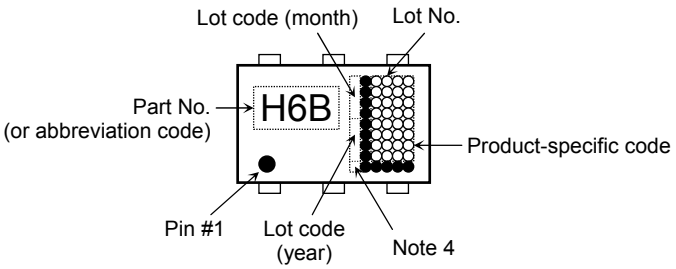
Note 2: Mounted on FR4 board (glass epoxy, 1.6 mm thick, Cu area: 645 mm^2)

Note 3: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Circuit Configuration



Marking



Note 4: A dot marking identifies the indication of product Labels.
[[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

Electrical Characteristics (Ta = 25°C): NPN

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cut-off current		I_{CBO}	V_{CB} = 100 V, I_E = 0	—	—	100	nA
Emitter cut-off current		I_{EBO}	V_{EB} = 7 V, I_C = 0	—	—	100	nA
Collector-emitter breakdown voltage		$V_{(BR)\ CEO}$	I_C = 10 mA, I_B = 0	50	—	—	V
DC current gain		h_{FE} (1)	V_{CE} = 2 V, I_C = 0.1 A	400	—	1000	
		h_{FE} (2)	V_{CE} = 2 V, I_C = 0.3 A	200	—	—	
Collector-emitter saturation voltage		$V_{CE\ (sat)}$	I_C = 300 mA, I_B = 6 mA	—	—	0.17	V
Base-emitter saturation voltage		$V_{BE\ (sat)}$	I_C = 300 mA, I_B = 6 mA	—	—	1.10	V
Collector output capacitance		C_{ob}	V_{CB} = 10 V, I_E = 0, f = 1 MHz	—	5	—	pF
Switching time	Rise time	t_r	See Figure 1 circuit diagram.	—	35	—	ns
	Storage time	t_{stg}	$V_{CC} \approx$ 30 V, R_L = 100 Ω	—	680	—	
	Fall time	t_f	$I_{B1} = I_{B2}$ = 10 mA	—	85	—	

Electrical Characteristics (Ta = 25°C): PNP

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cut-off current		I_{CBO}	V_{CB} = −50 V, I_E = 0	—	—	−100	nA
Emitter cut-off current		I_{EBO}	V_{EB} = −7 V, I_C = 0	—	—	−100	nA
Collector-emitter breakdown voltage		$V_{(BR)\ CEO}$	I_C = −10 mA, I_B = 0	−50	—	—	V
DC current gain		h_{FE} (1)	V_{CE} = −2 V, I_C = −0.1 A	200	—	500	
		h_{FE} (2)	V_{CE} = −2 V, I_C = −0.3 A	125	—	—	
Collector-emitter saturation voltage		$V_{CE\ (sat)}$	I_C = −300 mA, I_B = −10 mA	—	—	−0.23	V
Base-emitter saturation voltage		$V_{BE\ (sat)}$	I_C = −300 mA, I_B = −10 mA	—	—	−1.10	V
Collector output capacitance		C_{ob}	V_{CB} = −10 V, I_E = 0, f = 1 MHz	—	8	—	pF
Switching time	Rise time	t_r	See Figure 2 circuit diagram.	—	60	—	ns
	Storage time	t_{stg}	$V_{CC} \approx$ −30 V, R_L = 100 Ω	—	280	—	
	Fall time	t_f	$I_{B1} = I_{B2}$ = 10 mA	—	70	—	

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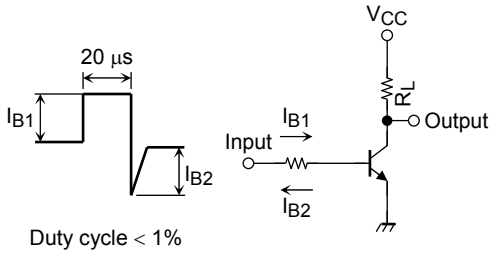


Figure 1 Switching Time Test Circuit & Timing Chart (NPN)

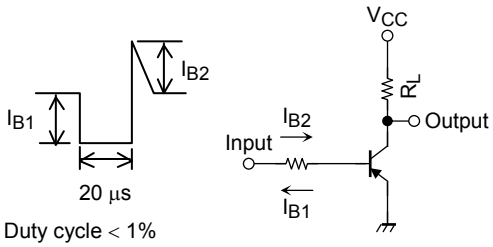
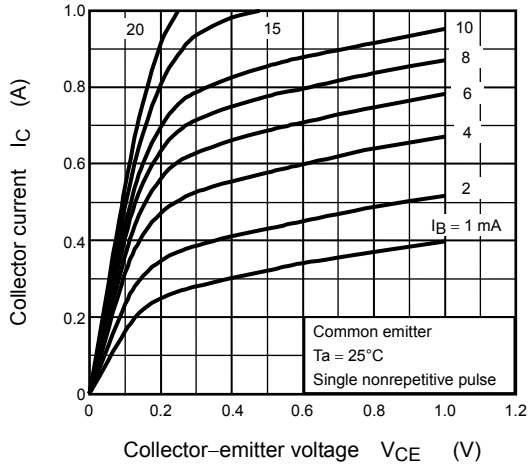


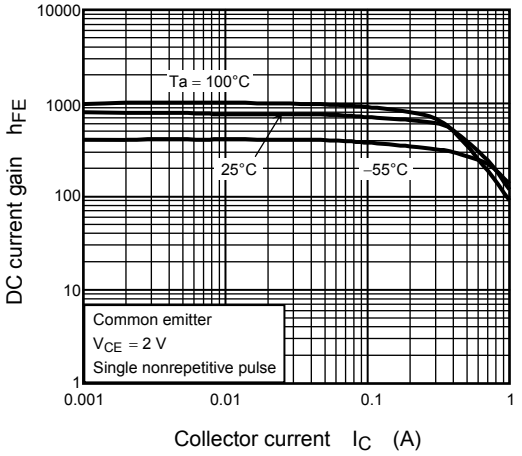
Figure 2 Switching Time Test Circuit & Timing Chart (PNP)

NPN

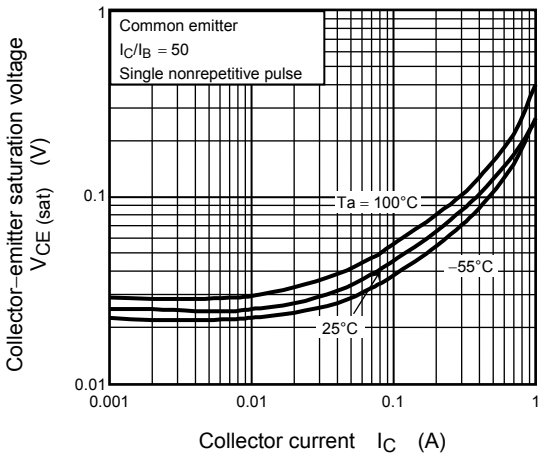
$I_C - V_{CE}$



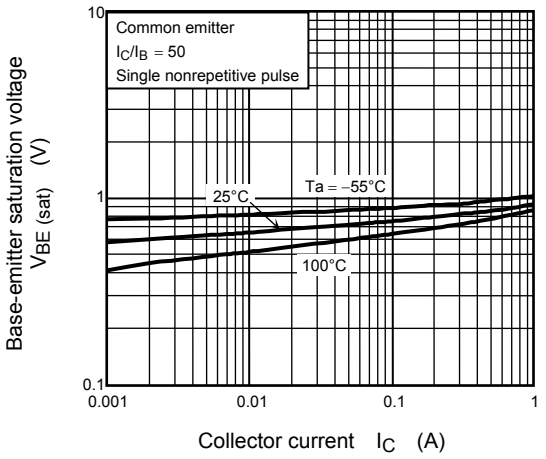
$h_{FE} - I_C$



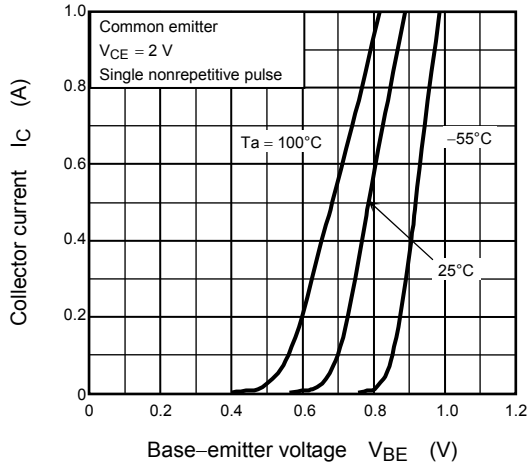
$V_{CE\ (sat)} - I_C$



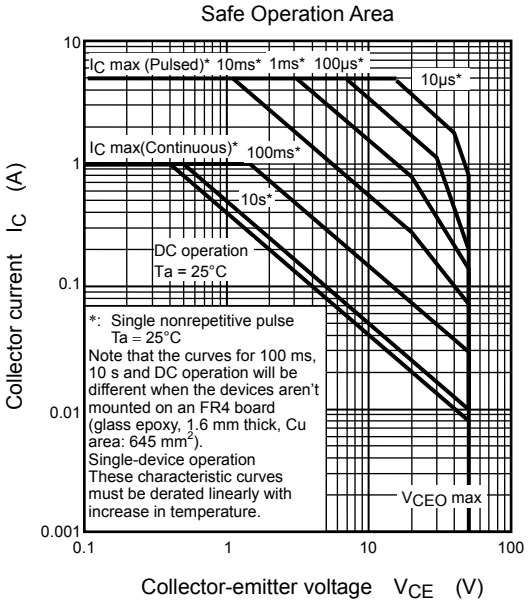
$V_{BE\ (sat)} - I_C$



$I_C - V_{BE}$

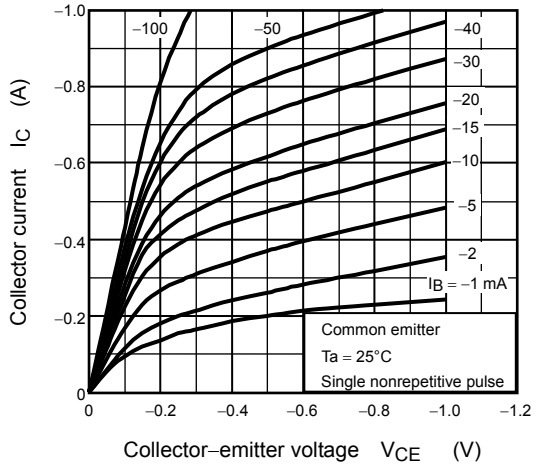


Safe Operation Area

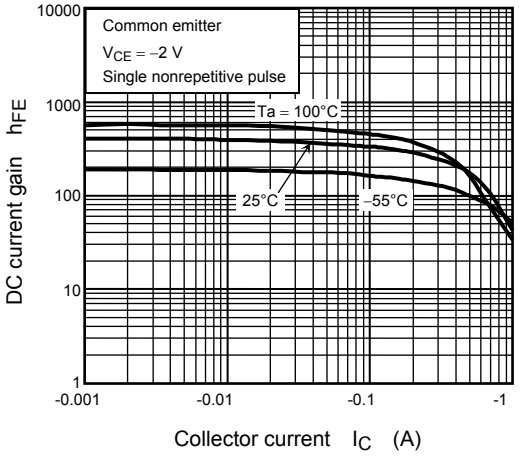


PNP

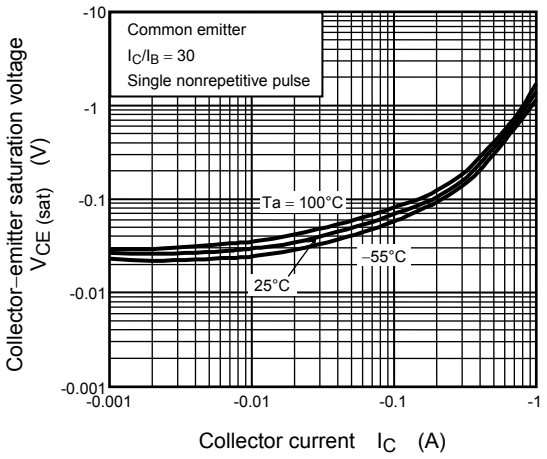
$I_C - V_{CE}$



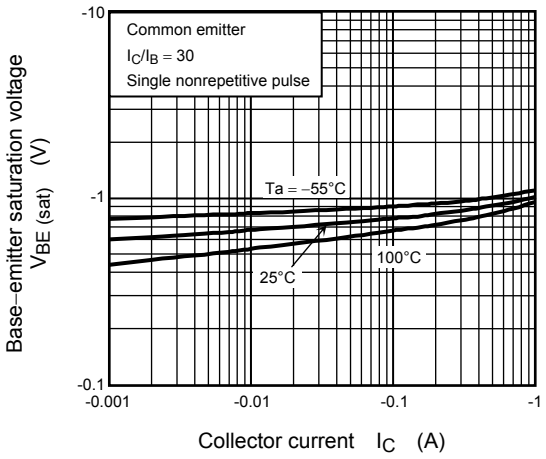
$h_{FE} - I_C$



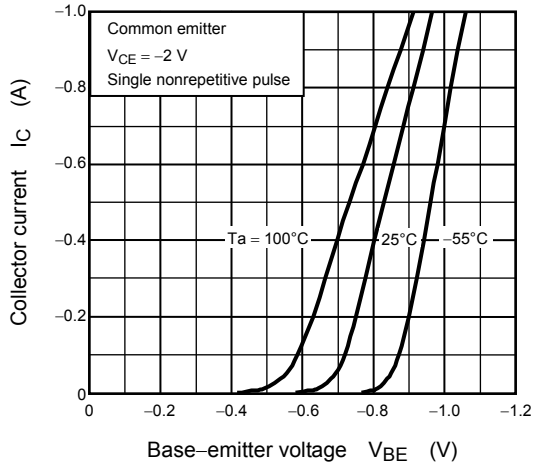
$V_{CE\ (sat)} - I_C$



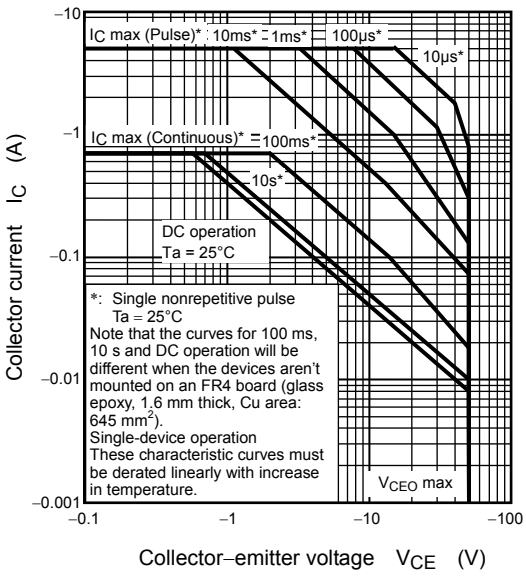
$V_{BE\ (sat)} - I_C$



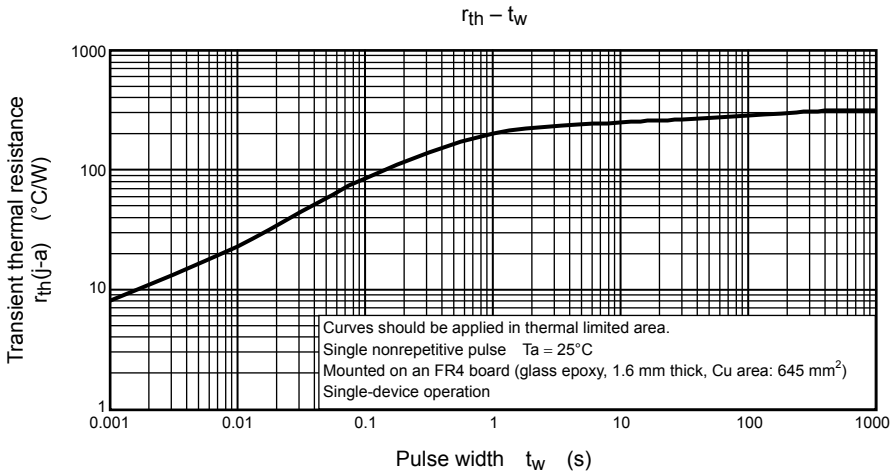
$I_C - V_{BE}$

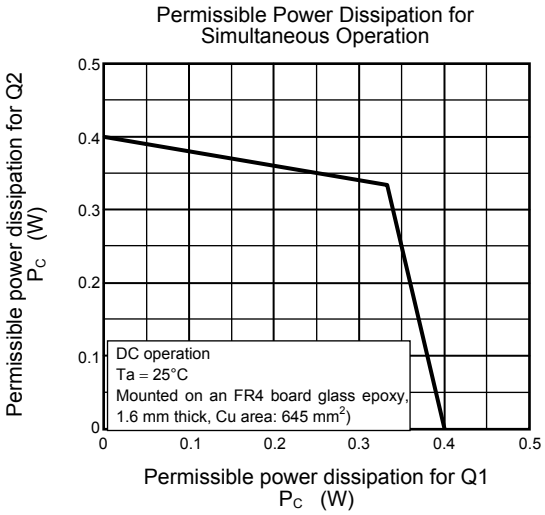


Safe operation area



Common





Collector power dissipation at the single-device operation is 0.4W.
Collector power dissipation at the single-device value at dual operation is 0.33W.
Collector power dissipation at the dual operation is set to 0.66W.

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