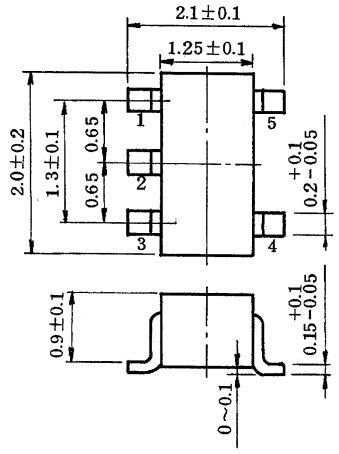
TOSHIBA Transistor Silicon PNP Epitaxial Type (PCT Process) (Bias Resistor Built-in Transistor)

# RN2714

Switching, Inverter Circuit, Interface Circuit
and Driver Circuit Applications

- Two devices incorporated in a USV (5-pin ultra-super-mini-type)
- Built-in bias resistors
- Simplified circuit design
- Reduced quantity of parts and manufacturing process

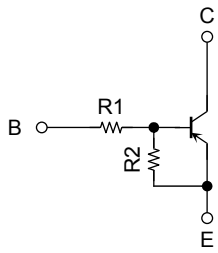
Unit: mm




| | |
|---|---|
| 1. BASE 1 | (B1) |
| 2. EMITTER | (E) |
| 3. BASE 2 | (B2) |
| 4. COLLECTOR 2 | (C2) |
| 5. COLLECTOR 1 | (C1) |
| USV | |
| JEDEC | — |
| JEITA | — |
| TOSHIBA | 2-2L1A |

Weight: 6.2 mg

## Equivalent Circuit




R1: 1.0 kΩ (Q1, Q2 common)

R2: 10 kΩ (Q1, Q2 common)

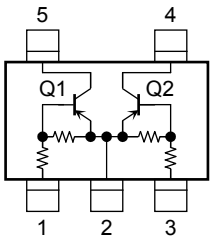
## Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 common)

| Characteristic | Symbol | Rating | Unit |
|---|---|---|---|
| Collector-base voltage | $V_{CBO}$ | −50 | V |
| Collector-emitter voltage | $V_{CEO}$ | −50 | V |
| Emitter-base voltage | $V_{EBO}$ | −5 | V |
| Collector current | $I_C$ | −100 | mA |
| Collector power dissipation | $P_C$* | 200 | mW |
| Junction temperature | $T_j$ | 150 | °C |
| Storage temperature range | $T_{stg}$ | −55 to 150 | °C |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

* : Total rating

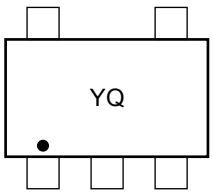
## Equivalent Circuit (top view)



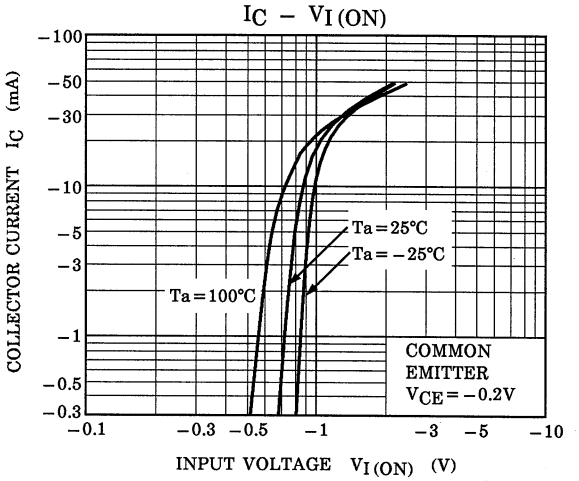
## Electrical Characteristics (Ta = 25°C) (Q1, Q2 common)

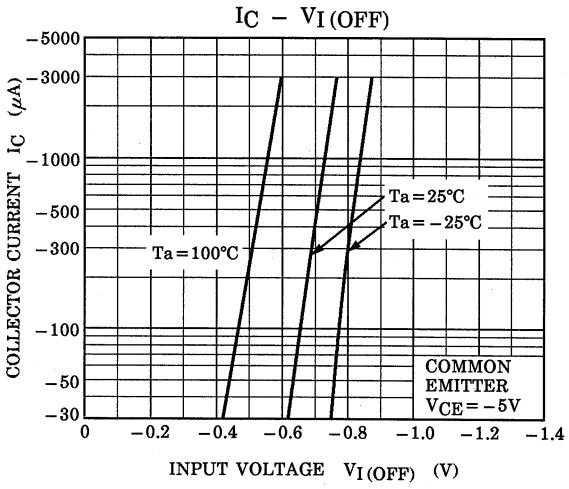
| Characteristic | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Collector cutoff current | $I_{CBO}$ | — | $V_{CB}$ = −50 V, $I_E$ = 0 | — | — | −100 | nA |
| Emitter cutoff current | $I_{EBO}$ | — | $V_{EB}$ = −5 V, $I_C$ = 0 | −0.35 | — | −0.65 | mA |
| DC current gain | $h_{FE}$ | — | $V_{CE}$ = −5 V, $I_C$ = −10 mA | 50 | — | — | — |
| Collector-emitter saturation voltage | $V_{CE\ (sat)}$ | — | $I_C$ = −5 mA, $I_B$ = −0.25 mA | — | −0.1 | −0.3 | V |
| Input voltage (ON) | $V_{I\ (ON)}$ | — | $V_{CE}$ = −0.2 V, $I_C$ = −5 mA | −0.5 | — | −2.0 | V |
| Input voltage (OFF) | $V_{I\ (OFF)}$ | — | $V_{CE}$ = −5 V, $I_C$ = −0.1 mA | −0.3 | — | −0.9 | V |
| Input resistor | R1 | — | — | 0.7 | 1.0 | 1.3 | kΩ |
| Resistor ratio | R1/R2 | — | — | — | 0.1 | — | — |

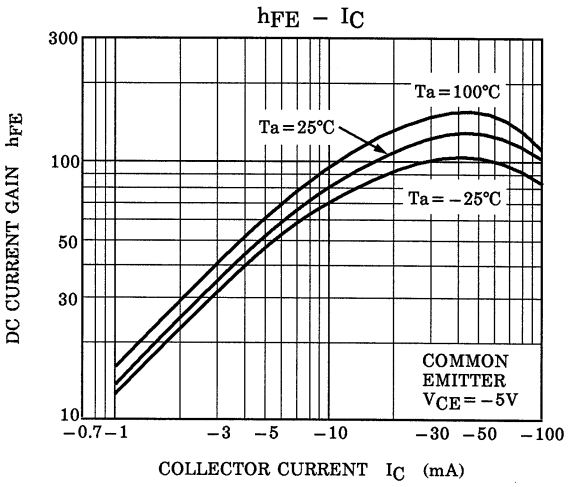
## Marking

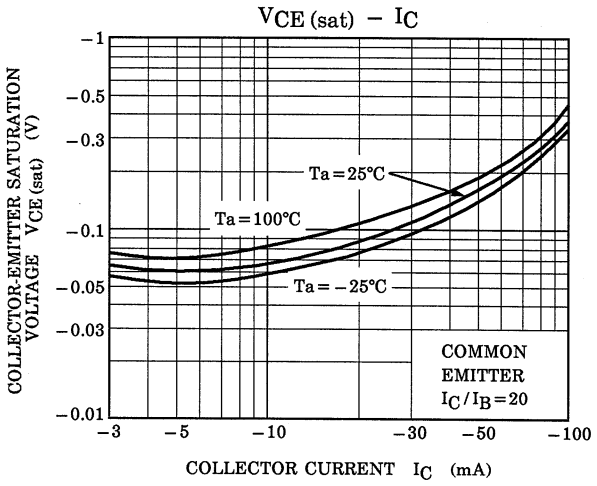


## Q1, Q2 Common


$I_C$ – $V_{I(ON)}$
COLLECTOR CURRENT $I_C$ (mA)
−100
−50
−30
−10
−5
−3
−1
−0.5
−0.3
Ta = 25°C
Ta = −25°C
Ta = 100°C
COMMON EMITTER
$V_{CE}$ = −0.2V
−0.1
−0.3
−0.5
−1
−3
−5
−10
INPUT VOLTAGE $V_{I(ON)}$ (V)


$I_C$ – $V_{I(OFF)}$
COLLECTOR CURRENT $I_C$ (μA)
−5000
−3000
−1000
−500
−300
−100
−50
−30
Ta = 25°C
Ta = −25°C
Ta = 100°C
COMMON EMITTER
$V_{CE}$ = −5V
0
−0.2
−0.4
−0.6
−0.8
−1.0
−1.2
−1.4
INPUT VOLTAGE $V_{I(OFF)}$ (V)


$h_{FE}$ – $I_C$
DC CURRENT GAIN $h_{FE}$
300
100
50
30
10
Ta = 100°C
Ta = 25°C
Ta = −25°C
COMMON EMITTER
$V_{CE}$ = −5V
−0.7
−1
−3
−5
−10
−30
−50
−100
COLLECTOR CURRENT $I_C$ (mA)


$V_{CE(sat)}$ – $I_C$
COLLECTOR-EMITTER SATURATION VOLTAGE $V_{CE(sat)}$ (V)
−1
−0.5
−0.3
−0.1
−0.05
−0.03
−0.01
Ta = 25°C
Ta = 100°C
Ta = −25°C
COMMON EMITTER
$I_C / I_B$ = 20
−3
−5
−10
−30
−50
−100
COLLECTOR CURRENT $I_C$ (mA)

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