## **DRC4114W**

## Silicon NPN epitaxial planar type

For digital circuits
DRC2114W in NS through hole type package

#### ■ Features

- $\bullet$  Low collector-emitter saturation voltage  $V_{\text{CE(sat)}}$
- Contributes to miniaturization of sets, mount area reduction
- Eco-friendly Halogen-free package

### Packaging

DRC4114W0A Radial type: 5000 pcs / carton

## ■ Absolute Maximum Ratings $T_a = 25$ °C

Parameter	Symbol	Rating	Unit	
Collector-base voltage (Emitter open)	V <sub>CBO</sub>	50	V	
Collector-emitter voltage (Base open)	V <sub>CEO</sub>	50	V	
Collector current	$I_{C}$	100	mA	
Total power dissipation	P <sub>T</sub>	300	mW	
Junction temperature	T <sub>j</sub>	150	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	

## ■ Package

• Code

NS-B2-B-B

Package dimension clicks here.  $\rightarrow$ 

#### Pin Name

- 1: Emitter
- 2: Collector
- 3: Base

## ■ Marking Symbol: N9

### ■ Internal Connection

$$B \circ \begin{array}{c} R_1 \\ \\ R_2 \\ \end{array} \circ E$$

Resistance value	R <sub>1</sub>	10	kΩ
	R <sub>2</sub>	4.7	kΩ

## ■ Electrical Characteristics $T_a = 25$ °C±3°C

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Collector-base voltage (Emitter open)	$V_{CBO}$	$I_{\rm C} = 10  \mu A, I_{\rm E} = 0$	50			V
Collector-emitter voltage (Base open)	V <sub>CEO</sub>	$I_{\rm C} = 2 \text{ mA}, I_{\rm B} = 0$	50			V
Collector-base cutoff current (Emitter open)	$I_{CBO}$	$V_{CB} = 50 \text{ V}, I_{E} = 0$			0.1	μΑ
Collector-emitter cutoff current (Base open)	I <sub>CEO</sub>	$V_{CE} = 50 \text{ V}, I_{B} = 0$			0.5	μΑ
Emitter-base cutoff current (Collector open)	$I_{EBO}$	$V_{EB} = 6 \text{ V}, I_{C} = 0$			1.0	mA
Forward current transfer ratio	h <sub>FE</sub>	$V_{CE} = 10 \text{ V}, I_{C} = 5 \text{ mA}$	20			_
Collector-emitter saturation voltage	V <sub>CE(sat)</sub>	$I_C = 10 \text{ mA}, I_B = 0.5 \text{ mA}$			0.25	V
Input voltage (ON)	V <sub>I(on)</sub>	$V_{CE} = 0.2 \text{ V}, I_{C} = 5 \text{ mA}$	3.0			V
Input voltage (OFF)	V <sub>I(off)</sub>	$V_{CE} = 5 \text{ V}, I_{C} = 100  \mu\text{A}$			1.3	V
Input resistance	$R_1$		-30%	10.0	+30%	kΩ
Resistance ratio	$R_1/R_2$		1.70	2.13	2.60	_

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

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