

# DRC3143Y

## Silicon NPN epitaxial planar type

For digital circuits

Complementary to DRA3143Y

DRC9143Y in SSSMini3 type package

### ■ Features

- High forward current transfer ratio  $h_{FE}$
- Low collector-emitter saturation voltage  $V_{CE(sat)}$
- Contributes to miniaturization of sets, reduction of component count.
- Eco-friendly Halogen-free package

### ■ Packaging

Embossed type (Thermo-compression sealing): 10000 pcs / reel (standard)

### ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

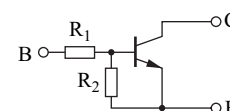
Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	$V_{CBO}$	50	V
Collector-emitter voltage (Base open)	$V_{CEO}$	50	V
Collector current	$I_C$	100	mA
Total power dissipation	$P_T$	100	mW
Junction temperature	$T_j$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

### ■ Package

- Code  
SSSMini3-F2-B
- Pin Name  
1: Base  
2: Emitter  
3: Collector

### ■ Marking Symbol: N7

### ■ Internal Connection

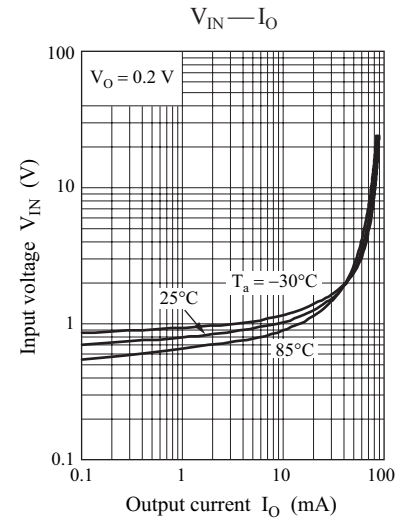
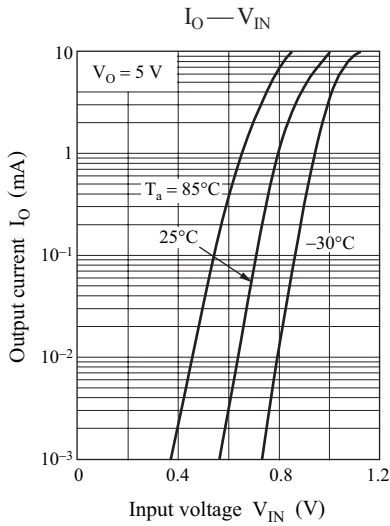
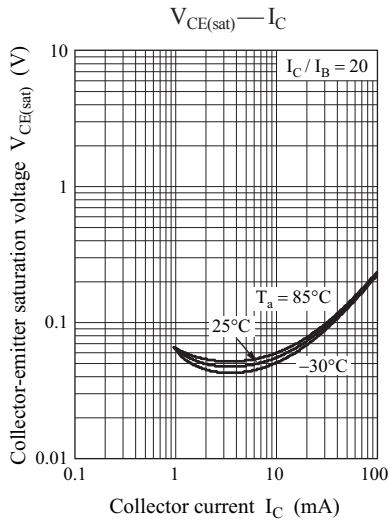
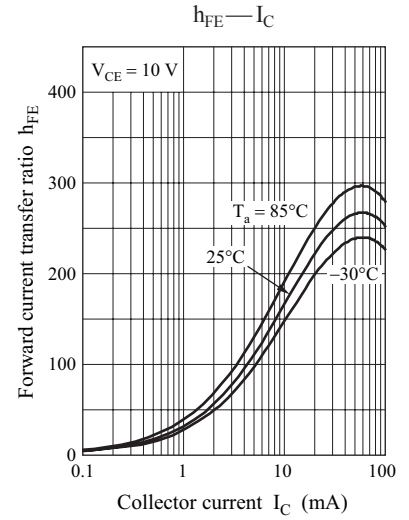
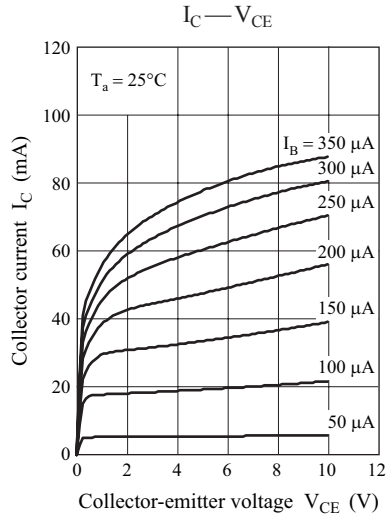
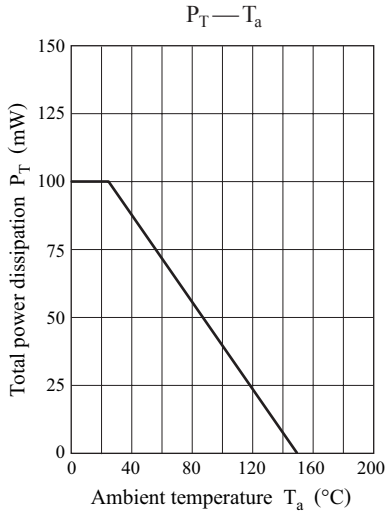


Resistance value	$R_1$	4.7	k $\Omega$
	$R_2$	22	k $\Omega$

### ■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

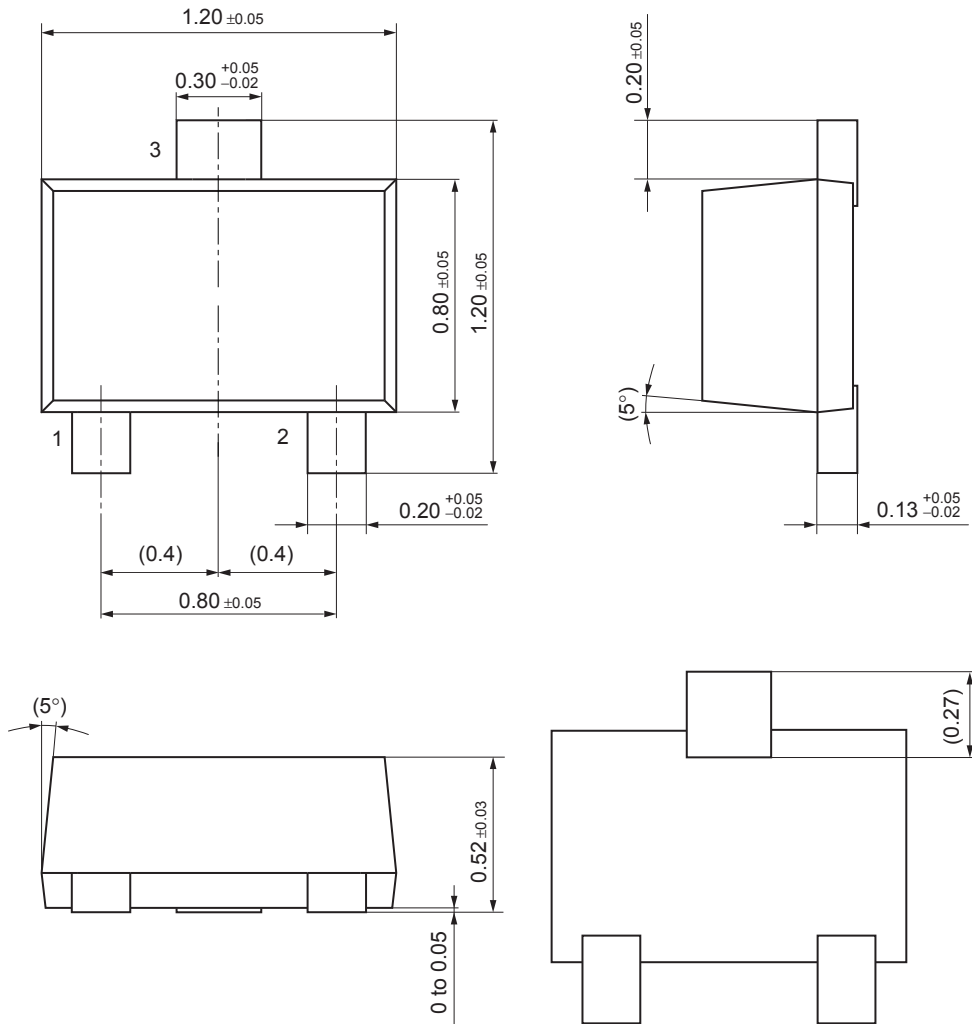
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	$V_{CBO}$	$I_C = 10 \mu\text{A}, I_E = 0$	50			V
Collector-emitter voltage (Base open)	$V_{CEO}$	$I_C = 2 \text{mA}, I_B = 0$	50			V
Collector-base cutoff current (Emitter open)	$I_{CBO}$	$V_{CB} = 50 \text{V}, I_E = 0$			0.1	$\mu\text{A}$
Collector-emitter cutoff current (Base open)	$I_{CEO}$	$V_{CE} = 50 \text{V}, I_B = 0$			0.5	$\mu\text{A}$
Emitter-base cutoff current (Collector open)	$I_{EBO}$	$V_{EB} = 6 \text{V}, I_C = 0$			0.4	mA
Forward current transfer ratio	$h_{FE}$	$V_{CE} = 10 \text{V}, I_C = 5 \text{mA}$	60		200	—
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = 10 \text{mA}, I_B = 0.5 \text{mA}$			0.25	V
Input voltage (ON)	$V_{I(on)}$	$V_{CE} = 0.2 \text{V}, I_C = 5 \text{mA}$	1.2			V
Input voltage (OFF)	$V_{I(off)}$	$V_{CE} = 5 \text{V}, I_C = 100 \mu\text{A}$			0.5	V
Input resistance	$R_1$		-30%	4.7	+30%	k $\Omega$
Resistance ratio	$R_1 / R_2$		0.17	0.21	0.27	—

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.



SSSMini3-F2-B

Unit: mm



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