



Dual N-Channel Enhancement-Mode Vertical DMOS FET

Features

- ▶ Dual N-channel devices
- ▶ Low threshold – 2.0V max.
- ▶ High input impedance
- ▶ Low input capacitance – 125pF max.
- ▶ Fast switching speeds
- ▶ Low on-resistance
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage

Applications

- ▶ Logic level interfaces – ideal for TTL and CMOS
- ▶ Solid state relays
- ▶ Battery operated systems
- ▶ Photo voltaic drives
- ▶ Analog switches
- ▶ General purpose line drivers
- ▶ Telecom switches

General Description

This low threshold, enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

| Device | Package Option | BV_{DSS}/BV_{DGS} (V) | $R_{DS(ON)}$ (max) (Ω) | $I_{D(ON)}$ (min) (A) | $V_{GS(th)}$ (max) (V) |
|--------|--|----------------------------|---------------------------------------|-----------------------------|------------------------------|
| | 8-Lead SOIC 4.90x3.90mm body 1.75mm height (max) 1.27mm pitch | | | | |
| TD9944 | TD9944TG-G | 240 | 6.0 | 1.0 | 2.0 |

-G indicates package is RoHS compliant ('Green')



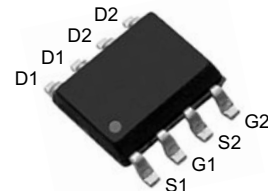
Absolute Maximum Ratings

| Parameter | Value |
|-----------------------------------|-----------------|
| Drain-to-source voltage | BV_{DSS} |
| Drain-to-gate voltage | BV_{DGS} |
| Gate-to-source voltage | $\pm 20V$ |
| Operating and storage temperature | -55°C to +150°C |
| Soldering temperature* | 300°C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* Distance of 1.6mm from case for 10 seconds.

Pin Configuration



8-Lead SOIC (TG)

Product Marking



YY = Year Sealed
 WW = Week Sealed
 — = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC (TG)

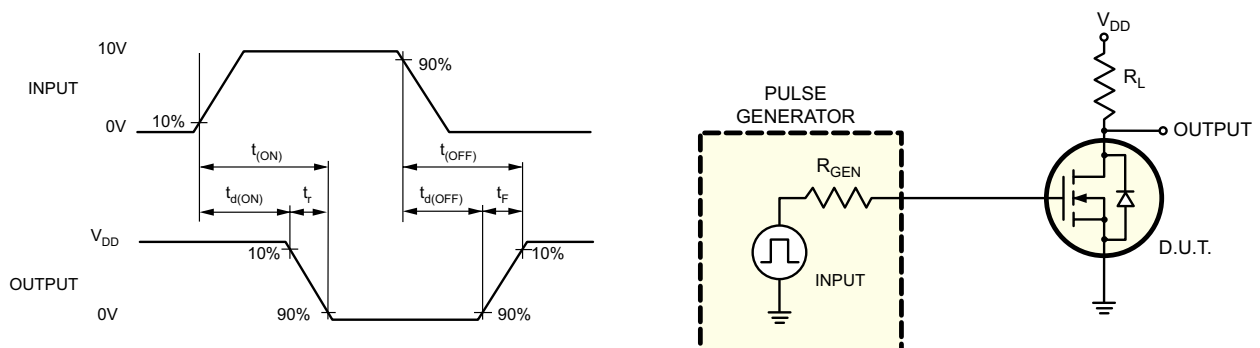
Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|---------------------|--|-----|-----|------|---------------|---|
| BV_{DSS} | Drain-to-source breakdown voltage | 240 | - | - | V | $V_{GS} = 0V, I_D = 2.0mA$ |
| $V_{GS(th)}$ | Gate threshold voltage | 0.6 | - | 2.0 | V | $V_{GS} = V_{DS}, I_D = 1.0mA$ |
| $\Delta V_{GS(th)}$ | Change in $V_{GS(th)}$ with temperature | - | - | -5.0 | mV/°C | $V_{GS} = V_{DS}, I_D = 1.0mA$ |
| I_{GSS} | Gate body leakage | - | - | 100 | nA | $V_{GS} = \pm 20V, V_{DS} = 0V$ |
| I_{DSS} | Zero gate voltage drain current | - | - | 10 | μA | $V_{GS} = 0V, V_{DS} = \text{Max Rating}$ |
| | | - | - | 1.0 | mA | $V_{DS} = 0.8\text{Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$ |
| $I_{D(ON)}$ | ON-state drain current | 0.5 | 1.9 | - | A | $V_{GS} = 4.5V, V_{DS} = 25V$ |
| | | 1.0 | 2.8 | - | | $V_{GS} = 10V, V_{DS} = 25V$ |
| $R_{DS(ON)}$ | Static drain-to-source on-state resistance | - | 4.0 | 6.0 | Ω | $V_{GS} = 4.5V, I_D = 250mA$ |
| | | - | 4.0 | 6.0 | | $V_{GS} = 10V, I_D = 0.5A$ |
| $\Delta R_{DS(ON)}$ | Change in $R_{DS(ON)}$ with temperature | - | - | 1.4 | %/°C | $V_{GS} = 10V, I_D = 0.5A$ |
| G_{FS} | Forward transductance | 300 | 600 | - | mmho | $V_{DS} = 20V, I_D = 0.5A$ |
| C_{ISS} | Input capacitance | - | 65 | 125 | pF | $V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz$ |
| C_{OSS} | Common source output capacitance | - | 35 | 70 | | |
| C_{RSS} | Reverse transfer capacitance | - | 10 | 25 | | |
| $t_{d(ON)}$ | Turn-on delay time | - | - | 10 | ns | $V_{DD} = 25V, I_D = 1.0A, R_{GEN} = 25\Omega$ |
| t_r | Rise time | - | - | 10 | | |
| $t_{d(OFF)}$ | Turn-off delay time | - | - | 20 | | |
| t_f | Fall time | - | - | 20 | | |
| V_{SD} | Diode forward voltage drop | - | - | 1.8 | V | $V_{GS} = 0V, I_{SD} = 1.0A$ |
| t_{rr} | Reverse recovery time | - | 300 | - | ns | $V_{GS} = 0V, I_{SD} = 1.0A$ |

Notes:

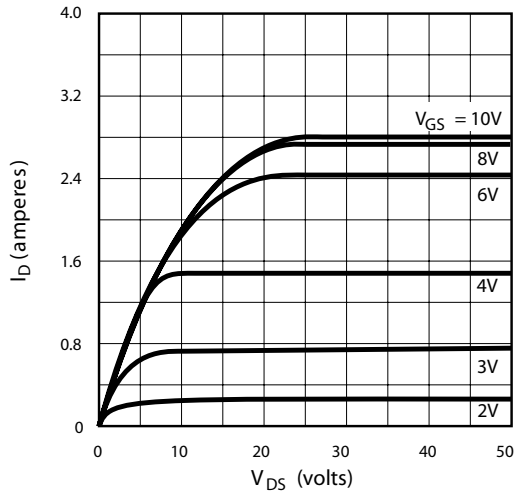
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

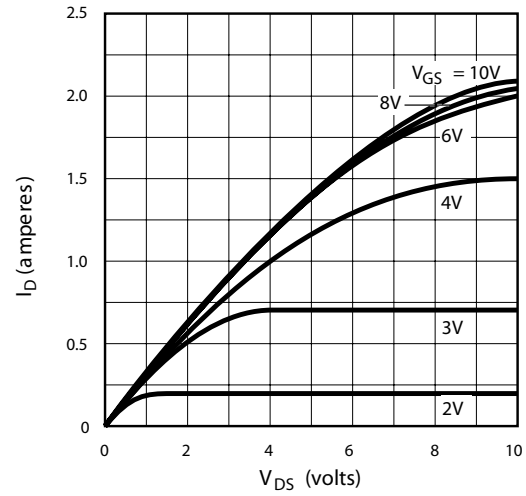


Typical Performance Curves

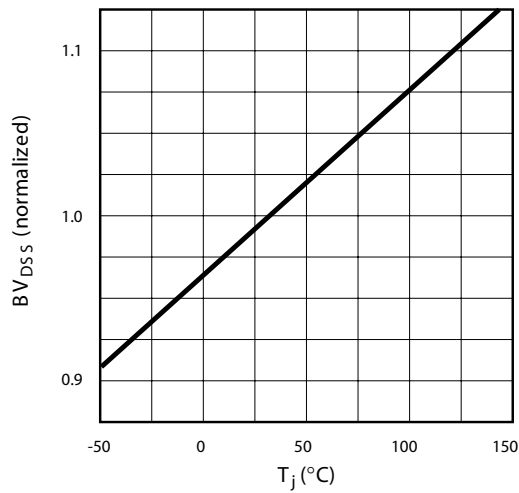
Output Characteristics



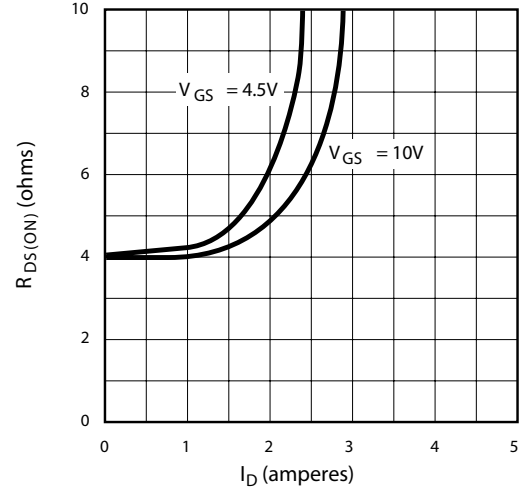
Saturation Characteristics



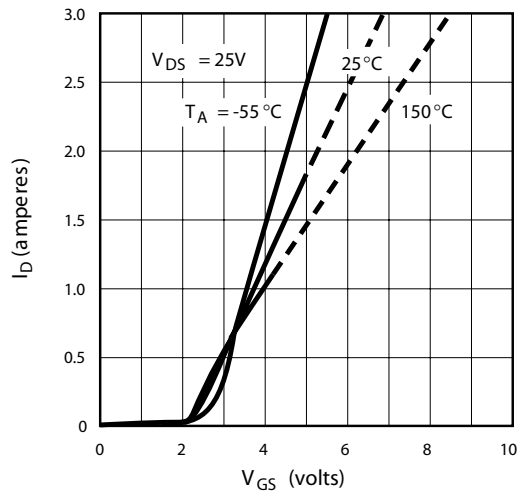
BV_{DSS} Variation with Temperature



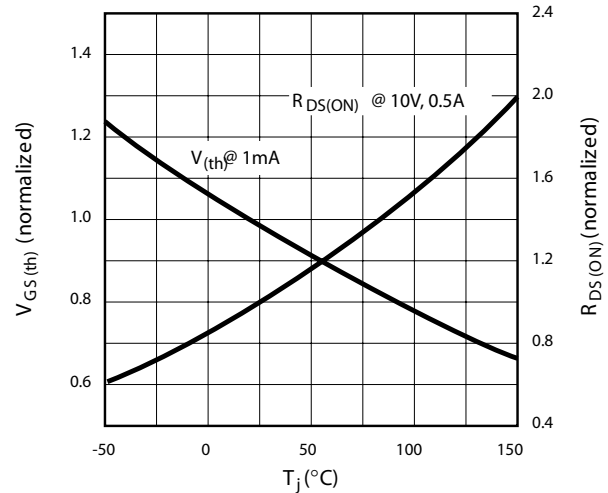
On-Resistance vs. Drain Current



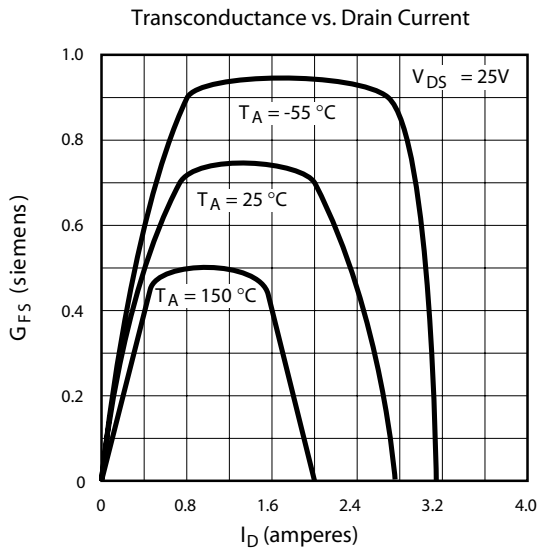
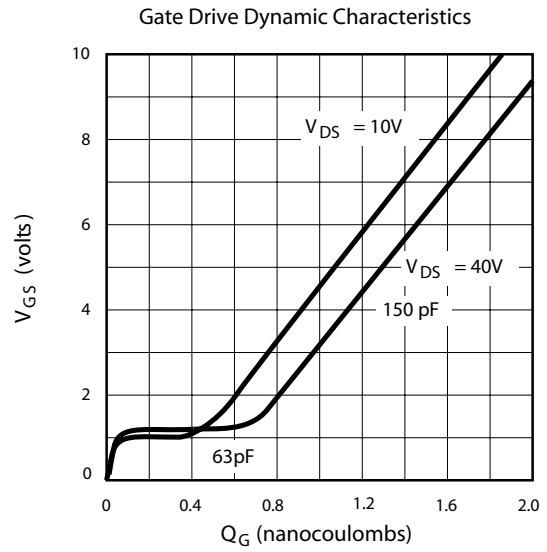
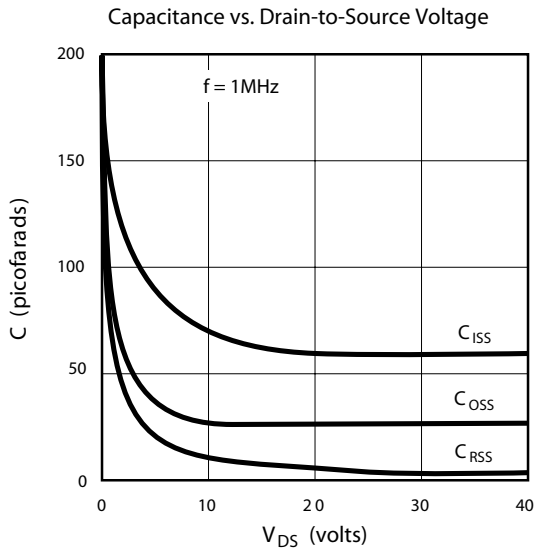
Transfer Characteristics



V_(th) and R_{DS} Variation with Temperature

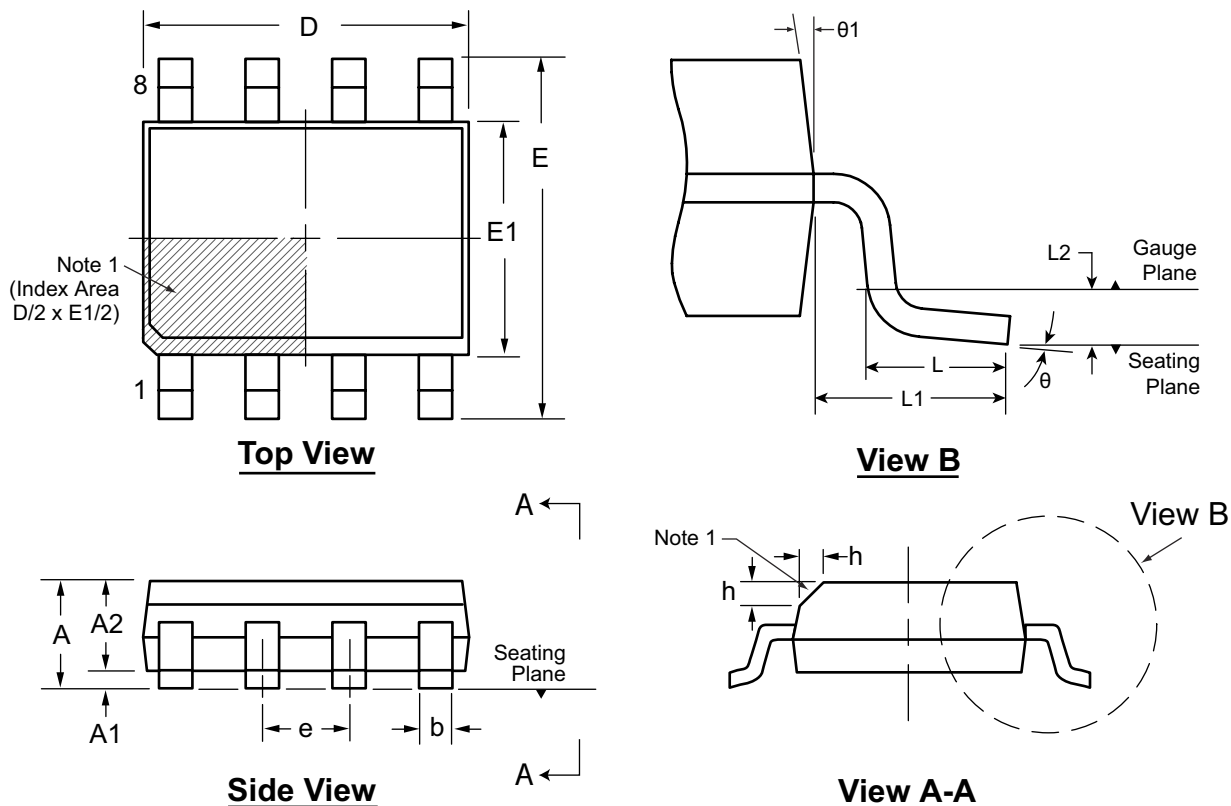


Typical Performance Curves (cont.)



8-Lead SOIC (Narrow Body) Package Outline (TG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note:
 1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol | A | A1 | A2 | b | D | E | E1 | e | h | L | L1 | L2 | θ | $\theta 1$ | |
|----------------|-----|-------|------|-------|------|-------|-------|-------|----------|------|------|----------|----------|------------|-----|
| Dimension (mm) | MIN | 1.35* | 0.10 | 1.25 | 0.31 | 4.80* | 5.80* | 3.80* | 1.27 BSC | 0.25 | 0.40 | 1.04 REF | 0.25 BSC | 0° | 5° |
| | NOM | - | - | - | - | 4.90 | 6.00 | 3.90 | | - | - | | | - | - |
| | MAX | 1.75 | 0.25 | 1.65* | 0.51 | 5.00* | 6.20* | 4.00* | | 0.50 | 1.27 | | | 8° | 15° |

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

Supertex Doc. #: DSPD-8SOLGTG, Version I041309.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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