



Solid State Devices, Inc.

14701 Firestone Blvd * La Mirada, Ca 90638
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SFT210DE

50 mA, 30 Volt, 1 nsec High Speed Analog N-Channel DMOSFET switch

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFT210 DE

└─ Screening ^{2/} = Not Screened
 TX = TX Level
 TXV = TXV Level
 S = S Level

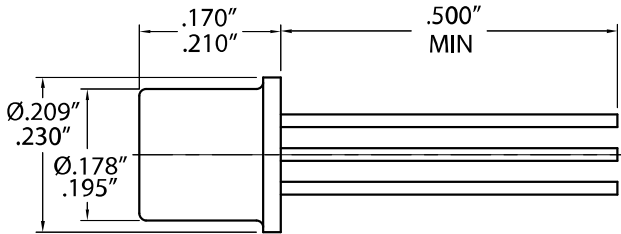
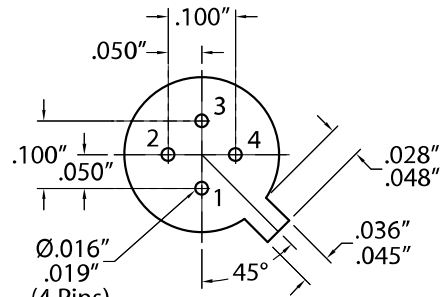
└─ Package DE = TO-72

- Features:**
- Ultra-High Speed Switching – $t_{ON} = 1$ ns
 - Ultra-Low Reverse Capacitance: 0.2pF
 - Low Guaranteed r_{DS} @ 5V
 - Low Turn-On Threshold Voltage
 - N-Channel Enhancement Mode
 - Replacement for SD210DE
 - TX, TXV, and S-Level Screening Available. Consult Factory. ^{2/}

Maximum Ratings	Symbol	Max	Units
Drain – Source Breakdown Voltage	V_{DS}	30	Volts
Source – Drain Voltage	V_{SD}	10	Volts
Gate - Drain Voltage	V_{GD}	± 40	Volts
Gate - Source Voltage	V_{GS}	± 40	Volts
Gate – Body (substrate) Voltage	V_{Gb}	± 30	Volts
Drain – Body (substrate) Voltage	V_{Db}	30	Volts
Source – Body (substrate) Voltage	V_{Sb}	15	Volts
Drain Current	I_D	50	mA
Power Dissipation	P_D	300 1.2	mWatts Watts
Maximum Thermal Resistance	Junction to Ambient Junction to Case	335 85	°C/W
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	°C
Operating & Storage Temperature	T_{OP} T_{STG}	-55 to +125 -65 to +150	°C °C

PACKAGE OUTLINE: TO-72

PIN ASSIGNMENT	
PIN 1	Source
PIN 2	Drain
PIN 3	Gate
PIN 4	Body (Substrate)



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Electrical Characteristics ^{3/}		Symbol	Typ	Min	Max	Units
Drain – Source Breakdown Voltage	$V_{GS} = V_{BS} = 0\text{ V}, I_D = 10\mu\text{A}$ $V_{GS} = V_{BS} = -5\text{ V}, I_D = 10\text{nA}$	$V_{(BR)DS}$	35 30	30 10	--	Volts
Source – Drain Breakdown Voltage	$V_{GD} = V_{BD} = -5\text{ V}, I_S = 10\text{nA}$	$V_{(BR)SD}$	22	10	--	Volts
Drain – Substrate Breakdown Voltage	$V_{GB} = 0\text{ V}, I_D = 10\text{nA}$, Source Open	$V_{(BR)DBO}$	35	15	--	Volts
Source – Substrate Breakdown Voltage	$V_{GB} = 0\text{ V}, I_S = 10\mu\text{A}$, Drain Open	$V_{(BR)SBO}$	35	15	--	Volts
Drain – Source ON State Resistance ($I_D = 1\text{ mA}, V_{SB} = 0\text{ V}$)	$V_{GS} = 5\text{ V}$ $V_{GS} = 10\text{ V}$ $V_{GS} = 15\text{ V}$ $V_{GS} = 20\text{ V}$ $V_{GS} = 25\text{ V}$	$r_{DS(ON)}$	58 38 30 26 24	-- -- -- -- --	70 45 -- -- --	Ohms
Drain – Source Leakage	$V_{GS} = V_{BS} = -5\text{V}$ $V_{DS} = 10\text{V}$ $V_{DS} = 20\text{V}$	$I_{DS(off)}$	0.5 1.0	-- --	10 --	nA
Source – Drain Leakage	$V_{GD} = V_{BD} = -5\text{V}$ $V_{SD} = 10\text{V}$ $V_{SD} = 20\text{V}$	$I_{SD(off)}$	0.5 0.8	-- --	10 --	nA
Gate Leakage	$V_{DB} = V_{SB} = 0\text{ V}, V_{GB} = \pm 40\text{V}$	I_{GBS}	0.001	--	0.1	nA
Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1\mu\text{A}, V_{SB} = 0\text{V}$	$V_{GS(th)}$	0.8	0.5	2.0	Volts
Forward Transconductance	$V_{DS} = 10\text{V}, V_{SB} = 0\text{ V}, I_D = 20\text{mA}, f = 1\text{ kHz}$	g_{fs} g_{os}	11 0.9	10 --	-- --	mS
Gate Node Capacitance	$V_{DS} = 10\text{V}, f = 1\text{MHz}$ $V_{GS} = V_{BS} = -15\text{V}$	$C_{(GS+GD+GB)}$	2.5	--	3.5	pF
Drain Node Capacitance		$C_{(GD+GB)}$	1.1	--	1.5	pF
Source Node Capacitance		$C_{(GS+SB)}$	3.7	--	5.5	pF
Reverse Transfer Capacitance		$C_{rss} (C_{DG})$	0.2	--	0.5	pF
Turn ON Delay Time		$V_{SB} = 0\text{ V}, V_{IN} 0\text{ to }5\text{ V},$ $R_G = 25\ \Omega$ $V_{DD} = 5\text{ V}, R_L = 680\ \Omega$	$t_{d(on)}$	0.5	--	1
Rise Time	t_r		0.6	--	1	ns
Turn OFF Delay Time	$t_{d(off)}$		2	--	--	ns
Fall Time	t_f		6	--	--	ns

NOTES: * Pulse Test: Pulse Width = 100 μsec , Duty Cycle = 2%
 1/ For Ordering Information, Price, and Availability Contact Factory.
 2/ Screening per MIL-PRF-19500
 3/ Unless Otherwise Specified, All Electrical Characteristics @25°C

NOTE: All specifications are subject to change without notification.
 SSDI's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0035A

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