Solid State Devices, Inc.
14701 Firestone Blvd * La Mirada, CA 90638
Phone: (562) 404-4474 * Fax: (562) 404-1773
ssdi@ssdi-power.com * www.ssdi-power.com

SFF440J

8 AMP
N-Channel
Power MOSFET
500 Volts
0.86 Ω

DESIGNER'S DATA SHEET

Part Number / Ordering Information[1/]

SFF440 ___ ____

L — **Screening[2/]**
__ = Not Screened
TX = TX Level
TXV = TXV Level
S = S Level

L — **Package[3/]**
J = TO-257

Features:

- Rugged construction with polysilicon gate
- Low RDS(on) and high transconductance
- Excellent high temperature stability
- Very fast switching speed
- Fast recovery and superior dv/dt performance
- Increased reverse energy capability
- Low input and transfer capacitance for easy paralleling
- Hermetically sealed package
- Low inductance leads
- TX, TXV, S-Level screening available
- Replaces: IRF440 types

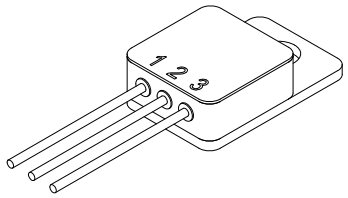
Maximum Ratings	Symbol	Value	Units
Drain - Source Voltage	V_{DS}	500	V
Gate - Source Voltage	V_{GS}	±20	V
Max. Continuous Drain Current (package limited) @ 25ºC	I_D	6.9	A
Operating & Storage Temperature	T_{OP} & T_{STG}	-55 to +150	ºC
Maximum Thermal Resistance (Junction to Case)	$R_{\theta JC}$	2	ºC/W
Total Power Dissipation @ T_C = 25ºC @ T_C = 55ºC	P_D	63 48	W

NOTES:

*Pulse Test: Pulse Width = 300µsec, Duty Cycle = 2%.

1/ For ordering information, price, and availability - contact factory.
2/ Screening based on MIL-PRF-19500. Screening flows available on request.
3/ Maximum current limited by package configuration
4/ Unless otherwise specified, all electrical characteristics @25°C.

TO-257



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.	**DATA SHEET #: F00087B**	**DOC**

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Electrical Characteristics[4/]		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	V_{GS} = 0V, I_D = 250 µA	BV_{DSS}	500	570	—	V
Drain to Source On State Resistance	V_{GS} = 10V, I_D = 60% Rated I_D	$R_{DS(on)}$	—	0.65	0.86	Ω
On State Drain Current	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ Max, V_{GS} = 10V	$I_{D(on)}$	8	12	—	A
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	$V_{GS(th)}$	2.0	3.2	4.0	V
Forward Transconductance	V_{DS} ≥ 50V, I_D = 60% Rated I_D	g_{fs}	4.9	6	—	S(℧)
Zero Gate Voltage **Drain Current**	V_{DS} = max rated voltage, V_{GS} = 0V V_{DS} = 80% Rated V_{DS}, V_{GS} = 0V, T_A = 125°C	I_{DSS}	— —	0.015 5	25 250	µA
Gate to Source Leakage Forward **Gate to Source Leakage Reverse**	At rated V_{GS}	I_{GSS}	— —	— —	100 -100	nA
Total Gate Charge **Gate to Source Charge** **Gate to Drain Charge**	V_{GS} = 10V 80% Rated V_{DS} I_D = 8A	Q_g Q_{gs} Q_{gd}	— — —	30 8 12	50 10 25	nC
Turn on Delay Time **Rise Time** **Turn off Delay Time** **Fall Time**	V_{DD} = 50% Rated V_{DS} I_D= 8 A R_G = 9.1Ω R_D = 30Ω	$t_{d(on)}$ t_r $t_{d(off)}$ t_f	— — — —	30 40 62 30	40 60 74 40	nsec
Diode Forward Voltage	I_S = Rated I_D, V_{GS} = 0V, T_j = 25°C	V_{SD}	—	0.85	1.2	V
Diode Reverse Recovery Time **Reverse Recovery Charge**	T_j = 25°C, I_F = Rated I_D, di/dt = 100A/usec	t_{rr} Q_{rr}	210 2	900 7.7	970 8.9	nsec µC
Input Capacitance **Output Capacitance** **Reverse Transfer Capacitance**	V_{GS} = 0V V_{DS} = 25V f = 1 MHz	C_{iss} C_{oss} C_{rss}	— — —	1450 180 40	— — —	pF

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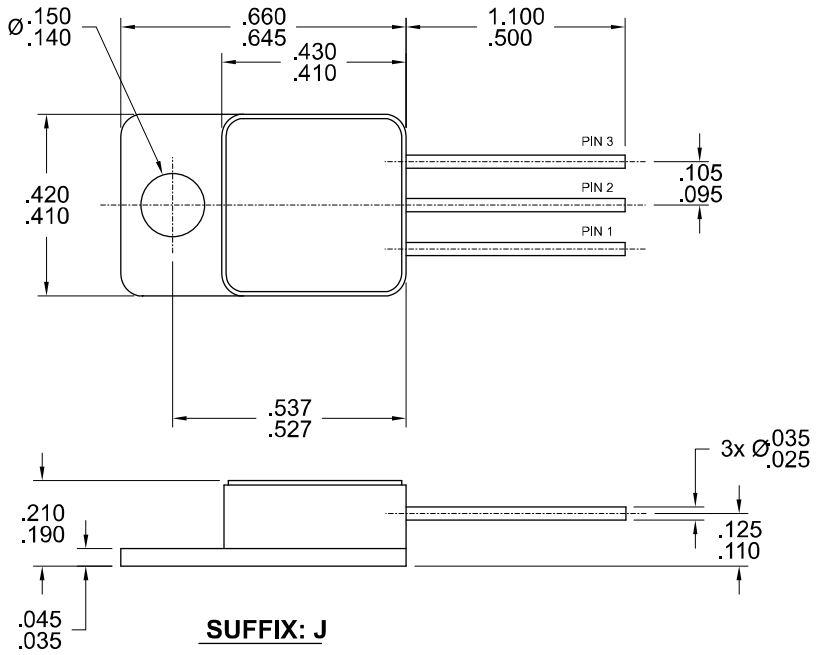
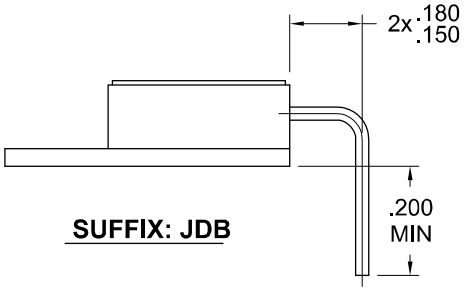
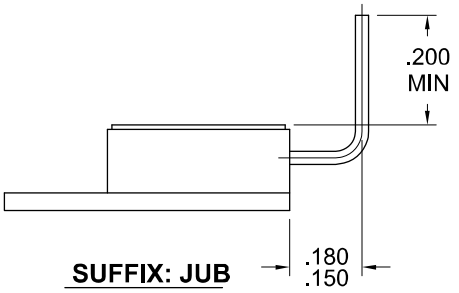
TO-254 (J)



SUFFIX: J



SUFFIX: JDB



SUFFIX: JUB

PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
TO-257 (J)	Pin 1	Pin 2	Pin 3