



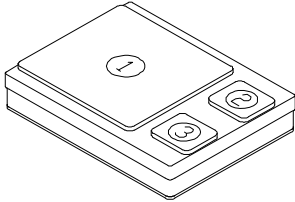
Solid State Devices, Inc.

14701 Firestone Blvd * La Mirada, Ca 90638
 Phone: (562) 404-4474 * Fax: (562) 404-1773
 ssdi@ssdi-power.com * www.ssdi-power.com

SFF44N50S1 SFF44N50S2

DESIGNER'S DATA SHEET

SMD1, 2

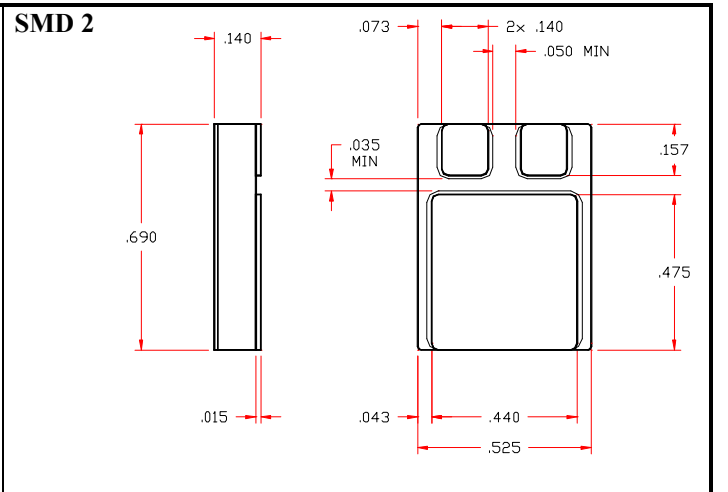
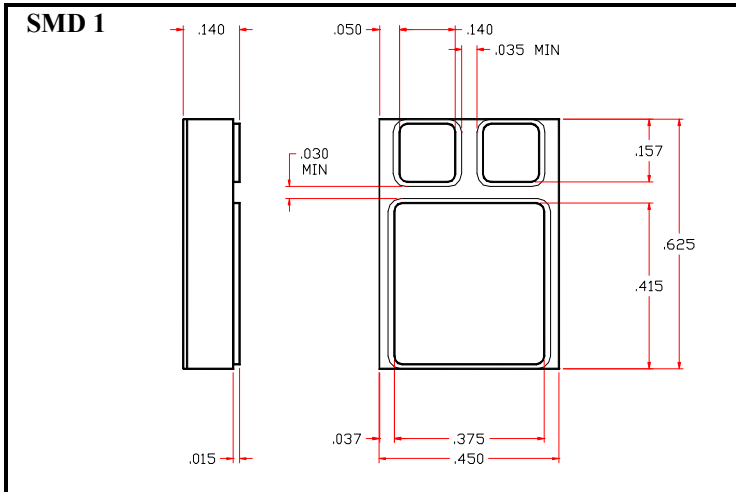


Note
1/ maximum current limited by package configuration

35 AMP, 500 Volts, 110 mΩ Avalanche Rated N-channel MOSFET

- Features:**
- Rugged poly-Si gate
 - Lowest ON-resistance in the industry
 - Avalanche rated
 - Hermetically Sealed, Hot Case power SMD
 - Low Total Gate Charge
 - Fast Switching
 - TX, TXV, S-Level screening available
 - Improved ($R_{DS(ON)}$ Q_G) figure of merit

Maximum Ratings	Symbol	Value	Units
Drain - Source Voltage	V_{DSS}	500	V
Gate – Source Voltage	V_{GS}	±30 ±40	V
Max. Continuous Drain Current (package limited)	@ $T_C = 25^\circ C$	I_{D1}	35
	@ $T_C = 125^\circ C$	I_{D2}	16
Pulsed Drain (Instantaneous) Current (T_j limited)	@ $T_C = 25^\circ C$	I_{D3}	50
Max. Avalanche current	@ $L = 0.1$ mH	I_{AR}	20
Single / Repetitive Avalanche Energy	@ $L = 0.1$ mH	E_{AS} / E_{AR}	1100 / 1
Total Power Dissipation	@ $T_C = 25^\circ C$	P_D	250
Operating & Storage Temperature		$T_{OP} \& T_{STG}$	-55 to +150
Maximum Thermal Resistance	Junction to Case	$R_{\theta JC}$	0.5 (typ 0.35)



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0031C

DOC



Solid State Devices, Inc.

14701 Firestone Blvd * La Mirada, Ca 90638
 Phone: (562) 404-4474 * Fax: (562) 404-1773
 ssdi@ssdi-power.com * www.ssdi-power.com

SFF44N50S1

SFF44N50S2

Electrical Characteristics ^{4/}		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	500	530	—	V
Drain to Source On State Resistance	$V_{GS} = 10V, I_D = 20A, T_j = 25^\circ C$ $V_{GS} = 10V, I_D = 12A, T_j = 125^\circ C$ $V_{GS} = 10V, I_D = 20A, T_j = 150^\circ C$	$R_{DS(on)}$	— — —	110 230 270	120 — —	mΩ
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1.8mA, T_j = 25^\circ C$ $V_{DS} = V_{GS}, I_D = 250\mu A, T_j = 25^\circ C$ $V_{DS} = V_{GS}, I_D = 250\mu A, T_j = -55^\circ C$ $V_{DS} = V_{GS}, I_D = 250\mu A, T_j = 125^\circ C$	$V_{GS(th)}$	2.1 — — —	3.0 2.7 3.2 1.9	3.9 — — —	V
Gate to Source Leakage	$V_{GS} = \pm 20V, T_j = 25^\circ C$ $V_{GS} = \pm 20V, T_j = 125^\circ C$	I_{GSS}	— —	10 30	±100 —	nA
Zero Gate Voltage Drain Current	$V_{DS} = 500V, V_{GS} = 0V, T_j = 25^\circ C$ $V_{DS} = 500V, V_{GS} = 0V, T_j = 125^\circ C$ $V_{DS} = 500V, V_{GS} = 0V, T_j = 150^\circ C$	I_{DSS}	— — —	0.01 2.0 10	25 — 250	μA μA μA
Forward Transconductance	$V_{DS} = 10V, I_D = 20A, T_j = 25^\circ C$	g_{fs}	10	30	—	Mho
Total Gate Charge	$V_{GS} = 10V$	Q_g	—	175	—	nC
Gate to Source Charge	$V_{DS} = 380V$	Q_{gs}	—	28	—	nC
Gate to Drain Charge	$I_D = 32A$	Q_{gd}	—	80	—	nC
Turn on Delay Time	$V_{GS} = 10V$	$t_{d(on)}$	—	30	—	nsec
Rise Time	$V_{DS} = 380V$	t_r	—	10	—	
Turn off Delay Time	$I_D = 32A$	$t_{d(off)}$	—	70	—	
Fall Time	$R_G = 2.7\Omega, pw = 3\mu s$	t_f	—	10	—	
Diode Forward Voltage	$I_F = 32A, V_{GS} = 0V$	V_{SD}	—	1.0	1.5	V
Diode Reverse Recovery Time	$I_F = 32A, di/dt = 100A/\mu sec$	t_{rr}	—	540	—	nsec
Peak Reverse Recovery Current		$I_{RM(rec)}$	—	45	—	A
Reverse Recovery Charge		Q_{rr}	—	12	—	μC
Input Capacitance	$V_{GS} = 0V$	C_{iss}	—	4500	—	pF
Output Capacitance	$V_{DS} = 25V$	C_{oss}	—	540	—	
Reverse Transfer Capacitance	$f = 1 MHz$	C_{rss}	—	100	—	

NOTES:

- * Pulse Test: Pulse Width = 300μsec, Duty Cycle = 2%.
- 1/ For Ordering Information, Price, and Availability Contact Factory.
- 2/ Screening per MIL-PRF-19500.
- 3/ For Package Outlines Contact Factory.
- 4/ Unless Otherwise Specified, All Electrical Characteristics @25°C.

Available Part Numbers:

Consult Factory

PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
SMD1	Pin 1	Pin 2	Pin 3
SMD2	Pin 1	Pin 2	Pin 3

NOTE: All specifications are subject to change without notification. SCDD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0031C

DOC