



PRELIMINARY

SOLID STATE DEVICES, INC

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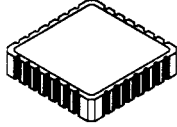
**SFF240-28**

**15 AMP  
200 VOLTS  
0.20Ω  
N-CHANNEL  
POWER MOSFET**

**Designer's Data Sheet**

- FEATURES:**
- Rugged construction with polysilicon gate
  - Low RDS(on) and high transconductance
  - Excellent high temperature stability
  - Very fast switching speed
  - Fast recovery and superior dv/dt performance
  - Increased reverse energy capability
  - Low input and transfer capacitance for easy paralleling
  - Ceramic Seals for improved hermeticity
  - Hermetically sealed surface mount package
  - TX, TXV and Space Level screening available
  - Replaces: IRF240 Types

**28 PIN CLCC**



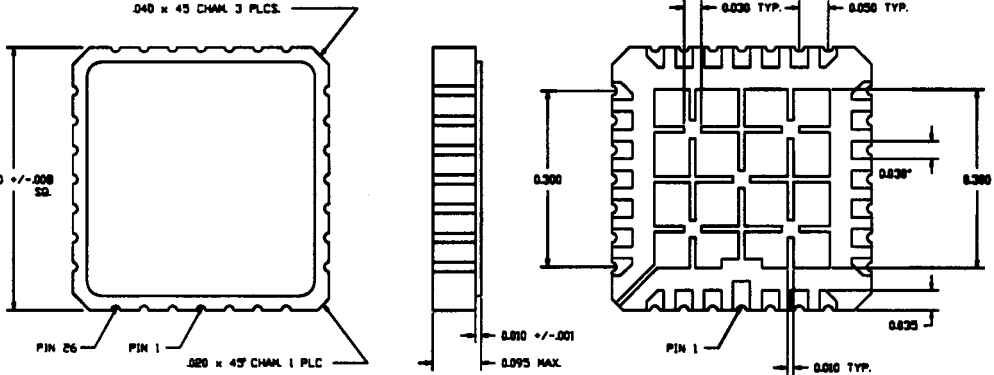
**MAXIMUM RATINGS**

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Drain to Source Voltage	V <sub>DS</sub>	200	Volts
Gate to Source Voltage	V <sub>GS</sub>	±20	Volts
Continuous Drain Current	I <sub>D</sub>	15	Amps
Operating and Storage Temperature	Top & Tstg	-55 to +150	°C
Thermal Resistance, Junction to Case	RθJC	3.5	°C/W
Total Device Dissipation @ TC=25°C	P <sub>D</sub>	36	Watts
Total Device Dissipation @ TC=80°C		20	

**PACKAGE OUTLINE: 28 PIN CLCC**

**PIN OUT:**  
**SOURCE: 1, 15-28**  
**DRAIN: 5-11**  
**GATE: 2, 3, 13, 14**

**NOTE:**  
**All Drain/Source pins must be connected on the PC Board in order to maximize current capability and minimize RDS(on)**



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

**DATA SHEET #: F00107 A**

**MED**

# SFF240-28

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## ELECTRICAL CHARACTERISTICS @ T<sub>J</sub>=25 C (Unless Otherwise Specified)

RATING	SYMBOL	MIN	TYP	MAX	UNIT
Drain to Source Breakdown Voltage (V <sub>GS</sub> =0 V, I <sub>D</sub> =250μA)	BV <sub>DSS</sub>	200	---	---	V
Drain to Source on State Resistance (V <sub>GS</sub> =10 V, I <sub>D</sub> = 9 A)	R <sub>DS(on)</sub>	---	0.13	0.20	Ω
On State Drain Current (V <sub>DS</sub> > I <sub>D(on)</sub> X R <sub>DS(on)</sub> Max, V <sub>GS</sub> =10 V)	I <sub>D(on)</sub>	15	---	---	A
Gate Threshold Voltage (V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA)	V <sub>GS(th)</sub>	2.0	---	4.0	V
Forward Transconductance (V <sub>DS</sub> ≥ 10 V, I <sub>DS</sub> = 9 A)	g <sub>fs</sub>	6.5	10	---	S(Ω)
Zero Gate Voltage Drain Current (V <sub>DS</sub> =max rated voltage, V <sub>GS</sub> =0 V) (V <sub>DS</sub> =80% rated V <sub>DS</sub> , V <sub>GS</sub> =0 V, T <sub>A</sub> =125°C)	I <sub>DSS</sub>	---	---	250 1000	μA
Gate to Source Leakage Forward Gate to Source Leakage Reverse	At rated V <sub>GS</sub> I <sub>gss</sub>	---	---	100 -100	nA
Total Gate Charge Gate to Source Charge Gate to Drain Charge	V <sub>GS</sub> =10 Volts 80% rated V <sub>DS</sub> Rated I <sub>D</sub> Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	---	40 7 21	60 10 32	nC
Turn on Delay Time Rise Time Turn Off Delay Time Fall Time	V <sub>DD</sub> =50% rated V <sub>DS</sub> 50% rated I <sub>D</sub> R <sub>G</sub> = 9.1 Ω R <sub>D</sub> = 5.6 t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub> t <sub>f</sub>	---	14 52 45 36	21 77 68 54	nsec
Diode Forward Voltage (I <sub>S</sub> =rated I <sub>D</sub> , V <sub>GS</sub> =0 V, T <sub>J</sub> =25°C)	V <sub>SD</sub>	---	---	2.0	V
Diode Reverse Recovery Time Reverse Recovery Charge	T <sub>J</sub> =25°C I <sub>F</sub> =rated I <sub>D</sub> di/dt=100 A/μsec t <sub>rr</sub> Q <sub>RR</sub>	120 1.3	250 2.6	530 5.6	nsec μC
Input Capacitance Output Capacitance Reverse Transfer Capacitance	V <sub>GS</sub> =0 Volts V <sub>DS</sub> =25 Volts f= 1 MHz C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	---	1300 380 93	---	pF

SAFE OPERATING AREA (S.O.A.)  
 T<sub>C</sub> = 25 C, D.C. CONDITION

