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RoHS 2002/95/EC

NTE2908
MOSFET
N–Channel, Enhancement Mode
High Speed Switch

Description:

The NTE2908 is a Power MOSFET in a TO220 type package that utilizes advanced processing techniques to achieve extremely low on–resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design provides an extremely efficient and reliable device for use in a wide variety of applications.

Features:

- Ultra Low ON–Resistance
- Dynamic dv/dt Rating
- +175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

Absolute Maximum Ratings:

Continuous Drain Current (V_{GS} = 10V), I_D
- T_C = +25°C 162A
- T_C = +100°C 115A

Pulsed Drain Current (Note 2), I_{DM} 650A

Power Dissipation (T_C = +25°C), P_D 200W
- Derate Linearly Above 25°C . . . . . 1.3W/°C

Gate–to–Source Voltage, V_{GS} . . . . . ±20V

Single Pulse Avalanche Energy (Note 3), E_{AS} 519mJ

Avalanche Current (Note 2), I_{AR} 95A

Repetitive Avalanche Energy (Note 2), E_{AR} 20mJ

Peak Diode Recovery dv/dt (Note 4), dv/dt 5.0V/ns

Operating Junction Temperature Range, T_J . . . . . –55° to +175°C

Storage Temperature Range, T_{stg} . . . . . –55° to +175°C

Lead Temperature (During Soldering, 1.6mm from case for 10sec), T_L . . . . . +300°C

Mounting Torque (6–32 or M3 Screw) . . . . . 10 lbf•in (1.1N•m)

Thermal Resistance, Junction–to–Case, R_{thJC} . . . . . 0.75°C/W

Thermal Resistance, Junction–to–Ambient, R_{thJA} . . . . . 62°C/W

Typical Thermal Resistance, Case–to–Sink (Flat, Greased Surface), R_{thCS} . . . . . 0.5°C/W

Note 1. Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

Note 2. Repetitive rating; pulse width limited by maximum junction temperature.

Note 3. Starting T_J = +25°C, L = 0.12mH, R_G = 25Ω, I_{AS} = 95A

Note 4. $I_{SD} \le 95A$, di/dt ≤ 150A/μs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le +175°C$

Electrical Characteristics: (T_J = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	40	–	–	V
Breakdown Voltage Temp. Coefficient	$\frac{\Delta V_{(BR)DSS}}{\Delta T_J}$	Reference to +25°C, I_D = 1mA	–	0.036	–	V/°C
Static Drain−to−Source On−Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 94A, Note 5	–	–	14	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = 10V, I_D = 250μA	2.0	–	4.0	V
Forward Transconductance	g_{fs}	V_{DS} = 25V, I_D = 60A	106	–	–	S
Drain−to−Source Leakage Current	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V	–	–	20	μA
		V_{DS} = 32V, V_{GS} = 0V, T_J = +150°C	–	–	250	μA
Gate−to−Source Forward Leakage	I_{GSS}	V_{GS} = 20V	–	–	200	nA
Gate−to−Source Reverse Leakage	I_{GSS}	V_{GS} = −20V	–	–	−200	nA
Total Gate Charge	Q_g	I_D = 95A, V_{DS} = 32V, V_{GS} = 10V, Note 5	–	160	200	nC
Gate−to−Source Charge	Q_{gs}		–	35	–	nC
Gate−to−Drain (“Miller”) Charge	Q_{gd}		–	42	60	nC
Turn−On Delay Time	$t_{d(on)}$	V_{DD} = 20V, I_D = 95A, R_G = 2.5Ω, R_D = 0.21Ω, Note 5	–	17	–	ns
Rise Time	t_r		–	140	–	ns
Turn−Off Delay Time	$t_{d(off)}$		–	72	–	ns
Fall Time	t_f		–	26	–	ns
Internal Drain Inductance	L_D	Between lead, .250in. (6.0) mm from package and center of die contact	–	4.5	–	nH
Internal Source Inductance	L_S		–	7.5	–	nH
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	7360	–	pF
Output Capacitance	C_{oss}		–	1680	–	pF
Reverse Transfer Capaticance	C_{rss}		–	240	–	pF
Output Capacitance	C_{oss}	V_{GS} = 0V, V_{DS} = 1.0V, f = 1MHz	–	6630	–	pF
		V_{GS} = 0V, V_{DS} = 32V, f = 1MHz	–	1490	–	pF
Effective Output Capacitance	C_{oss} eff.	V_{GS} = 0V, V_{DS} = 0V to 32V, Note 6	–	1540	–	pF

Source−Drain Ratings and Characteristics:

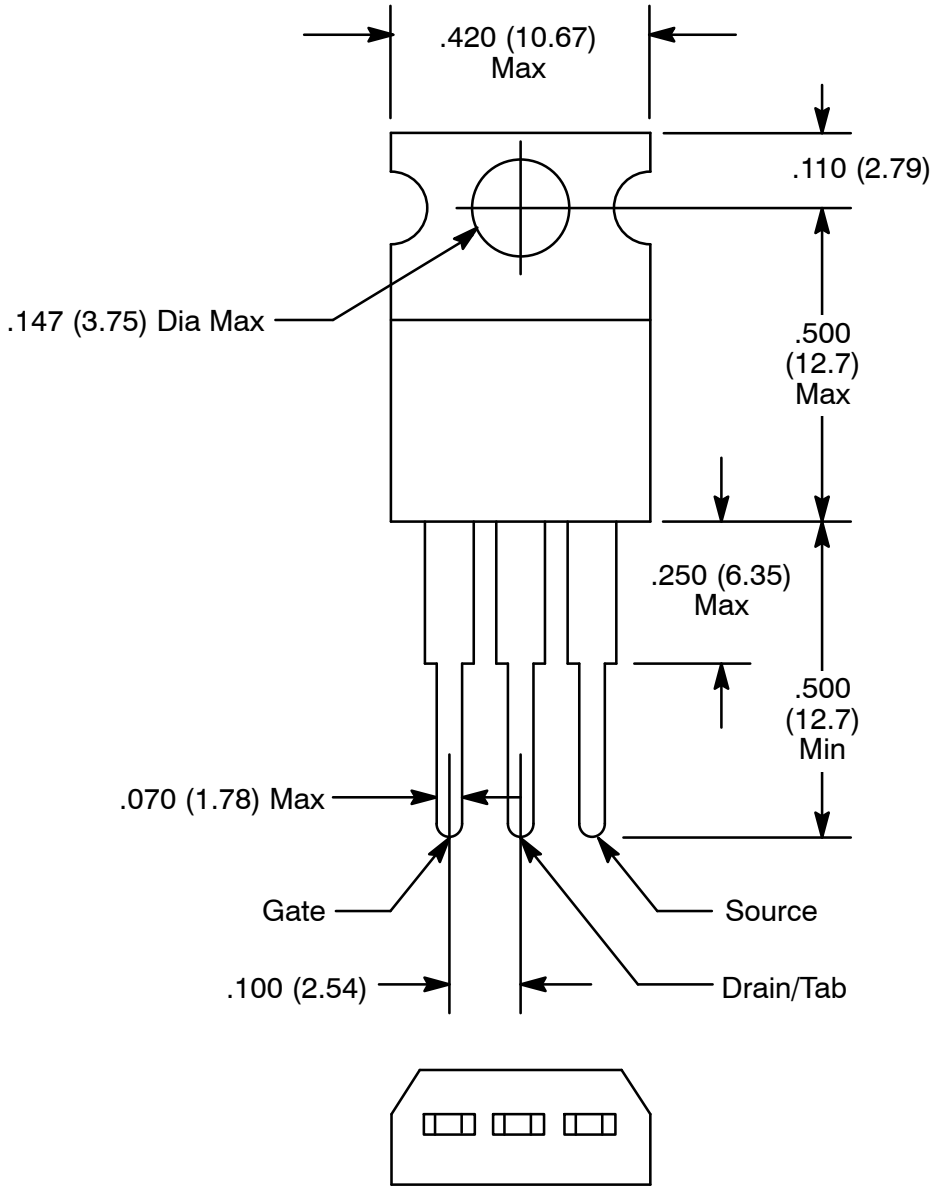
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Continuous Source Current (Body Diode)	I_S	Note 1	–	–	162	A
Pulsed Source Current (Body Diode)	I_{SM}	Note 2	–	–	650	A
Diode Forward Voltage	V_{SD}	T_J = +25°C, I_S = 95A, V_{GS} = 0V, Note 5	–	–	1.3	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 95A, di/dt = 100A/μs, Note 5	–	71	110	ns
Reverse Recovery Charge	Q_{rr}		–	180	270	μC
Forward Turn−On Time	t_{on}	Intrinsic turn−on time is neglegible (turn−on is dominated by L_S+L_D)				

Note 1. Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

Note 2. Repetitive rating; pulse width limited by maximum junction temperature.

Note 5. Pulse width ≤ 300μs; duty cycle ≤ 2%.

Note 6. C_{oss} eff. is a fixed capacitance that ives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.


.420 (10.67)
Max
.110 (2.79)
.147 (3.75) Dia Max
.500
(12.7)
Max
.250 (6.35)
Max
.500
(12.7)
Min
.070 (1.78) Max
Gate
Source
.100 (2.54)
Drain/Tab