

CMLDM7005  
CMLDM7005R

SURFACE MOUNT  
DUAL N-CHANNEL  
ENHANCEMENT-MODE  
SILICON MOSFET

PICOmini™



SOT-563 CASE



www.centrasemi.com

**DESCRIPTION:**

These CENTRAL SEMICONDUCTOR devices are dual N-Channel enhancement-mode silicon MOSFETs designed for high speed pulsed amplifier and driver applications. These MOSFETs offer very low  $r_{DS(ON)}$  and low threshold voltage. The CMLDM7005R utilizes a reverse pinout configuration for the gate and source terminals as compared to the CMLDM7005.

**MARKING CODES: CMLDM7005: CC7  
CMLDM7005R: C7R**

**FEATURES:**

- ESD protection up to 2kV
- 350mW power dissipation
- Very low  $r_{DS(ON)}$
- Low threshold voltage
- Logic level compatible
- Small, SOT-563 surface mount package
- Complementary dual P-Channel device: CMLDM8005

**APPLICATIONS:**

- Load switch / Level shifting
- Battery charging
- Boost switch
- Electro-luminescent backlighting

**MAXIMUM RATINGS:** ( $T_A=25^\circ\text{C}$ )

Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	8.0	V
Continuous Drain Current (Steady State - Note 1)	$I_D$	650	mA
Continuous Source Current (Body Diode)	$I_S$	280	mA
Maximum Pulsed Drain Current	$I_{DM}$	1.3	A
Power Dissipation (Note 1)	$P_D$	350	mW
Power Dissipation (Note 2)	$P_D$	300	mW
Power Dissipation (Note 2)	$P_D$	150	mW
Operating and Storage Junction Temperature	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$
Thermal Resistance (Note 1)	$\theta_{JA}$	357	$^\circ\text{C/W}$

**SYMBOL**

SYMBOL	UNITS
$V_{DS}$	V
$V_{GS}$	V
$I_D$	mA
$I_S$	mA
$I_{DM}$	A
$P_D$	mW
$P_D$	mW
$P_D$	mW
$T_J, T_{stg}$	$^\circ\text{C}$
$\theta_{JA}$	$^\circ\text{C/W}$

**ELECTRICAL CHARACTERISTICS PER TRANSISTOR:** ( $T_A=25^\circ\text{C}$  unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{GSSF}, I_{GSSR}$	$V_{GS}=4.5V, V_{DS}=0$			1.0	$\mu\text{A}$
$I_{DSS}$	$V_{DS}=16V, V_{GS}=0$			100	nA
$BV_{DSS}$	$V_{GS}=0, I_D=250\mu\text{A}$	20			V
$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.5		1.1	V
$V_{SD}$	$V_{GS}=0, I_S=200\text{mA}$			1.1	V
$r_{DS(ON)}$	$V_{GS}=4.5V, I_D=600\text{mA}$		0.14	0.23	$\Omega$
$r_{DS(ON)}$	$V_{GS}=2.5V, I_D=500\text{mA}$		0.2	0.275	$\Omega$
$r_{DS(ON)}$	$V_{GS}=1.8V, I_D=350\text{mA}$			0.7	$\Omega$
gFS	$V_{DS}=10V, I_D=400\text{mA}$	1.0			S

- Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 4.0mm<sup>2</sup>  
 (2) FR-4 Epoxy PC Board with copper mounting pad area of 4.0mm<sup>2</sup>  
 (3) FR-4 Epoxy PC Board with copper mounting pad area of 1.4mm<sup>2</sup>

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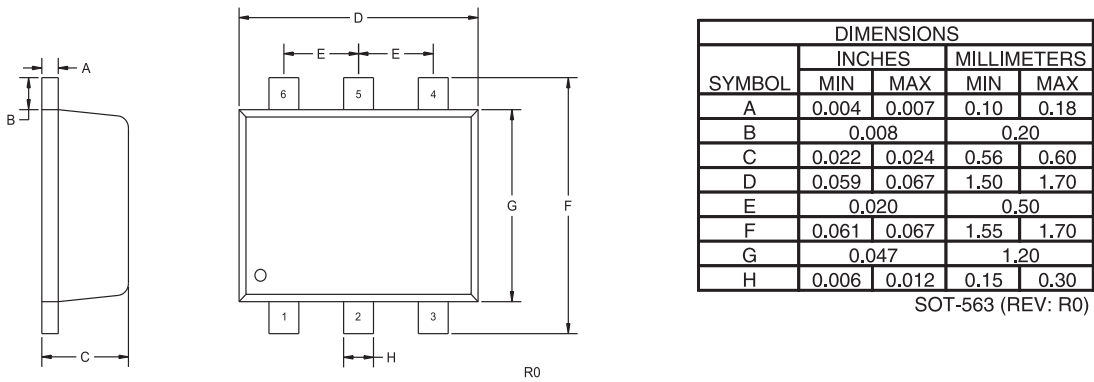
**SURFACE MOUNT  
DUAL N-CHANNEL  
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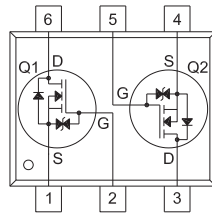
**ELECTRICAL CHARACTERISTICS PER TRANSISTOR - Continued:** ( $T_A=25^\circ\text{C}$  unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$C_{rss}$	$V_{DS}=16\text{V}$ , $V_{GS}=0$ , $f=1.0\text{MHz}$		18		pF
$C_{iss}$	$V_{DS}=16\text{V}$ , $V_{GS}=0$ , $f=1.0\text{MHz}$		100		pF
$C_{oss}$	$V_{DS}=16\text{V}$ , $V_{GS}=0$ , $f=1.0\text{MHz}$		16		pF
$Q_{g(\text{tot})}$	$V_{DS}=10\text{V}$ , $V_{GS}=4.5\text{V}$ , $I_D=500\text{mA}$		1.58		nC
$Q_{gs}$	$V_{DS}=10\text{V}$ , $V_{GS}=4.5\text{V}$ , $I_D=500\text{mA}$		0.17		nC
$Q_{gd}$	$V_{DS}=10\text{V}$ , $V_{GS}=4.5\text{V}$ , $I_D=500\text{mA}$		0.24		nC
$t_{on}$	$V_{DD}=10\text{V}$ , $V_{GS}=4.5\text{V}$ , $I_D=200\text{mA}$ , $R_G=10\Omega$		10		ns
$t_{off}$	$V_{DD}=10\text{V}$ , $V_{GS}=4.5\text{V}$ , $I_D=200\text{mA}$ , $R_G=10\Omega$		25		ns

**SOT-563 CASE - MECHANICAL OUTLINE**



**PIN CONFIGURATIONS**

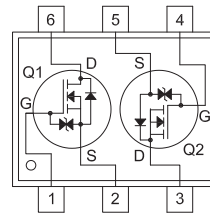


**CMLDM7005**

**LEAD CODE:**

- 1) Source Q1
- 2) Gate Q1
- 3) Drain Q2
- 4) Source Q2
- 5) Gate Q2
- 6) Drain Q1

**MARKING CODE: CC7**



**CMLDM7005R**

**LEAD CODE:**

- 1) Gate Q1
- 2) Source Q1
- 3) Drain Q2
- 4) Gate Q2
- 5) Source Q2
- 6) Drain Q1

**MARKING CODE: C7R**

R2 (25-October 2012)