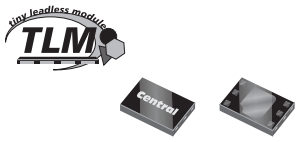
CTLDM7002A-M621H

SURFACE MOUNT
N-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET



Top View Bottom View

TLM621H CASE

• Device is ***Halogen Free*** by design

APPLICATIONS:
- Load/Power Switches
- Power Supply Converter Circuits
- Battery Powered Portable Equipment

Central Semiconductor Corp.

www.centralsemi.com

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLDM7002A-M621H is a very low profile (0.4mm) Silicon N-Channel Enhancement-mode MOSFET in a small, thermally efficient, 1.5mm x 2mm TLM™ package.

MARKING CODE: CND

FEATURES:
- Low $r_{DS(ON)}$
- Low $V_{DS(ON)}$
- Low Threshold Voltage
- Fast Switching
- Logic Level Compatible
- Small, Very Low Profile, TLM™

MAXIMUM RATINGS: (T_A=25°C)	**SYMBOL**		**UNITS**
Drain-Source Voltage	V_{DS}	60	V
Drain-Gate Voltage	V_{DG}	60	V
Gate-Source Voltage	V_{GS}	40	V
Continuous Drain Current	I_D	280	mA
Continuous Source Current (Body Diode)	I_S	280	mA
Maximum Pulsed Drain Current	I_{DM}	1.5	A
Maximum Pulsed Source Current	I_{SM}	1.5	A
Power Dissipation (Note 1)	P_D	1.6	W
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	°C
Thermal Resistance (Note 1)	Θ_{JA}	75	°C/W

ELECTRICAL CHARACTERISTICS: (T_A=25°C unless otherwise noted)

SYMBOL	**TEST CONDITIONS**	**MIN**	**MAX**	**UNITS**
I_{GSSF}, I_{GSSR}	V_{GS}=20V, V_{DS}=0		100	nA
I_{DSS}	V_{DS}=60V, V_{GS}=0		1.0	μA
I_{DSS}	V_{DS}=60V, V_{GS}=0, T_J=125°C		500	μA
$I_{D(ON)}$	V_{GS}=10V, V_{DS}=10V	500		mA
BV_{DSS}	V_{GS}=0, I_D=10μA	60		V
$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1.0	2.5	V
$V_{DS(ON)}$	V_{GS}=10V, I_D=500mA		1.0	V
$V_{DS(ON)}$	V_{GS}=5.0V, I_D=50mA		0.15	V
V_{SD}	V_{GS}=0, I_S=400mA		1.2	V

Notes: (1) Mounted on a 4-layer JEDEC test board with one thermal vias connecting the exposed thermal pad to the first buried plane. PCB was constructed as per JEDEC standards JESD51-5 and JESD51-7.

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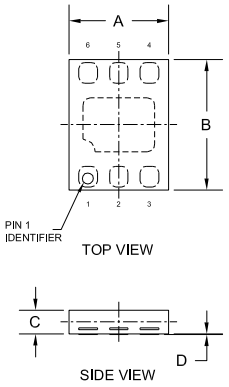
ELECTRICAL CHARACTERISTICS - Continued: (T_A=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
$r_{DS(ON)}$	V_{GS}=10V, I_D=500mA		2.0	Ω
$r_{DS(ON)}$	V_{GS}=10V, I_D=500mA, T_J=125°C		3.5	Ω
$r_{DS(ON)}$	V_{GS}=5.0V, I_D=50mA		3.0	Ω
$r_{DS(ON)}$	V_{GS}=5.0V, I_D=50mA, T_J=125°C		5.0	Ω
g_{FS}	V_{DS}=10V, I_D=200mA	80		mS
C_{rss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz		5.0	pF
C_{iss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz		50	pF
C_{oss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz		15	pF
t_{on}, t_{off}	V_{DD}=30V, V_{GS}=10V, I_D=200mA, R_G=25Ω, R_L=150Ω		20	ns

TLM621H CASE - MECHANICAL OUTLINE

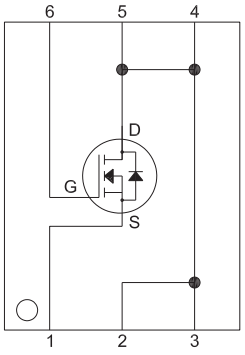


*Exposed pad P internally connected to pins 2, 3, 4, and 5.

DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.053	0.065	1.35	1.65
B	0.073	0.085	1.85	2.15
C	0.012	0.016	0.30	0.40
D	0.000	0.002	0.00	0.05
E	0.020		0.50	
F	0.008	0.012	0.20	0.30
G	0.027	0.035	0.69	0.89
H	0.053	0.057	1.35	1.45
J	0.039	0.047	0.99	1.19
K	0.011	0.015	0.28	0.38

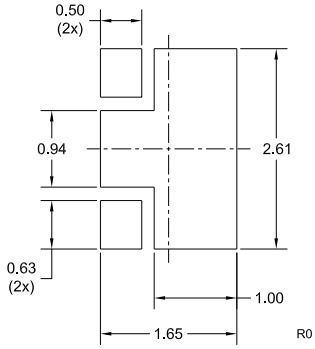
TLM621H (REV:R0)

PIN CONFIGURATION



OPTIONAL MOUNTING PADS

(Dimensions in mm)



For standard mounting refer to TLM621H Package Details

LEAD CODE:
1) Source
2) Drain
3) Drain
4) Drain
5) Drain
6) Gate

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