

## AOD466

### N-Channel Enhancement Mode Field Effect Transistor

#### General Description

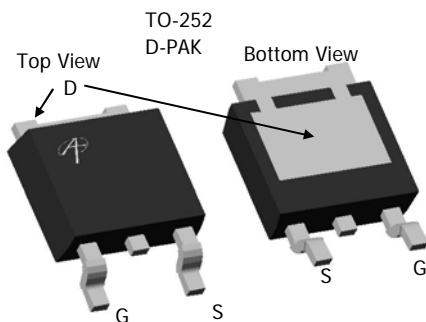
The AOD466 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

- RoHS Compliant
- Halogen Free\*

#### Features

$V_{DS} (V) = 25V$   
 $I_D = 30A (V_{GS} = 10V)$   
 $R_{DS(ON)} < 14 m\Omega (V_{GS} = 10V)$   
 $R_{DS(ON)} < 24 m\Omega (V_{GS} = 4.5V)$

**100% UIS Tested!**  
**100% Rg Tested!**



#### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	25	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>G</sup>	$T_C=25^\circ C$	30	A
		$T_C=100^\circ C$	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	70	
Avalanche Current <sup>C</sup>	$I_{AR}$	20	A
Repetitive avalanche energy 0.1mH <sup>C</sup>	$E_{AR}$	20	mJ
Power Dissipation <sup>B</sup>	$T_C=25^\circ C$	30	W
		$T_C=100^\circ C$	
Power Dissipation <sup>A</sup>	$T_A=25^\circ C$	2.5	W
		$T_A=70^\circ C$	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ C$

#### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units	
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	$t \leq 10s$	15	20	$^\circ C/W$
		Steady-State	41	50	$^\circ C/W$
Maximum Junction-to-Case <sup>B</sup>	$R_{\theta JC}$	3.6	5	$^\circ C/W$	

Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$ , $V_{GS}=0\text{V}$	25			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=20\text{V}$ , $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1	$\mu\text{A}$
					5	
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 20\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	1	1.8	2.5	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$ , $V_{DS}=5\text{V}$	70			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$ , $I_D=30\text{A}$ $T_J=125^\circ\text{C}$		11.1	14	m $\Omega$
				15.5		
				19	24	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=5\text{V}$ , $I_D=30\text{A}$		30		S
$V_{SD}$	Diode Forward Voltage	$I_S=1\text{A}$ , $V_{GS}=0\text{V}$		0.74	1	V
$I_S$	Maximum Body-Diode Continuous Current				25	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=12.5\text{V}$ , $f=1\text{MHz}$		830	1000	pF
$C_{oss}$	Output Capacitance			224		pF
$C_{rss}$	Reverse Transfer Capacitance			127		pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$		0.93	1.5	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$ , $V_{DS}=12.5\text{V}$ , $I_D=30\text{A}$		15.3	19	nC
$Q_g(4.5\text{V})$	Total Gate Charge			7.4	9	nC
$Q_{gs}$	Gate Source Charge			2.7		nC
$Q_{gd}$	Gate Drain Charge			4.3		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$ , $V_{DS}=12.5\text{V}$ , $R_L=0.42\Omega$ , $R_{GEN}=3\Omega$		8		ns
$t_r$	Turn-On Rise Time			11.7		ns
$t_{D(off)}$	Turn-Off DelayTime			30		ns
$t_f$	Turn-Off Fall Time			11		ns
$t_{rr}$	Body Diode Reverse Recovery Time		$I_F=30\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		23.5	30
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=30\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		12.8		nC

A: The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation  $P_{DSM}$  is based on  $R_{\theta JA}$  and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any given application depends on the user's specific board design, and the maximum temperature of  $175^\circ\text{C}$  may be used if the PCB allows it.

B: The power dissipation  $P_D$  is based on  $T_{J(MAX)}=175^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=175^\circ\text{C}$ .

D: The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to case  $R_{\theta JC}$  and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using  $<300 \mu\text{s}$  pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(MAX)}=175^\circ\text{C}$ .

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The SOA curve provides a single pulse rating.

\*This device is guaranteed green after data code 8X11 (Sep 1<sup>ST</sup> 2008).

Rev1: Sep. 2008

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

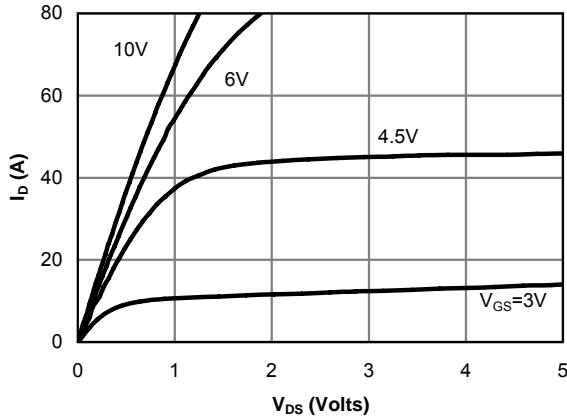


Fig 1: On-Region Characteristics

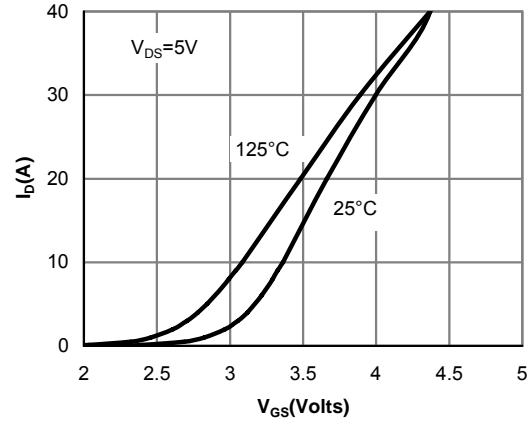


Figure 2: Transfer Characteristics

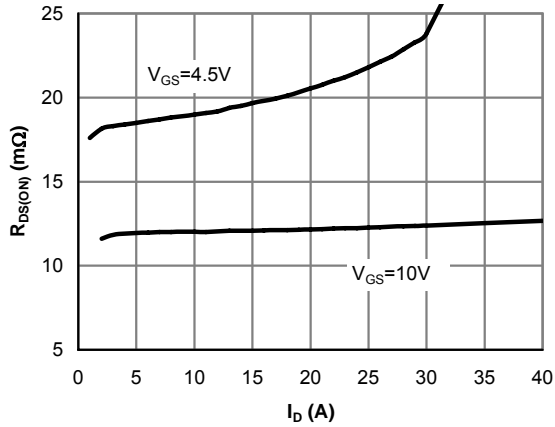


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

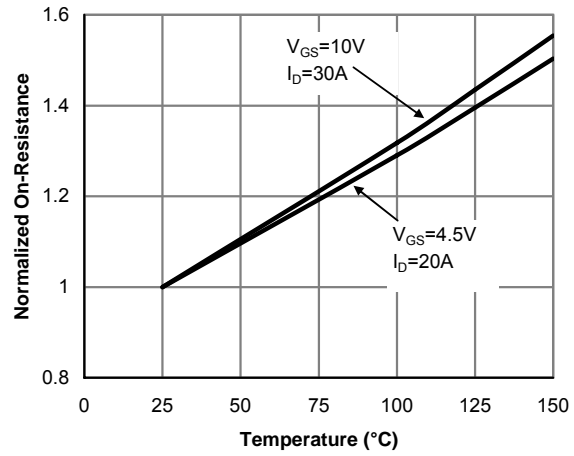


Figure 4: On-Resistance vs. Junction Temperature

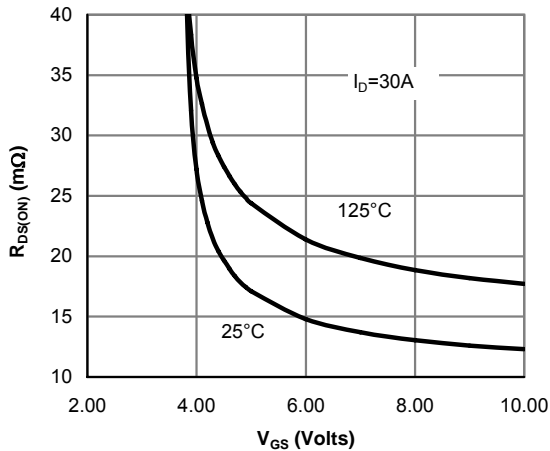


Figure 5: On-Resistance vs. Gate-Source Voltage

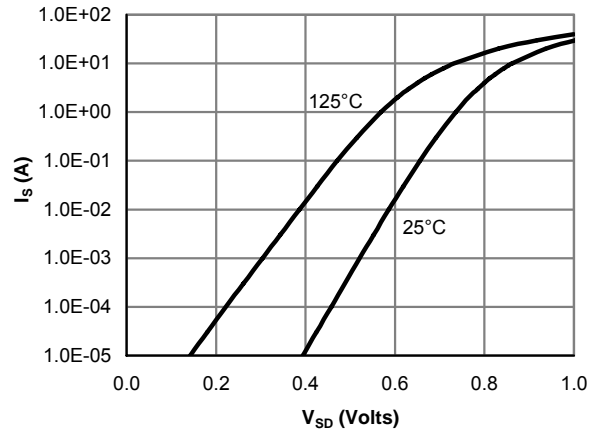


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

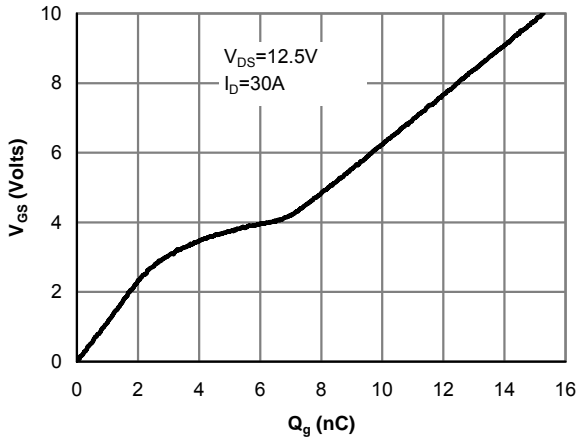


Figure 7: Gate-Charge Characteristics

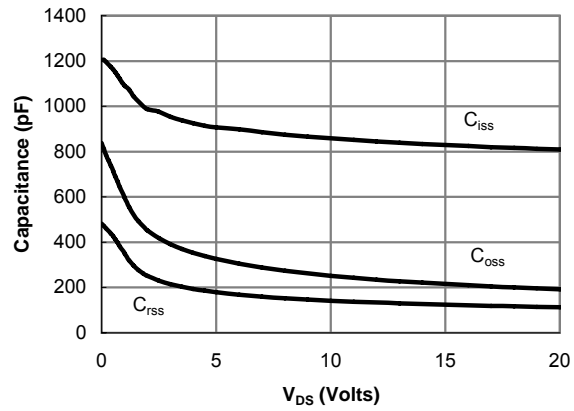


Figure 8: Capacitance Characteristics

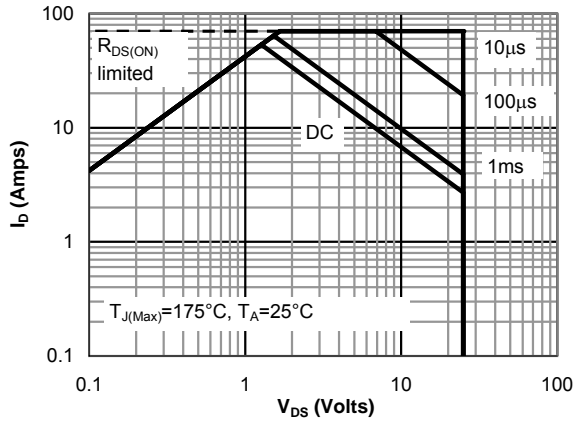


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

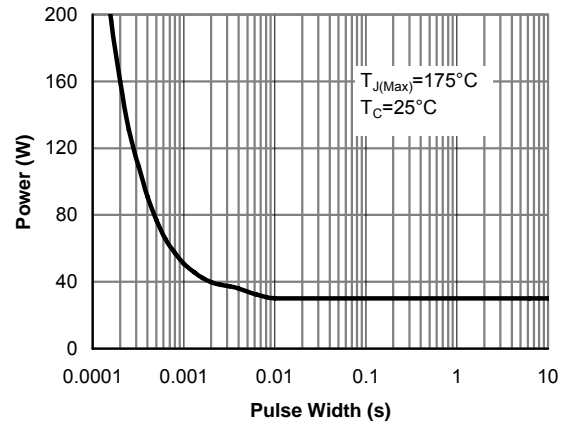


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

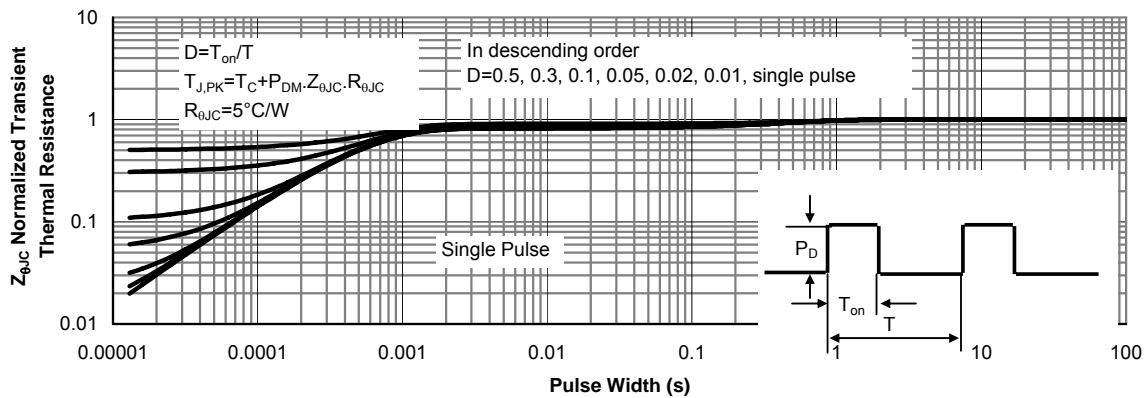


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

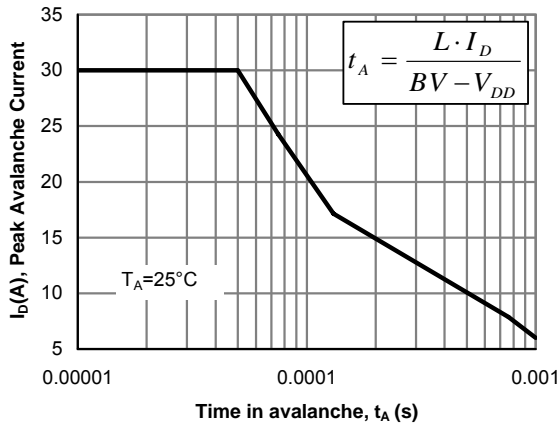


Figure 12: Single Pulse Avalanche capability

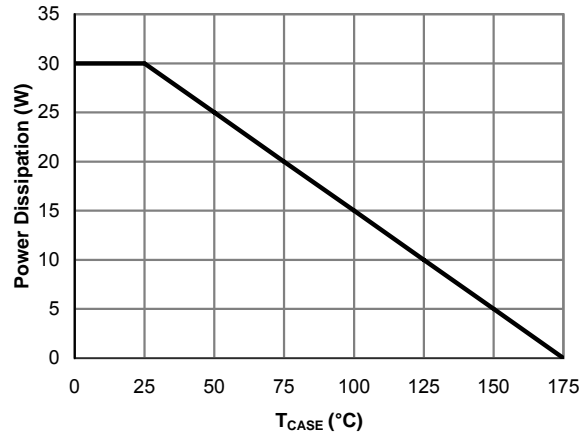


Figure 13: Power De-rating (Note B)

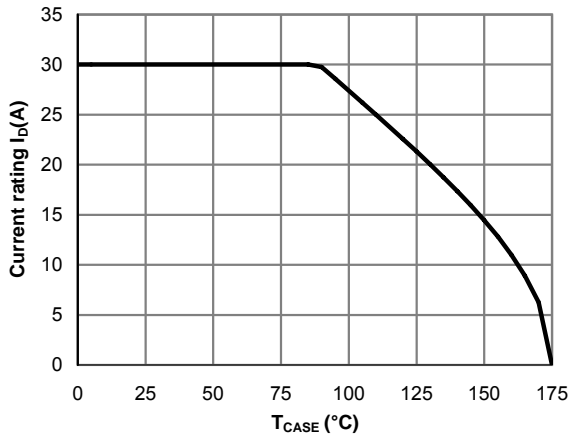


Figure 14: Current De-rating (Note B)

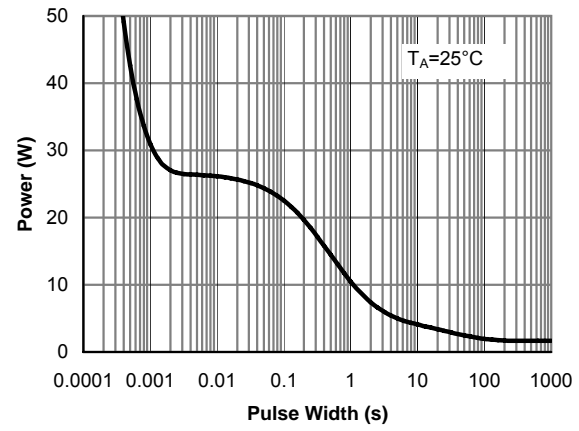


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

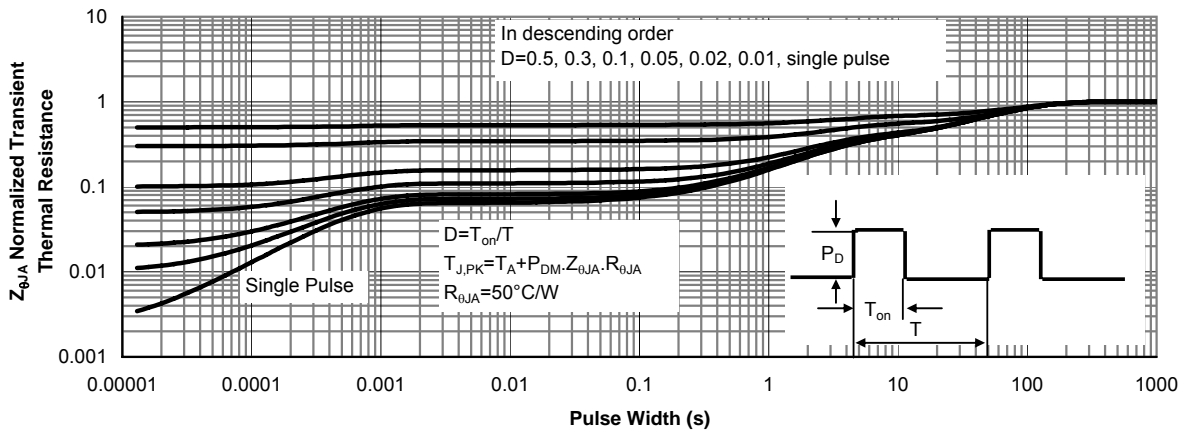
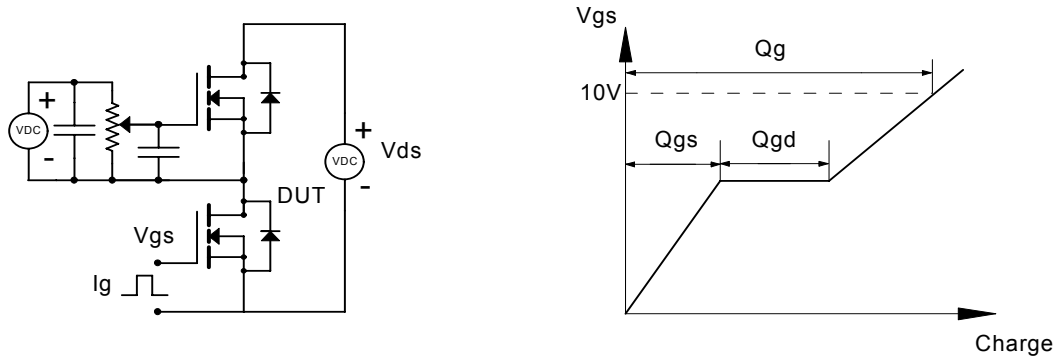
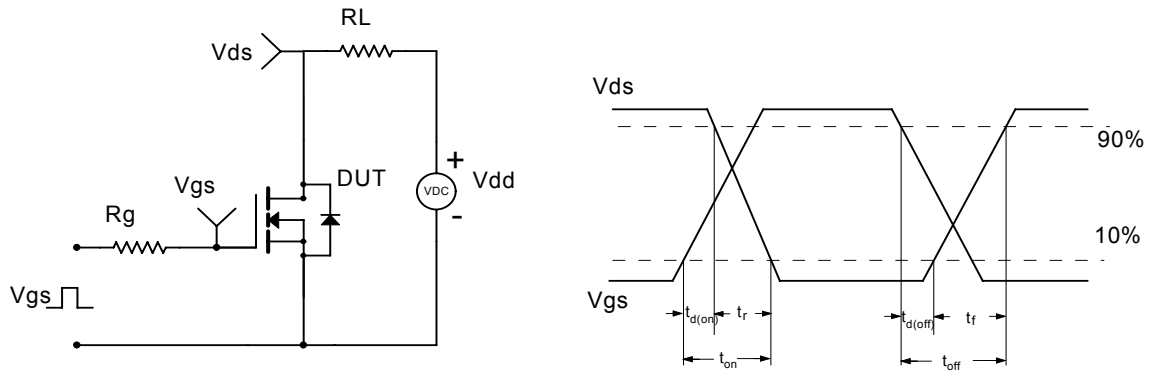


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

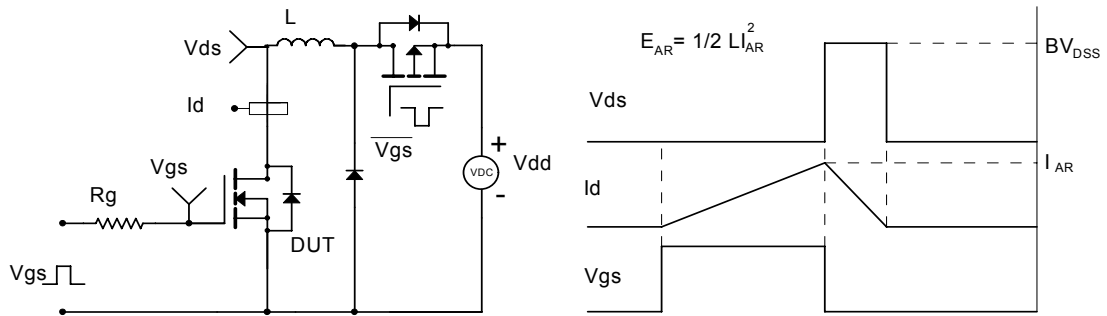
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

