



AON5800

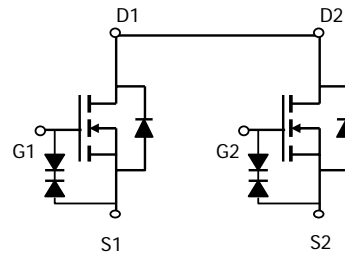
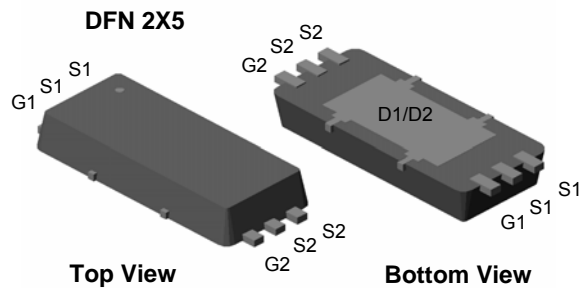
Common-Drain Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

The AON5800 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.8V while retaining a 12V $V_{GS(MAX)}$ rating. It is ESD protected. This device is suitable for use as a uni-directional or bi-directional load switch, facilitated by its common-drain configuration. *Standard Product AON5800 is Pb-free (meets ROHS & Sony 259 specifications). AON5800L is a Green Product ordering option. AON5800 and AON5800L are electrically identical.*

Features

$V_{DS} (V) = 20V$
 $I_D = 8 A (V_{GS} = 10V)$
 $R_{DS(ON)} < 16 m\Omega (V_{GS} = 10V)$
 $R_{DS(ON)} < 20 m\Omega (V_{GS} = 4.5V)$
 $R_{DS(ON)} < 21 m\Omega (V_{GS} = 4.0V)$
 $R_{DS(ON)} < 22 m\Omega (V_{GS} = 3.1V)$
 $R_{DS(ON)} < 27 m\Omega (V_{GS} = 2.5V)$
 $R_{DS(ON)} < 45 m\Omega (V_{GS} = 1.8V)$
 ESD Rating: 2000V HBM



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

| Parameter | Symbol | Maximum | Units |
|---|----------------|-------------------------|------------|
| Drain-Source Voltage | V_{DS} | 20 | V |
| Gate-Source Voltage | V_{GS} | ± 12 | |
| Continuous Drain Current $R_{\theta JA}=75^\circ C/W$ | I_D | $T_A=25^\circ C$ 8 | A |
| | | $T_A=70^\circ C$ 6.3 | |
| Pulsed Drain Current ^B | I_{DM} | 45 | |
| Power Dissipation ^A $R_{\theta JA}=75^\circ C/W$ | P_{DSM} | $T_A=25^\circ C$ 1.6 | W |
| | | $T_A=70^\circ C$ 1.0 | |
| Junction and Storage Temperature Range | T_J, T_{STG} | -55 to 150 | $^\circ C$ |

Thermal Characteristics

| Parameter | Symbol | Typ | Max | Units |
|---|-----------------|-----|-----|--------------|
| Maximum Junction-to-Ambient ^A $t \leq 10s$ | $R_{\theta JA}$ | 30 | 40 | $^\circ C/W$ |
| Maximum Junction-to-Ambient ^A Steady-State | | 61 | 75 | $^\circ C/W$ |
| Maximum Junction-to-Case ^B Steady-State | $R_{\theta JC}$ | 4.5 | 6 | $^\circ C/W$ |

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------|---------------------------------------|--|----------|----------|----------|------------------|
| STATIC PARAMETERS | | | | | | |
| BV_{DSS} | Drain-Source Breakdown Voltage | $I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$ | 20 | | | V |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS}=16\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$ | | | 1 5 | μA |
| I_{GSS} | Gate-Body leakage current | $V_{DS}=0\text{V}$, $V_{GS}=\pm 10\text{V}$ | | | 10 | μA |
| BV_{GSO} | Gate-Source Breakdown Voltage | $V_{DS}=0\text{V}$, $I_G=\pm 250\mu\text{A}$ | ± 12 | | | V |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$ | 0.5 | 0.73 | 1 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$ | 30 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}=10\text{V}$, $I_D=8\text{A}$ $T_J=125^\circ\text{C}$ | | 13 18 | 16 22 | $\text{m}\Omega$ |
| | | $V_{GS}=4.5\text{V}$, $I_D=7\text{A}$ | | 16 | 20 | $\text{m}\Omega$ |
| | | $V_{GS}=4.0\text{V}$, $I_D=6\text{A}$ | | 17 | 21 | $\text{m}\Omega$ |
| | | $V_{GS}=3.1\text{V}$, $I_D=6\text{A}$ | | 18 | 22 | $\text{m}\Omega$ |
| | | $V_{GS}=2.5\text{V}$, $I_D=6\text{A}$ | | 22 | 27 | $\text{m}\Omega$ |
| | | $V_{GS}=1.8\text{V}$, $I_D=4.5\text{A}$ | | 35 | 45 | $\text{m}\Omega$ |
| g_{FS} | Forward Transconductance | $V_{DS}=5\text{V}$, $I_D=8\text{A}$ | | 28 | | S |
| V_{SD} | Diode Forward Voltage | $I_S=1\text{A}$, $V_{GS}=0\text{V}$ | 0.5 | 0.74 | 1 | V |
| I_S | Maximum Body-Diode Continuous Current | | | | 2.5 | A |
| DYNAMIC PARAMETERS | | | | | | |
| C_{iss} | Input Capacitance | $V_{GS}=0\text{V}$, $V_{DS}=10\text{V}$, $f=1\text{MHz}$ | | 1330 | | pF |
| C_{oss} | Output Capacitance | | | 182 | | pF |
| C_{rss} | Reverse Transfer Capacitance | | | 161 | | pF |
| R_g | Gate resistance | $V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$ | | 1.5 | | Ω |
| SWITCHING PARAMETERS | | | | | | |
| $Q_g(4.5\text{V})$ | Total Gate Charge | $V_{GS}=4.5\text{V}$, $V_{DS}=10\text{V}$, $I_D=8\text{A}$ | | 13.1 | | nC |
| Q_{gs} | Gate Source Charge | | | 2 | | nC |
| Q_{gd} | Gate Drain Charge | | | 3.9 | | nC |
| $t_{D(on)}$ | Turn-On Delay Time | $V_{GS}=5\text{V}$, $V_{DS}=10\text{V}$, $R_L=1.25\Omega$, $R_{GEN}=3\Omega$ | | 6.2 | | ns |
| t_r | Turn-On Rise Time | | | 11 | | ns |
| $t_{D(off)}$ | Turn-Off Delay Time | | | 40.5 | | ns |
| t_f | Turn-Off Fall Time | | | 10 | | ns |
| t_{rr} | Body Diode Reverse Recovery Time | $I_F=8\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$ | | 18.8 | | ns |
| Q_{rr} | Body Diode Reverse Recovery Charge | $I_F=8\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$ | | 8.1 | | nC |

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using 80 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

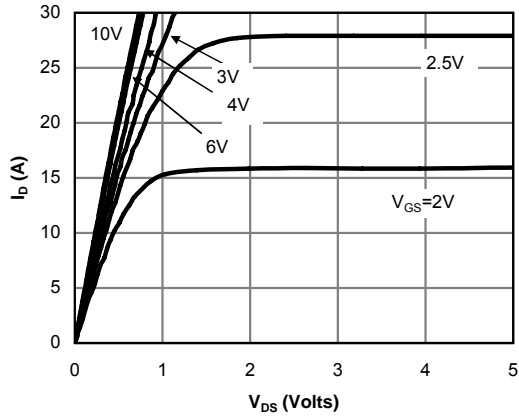


Fig 1: On-Region Characteristics

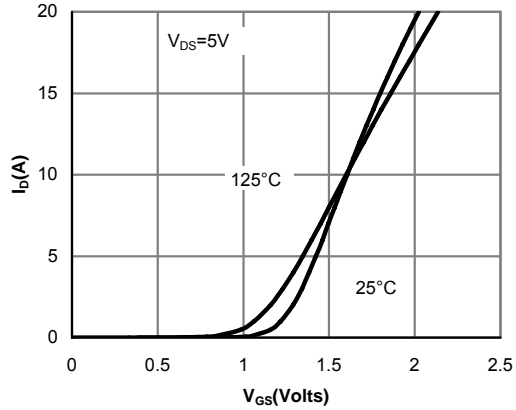


Figure 2: Transfer Characteristics

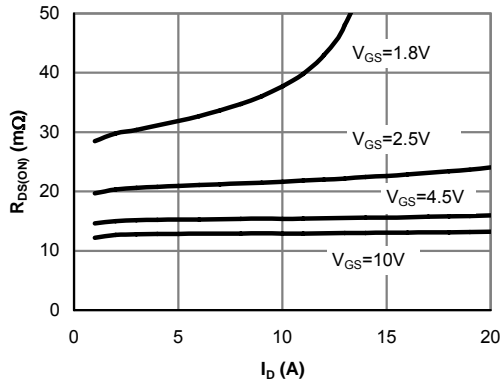


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

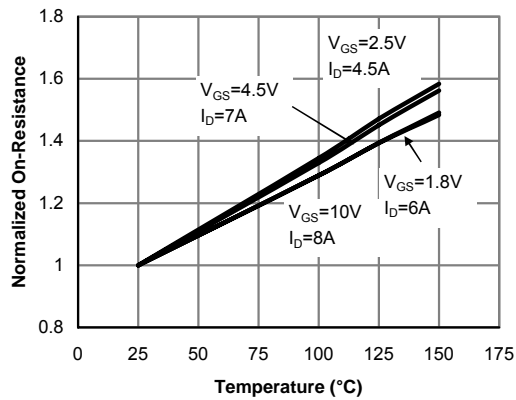


Figure 4: On-Resistance vs. Junction Temperature

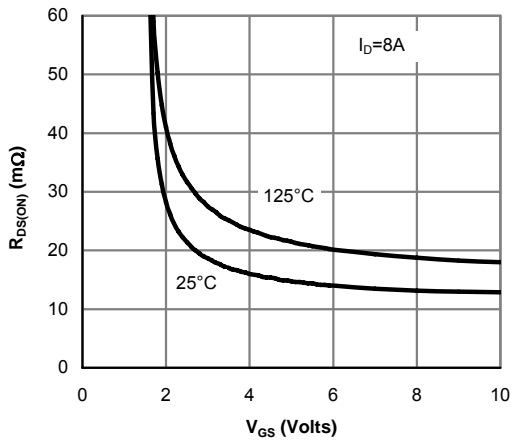


Figure 5: On-Resistance vs. Gate-Source Voltage

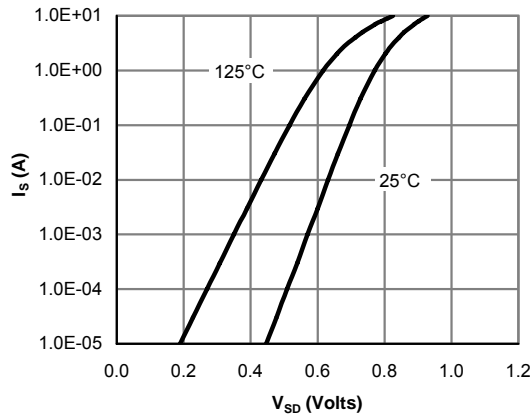


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

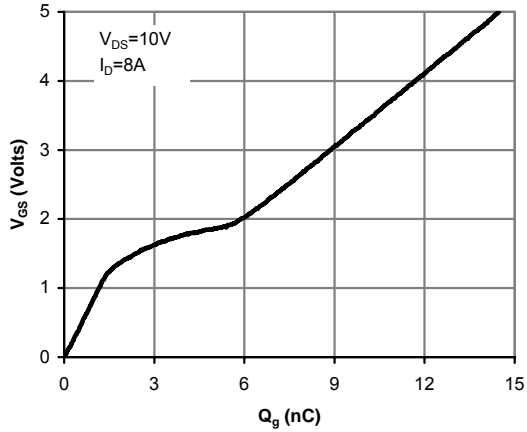


Figure 7: Gate-Charge Characteristics

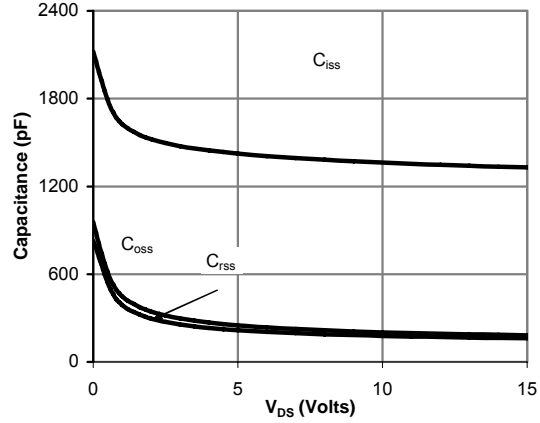


Figure 8: Capacitance Characteristics

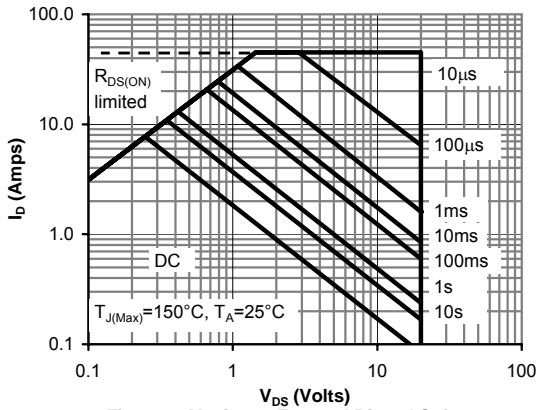


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

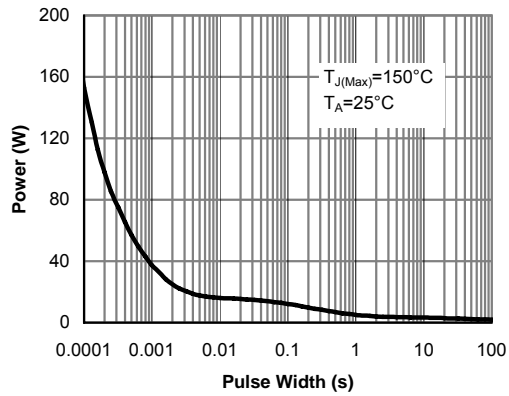


Figure 10: Single Pulse Power Rating Junction-to-Case (Note E)

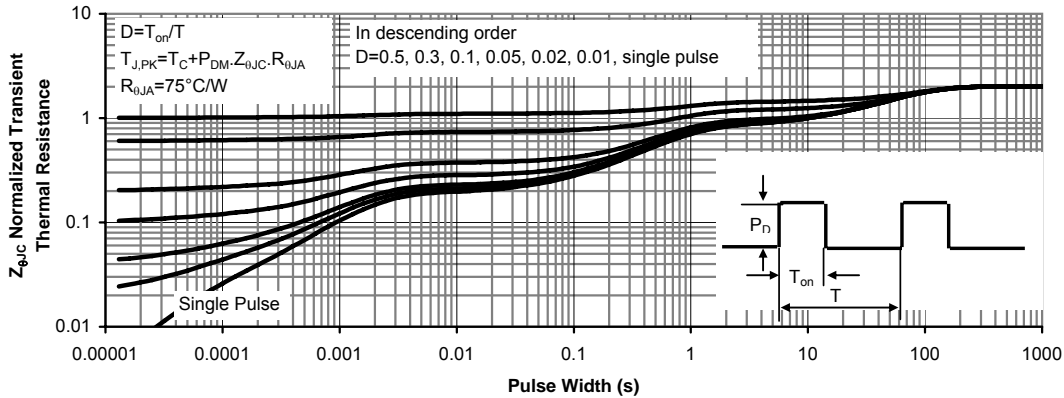


Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)