



AO4609

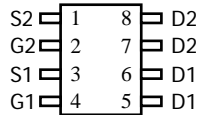
Complementary Enhancement Mode Field Effect Transistor

General Description

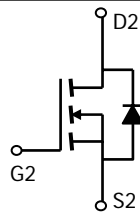
The AO4609 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications. *Standard Product AO4609 is Pb-free (meets ROHS & Sony 259 specifications). AO4609L is a Green Product ordering option. AO4609 and AO4609L are electrically identical.*

Features

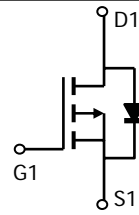
n-channel	p-channel
$V_{DS} (V) = 30V$	-30V
$I_D = 8.5A (V_{GS}=10V)$	-3A ($V_{GS} = -10V$)
$R_{DS(ON)}$	$R_{DS(ON)}$
< 18m Ω ($V_{GS}=10V$)	< 130m Ω ($V_{GS} = -10V$)
< 28m Ω ($V_{GS}=4.5V$)	< 180m Ω ($V_{GS} = -4.5V$)
	< 260m Ω ($V_{GS} = -2.5V$)



SOIC-8



n-channel



p-channel

Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	± 20	± 12	V
Continuous Drain Current ^A	$T_A=25^\circ C$	8.5	-3	A
Pulsed Drain Current ^B	I_{DM}	40	-6	
Power Dissipation	$T_A=25^\circ C$	2	2	
				$T_A=70^\circ C$
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	-55 to 150	$^\circ C$

Thermal Characteristics: n-channel and p-channel

Parameter	Symbol	Device	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$t \leq 10s$	n-ch	48	62.5	$^\circ C/W$
Maximum Junction-to-Ambient ^A					
Maximum Junction-to-Lead ^C	Steady-State	n-ch	35	40	$^\circ C/W$
Maximum Junction-to-Ambient ^A	$t \leq 10s$	p-ch	56	62.5	$^\circ C/W$
Maximum Junction-to-Ambient ^A					
Maximum Junction-to-Lead ^C	Steady-State	p-ch	40	48	$^\circ C/W$

N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=24\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1	μA
					5	
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1	1.8	3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=8.5\text{A}$ $T_J=125^\circ\text{C}$		15.5	18	m Ω
				22.3	27	
					23	28
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=8.5\text{A}$		23		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.75	1	V
I_S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C_{ISS}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=15\text{V}$, $f=1\text{MHz}$		1040	1250	pF
C_{OSS}	Output Capacitance			180		pF
C_{RSS}	Reverse Transfer Capacitance			110		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		0.7	0.85	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $I_D=8.5\text{A}$		19.2	23	nC
$Q_g(4.5\text{V})$	Total Gate Charge			9.36	11.2	nC
Q_{gs}	Gate Source Charge			2.6		nC
Q_{gd}	Gate Drain Charge			4.2		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $R_L=1.8\Omega$, $R_{GEN}=3\Omega$		5.2	7.5	ns
t_r	Turn-On Rise Time			4.4	6.5	ns
$t_{D(off)}$	Turn-Off DelayTime			17.3	25	ns
t_f	Turn-Off Fall Time			3.3	5	ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=8.5\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		16.7	21	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=8.5\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		6.7	10	nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $\leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using 80 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

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N-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

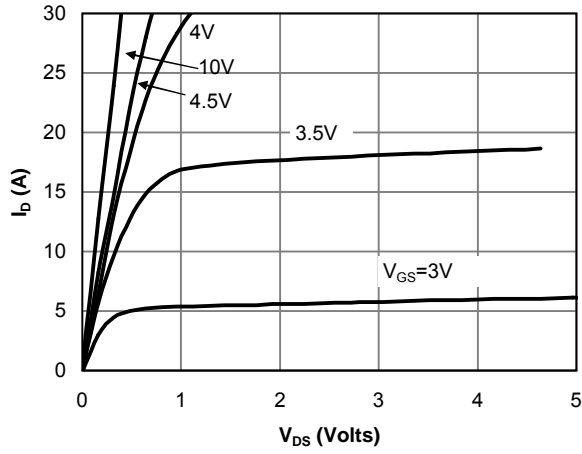


Fig 1: On-Region Characteristics

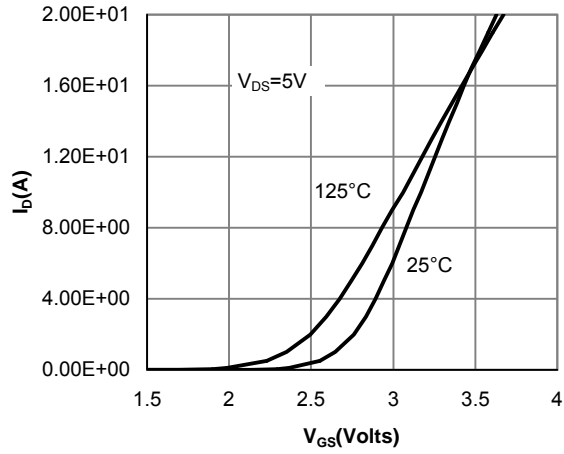


Figure 2: Transfer Characteristics

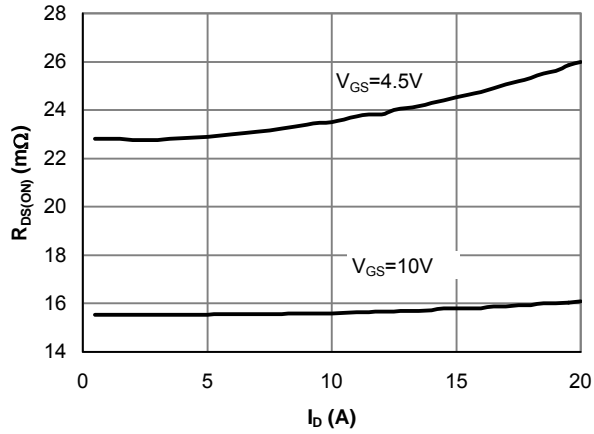


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

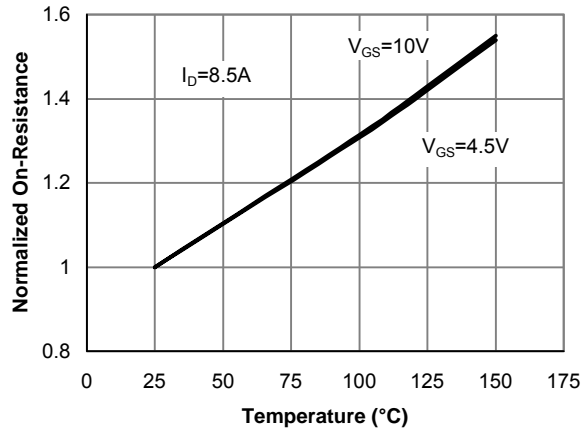


Figure 4: On-Resistance vs. Junction Temperature

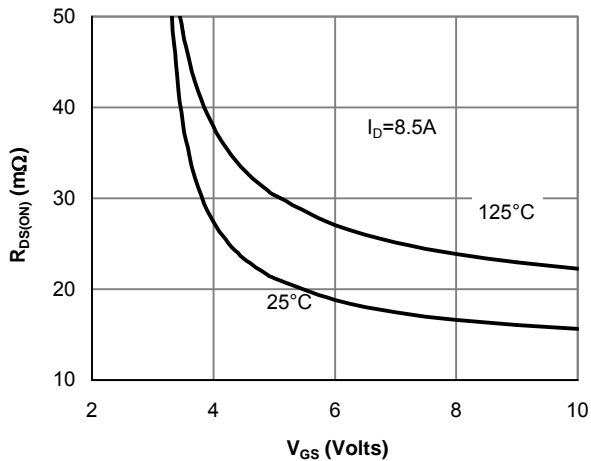


Figure 5: On-Resistance vs. Gate-Source Voltage

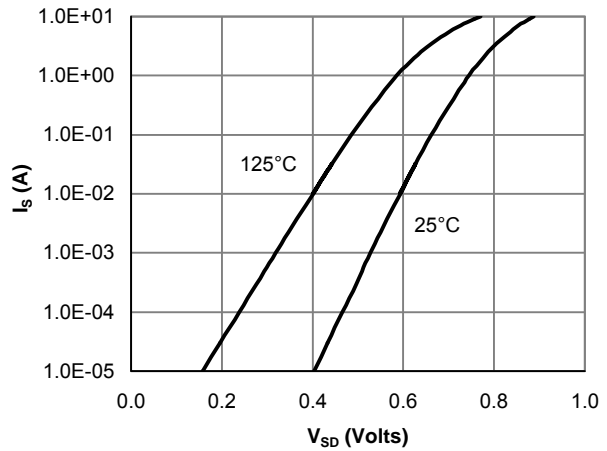


Figure 6: Body-Diode Characteristics

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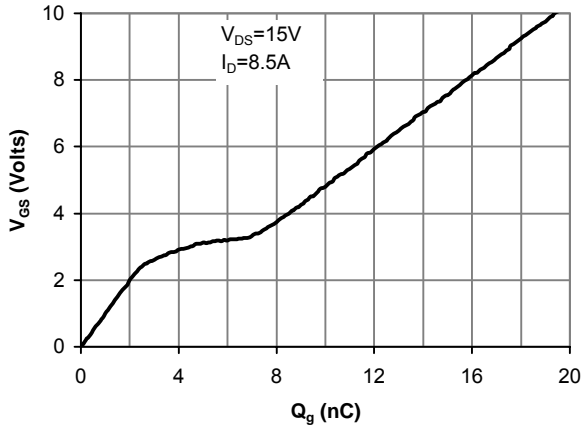


Figure 7: Gate-Charge Characteristics

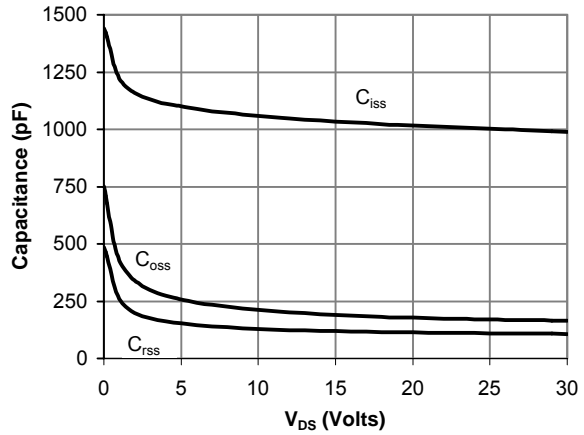


Figure 8: Capacitance Characteristics

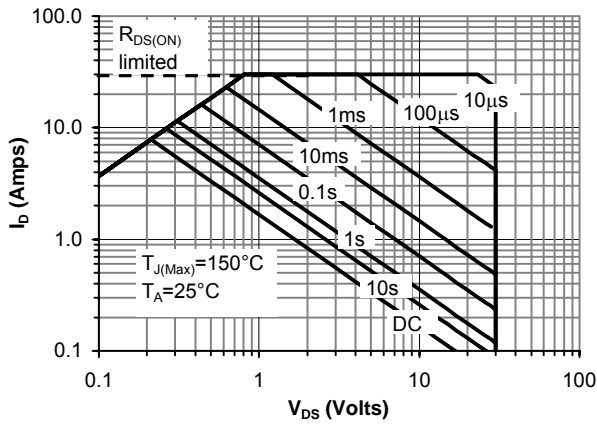


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

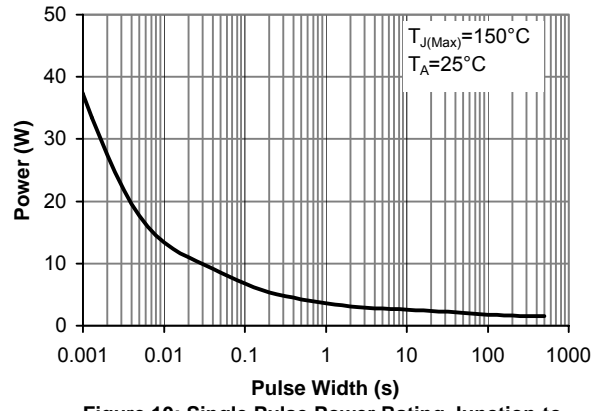


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

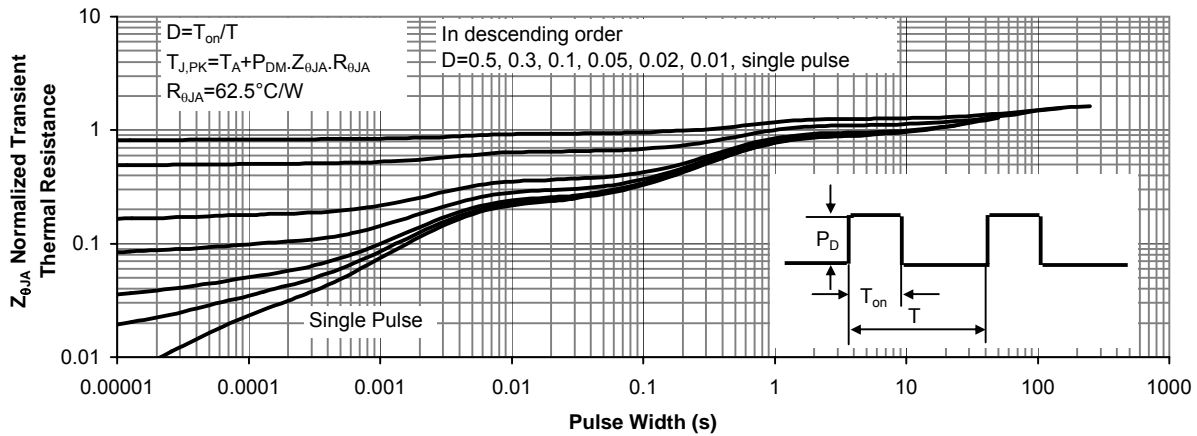


Figure 11: Normalized Maximum Transient Thermal Impedance

P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-24\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			-1 -5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 12\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-0.6	-1	-1.4	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-4.5\text{V}$, $V_{DS}=-5\text{V}$	-10			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}$, $I_D=-3\text{A}$ $T_J=125^\circ\text{C}$		102 154	130 200	$\text{m}\Omega$
		$V_{GS}=-4.5\text{V}$, $I_D=-2\text{A}$		128	180	$\text{m}\Omega$
		$V_{GS}=-2.5\text{V}$, $I_D=-1\text{A}$		187	260	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}$, $I_D=-3\text{A}$	3	4.5		S
V_{SD}	Diode Forward Voltage	$I_S=-1\text{A}$, $V_{GS}=0\text{V}$		-0.85	-1	V
I_S	Maximum Body-Diode Continuous Current				-2	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=-15\text{V}$, $f=1\text{MHz}$		409		pF
C_{oss}	Output Capacitance			55		pF
C_{rSS}	Reverse Transfer Capacitance			42		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		12		Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	$V_{GS}=-4.5\text{V}$, $V_{DS}=-15\text{V}$, $I_D=-3\text{A}$		4.4		nC
Q_{gs}	Gate Source Charge			0.8		nC
Q_{gd}	Gate Drain Charge			1.32		nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=-10\text{V}$, $V_{DS}=-15\text{V}$, $R_L=5\Omega$, $R_{GEN}=3\Omega$		5.3		ns
t_r	Turn-On Rise Time			4.4		ns
$t_{D(off)}$	Turn-Off Delay Time			31.5		ns
t_f	Turn-Off Fall Time			8		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=-3\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		15.8		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-3\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		8		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D: The static characteristics in Figures 1 to 6, 12, 14 are obtained using 80 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

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P-CHANNEL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

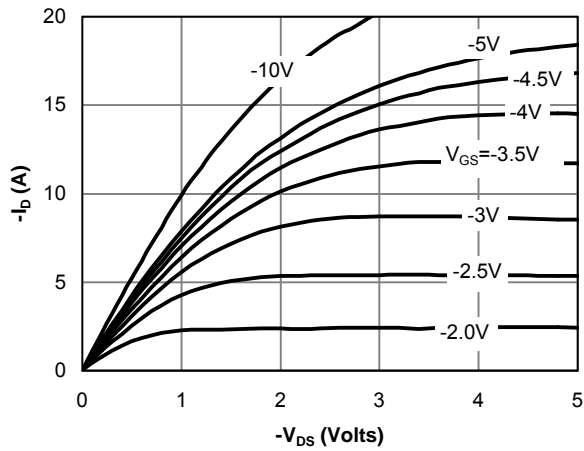


Fig 1: On-Region Characteristics

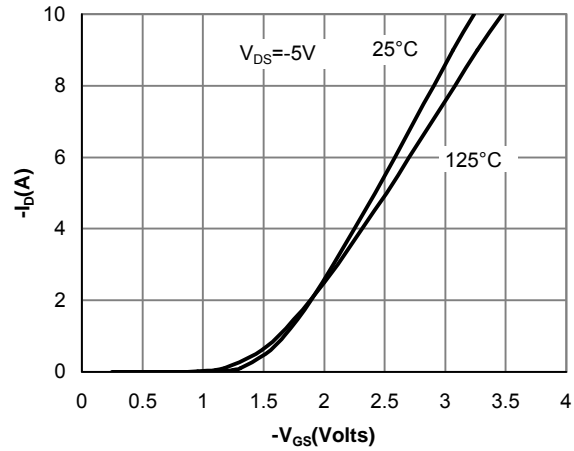


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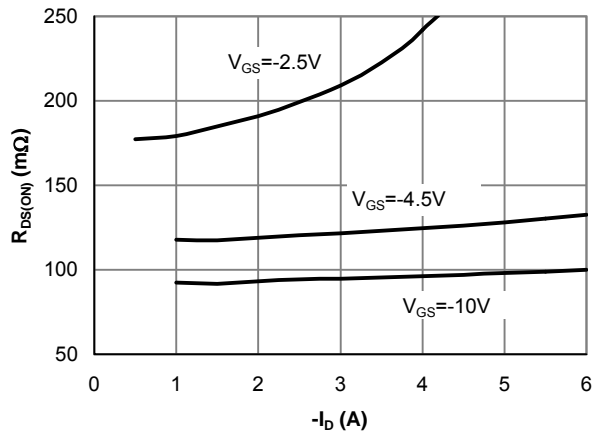


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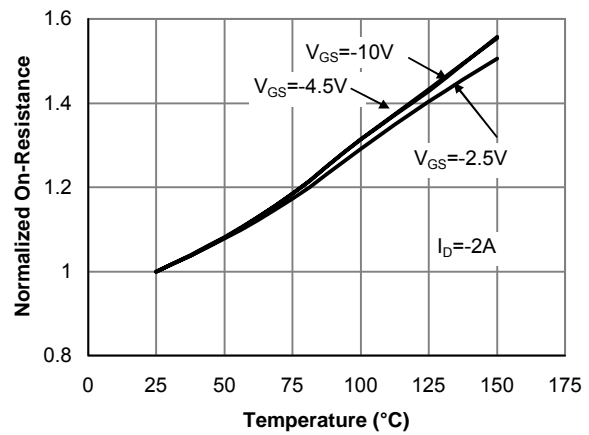


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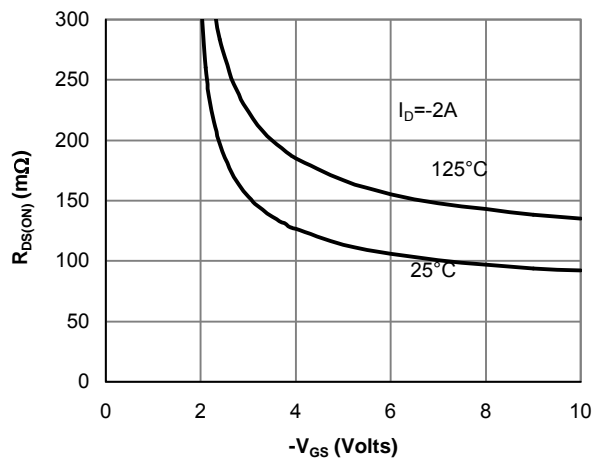


Figure 5: On-Resistance vs. Gate-Source Voltage

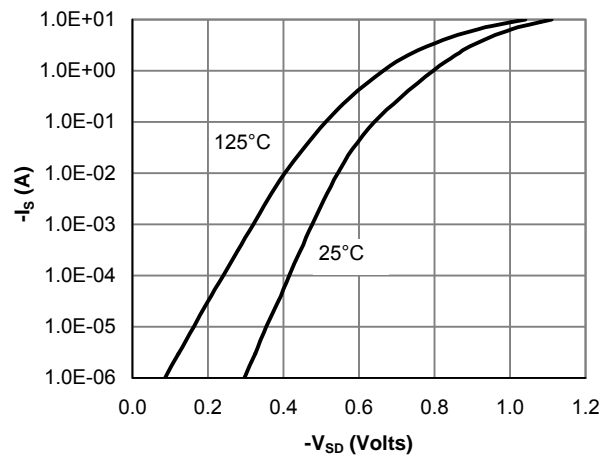


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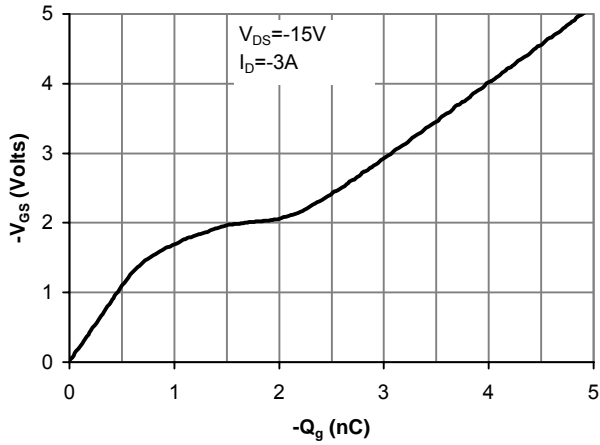


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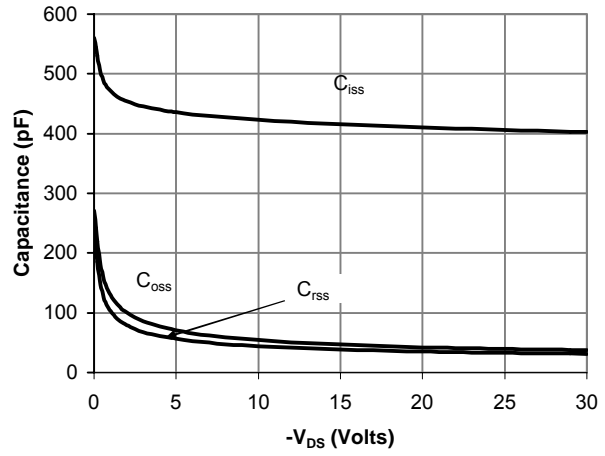


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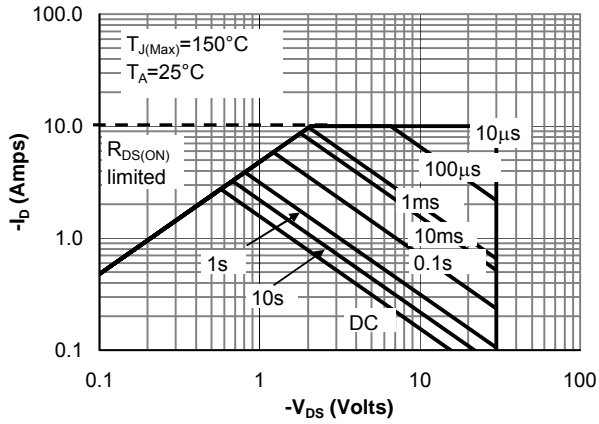


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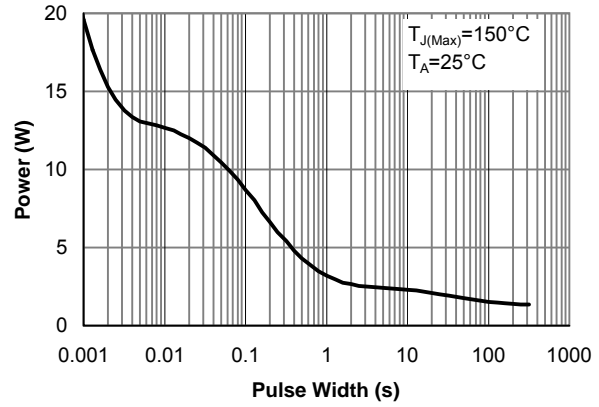


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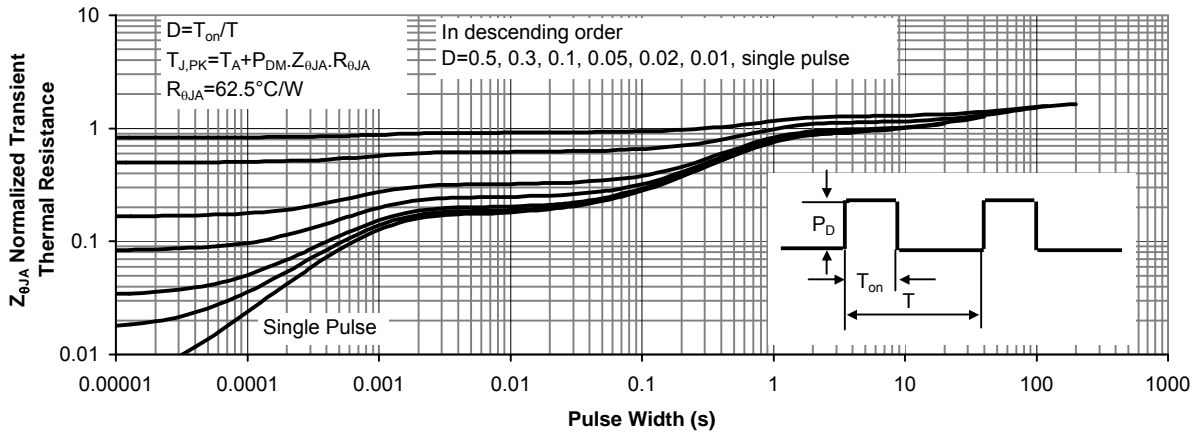


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