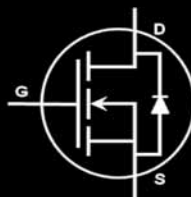


EPC1001 – Enhancement Mode Power Transistor

 $V_{DSS}, 100\text{ V}$
 $R_{DS(ON)}, 7\text{ m}\Omega$
 $I_D, 25\text{ A}$


Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 55 years. GaN's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(ON)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings

| Parameter | Description | Value | Unit |
|-----------|---|------------|------------------|
| V_{DS} | Drain-to-Source Voltage | 100 | V |
| I_D | Continuous ($T_A = 25^\circ\text{C}, \theta_{JA} = 20$) | 25 | A |
| | Pulsed ($25^\circ\text{C}, T_{pulse} = 300\ \mu\text{s}$) | 100 | |
| V_{GS} | Gate-to-Source Voltage | 6 | V |
| | Gate-to-Source Voltage | -5 | |
| T_J | Operating Temperature | -40 to 125 | $^\circ\text{C}$ |
| T_{STG} | Storage Temperature | -40 to 150 | |



EPC Power Transistors are supplied only in passivated die form with solder bumps

Applications

- High Speed DC-DC conversion
- Class D Audio
- Hard Switched and High Frequency Circuits

Benefits

- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra low Q_G
- Ultra small footprint

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|--|------|-----|------------------|
| Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated) | | | | | |
| BV_{DSS} | Drain-to-Source Voltage | $V_{GS} = 0\text{ V}, I_D = 300\ \mu\text{A}$ | 100 | | V |
| I_{DSS} | Drain Source Leakage | $V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$ | 100 | 250 | μA |
| I_{GSS} | Gate-Source Forward Leakage | $V_{GS} = 5\text{ V}$ | 1 | 5 | mA |
| | Gate-Source Reverse Leakage | $V_{GS} = -5\text{ V}$ | 0.2 | 1 | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = 5\text{ mA}$ | 0.7 | 1.4 | V |
| $R_{DS(ON)}$ | Drain-Source On Resistance | $V_{GS} = 5\text{ V}, I_D = 25\text{ A}$ | 5.6 | 7 | $\text{m}\Omega$ |
| Dynamic Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated) | | | | | |
| C_{ISS} | Input Capacitance | $V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$ | 800 | | pF |
| C_{OSS} | Output Capacitance | | 450 | | |
| C_{RSS} | Reverse Transfer Capacitance | | 40 | | |
| Q_G | Total Gate Charge ($V_{GS} = 5\text{ V}$) | $V_{DS} = 50\text{ V}, I_D = 25\text{ A}$ | 10.5 | | nC |
| Q_{GD} | Gate to Drain Charge | | 3.3 | | |
| Q_{GS} | Gate to Source Charge | | 3 | | |
| Q_{OSS} | Output Charge | | 32 | | |
| Q_{RR} | Source-Drain Recovery Charge | | 0 | | |
| Source-Drain Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated) | | | | | |
| V_{SD} | Source-Drain Forward Voltage | $I_S = 0.5\text{ A}, V_{GS} = 0\text{ V}, T = 25^\circ\text{C}$ | 1.8 | | V |
| | | $I_S = 0.5\text{ A}, V_{GS} = 0\text{ V}, T = 125^\circ\text{C}$ | 1.75 | | |

Figure 1: Typical Output Characteristics

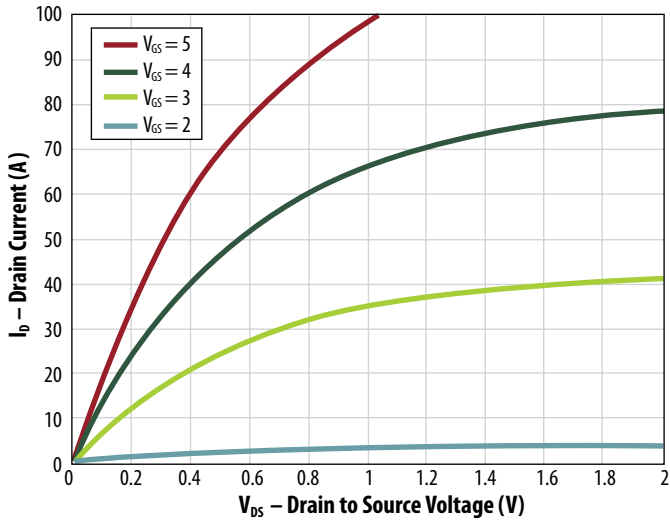


Figure 2: Transfer Characteristics

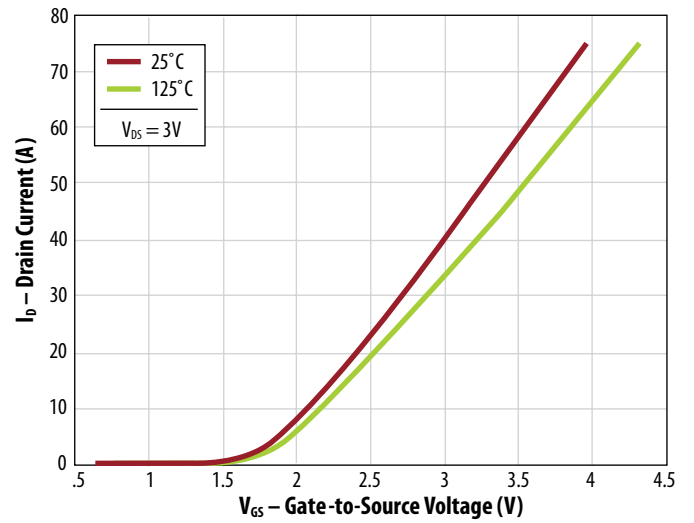


Figure 3: $R_{DS(on)}$ vs V_{GS} for Various Current

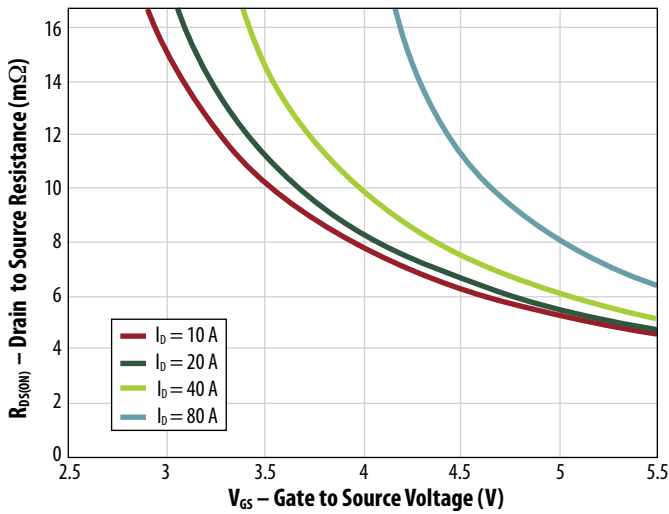


Figure 4: $R_{DS(on)}$ vs V_{GS} for Various Temperature

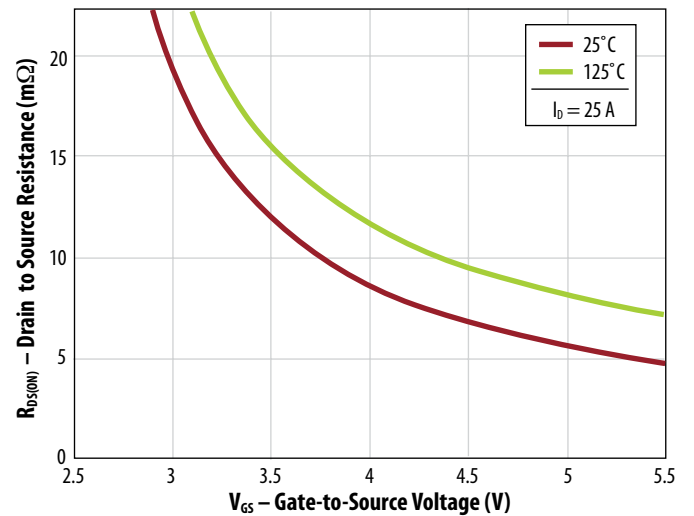


Figure 5: Capacitance

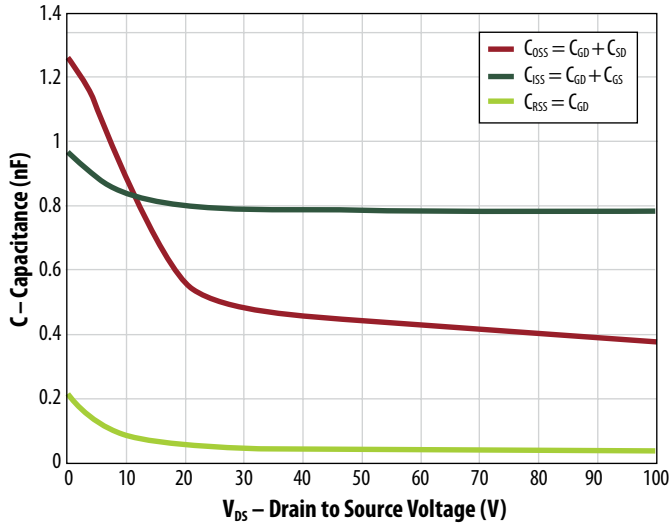


Figure 6: Gate Charge

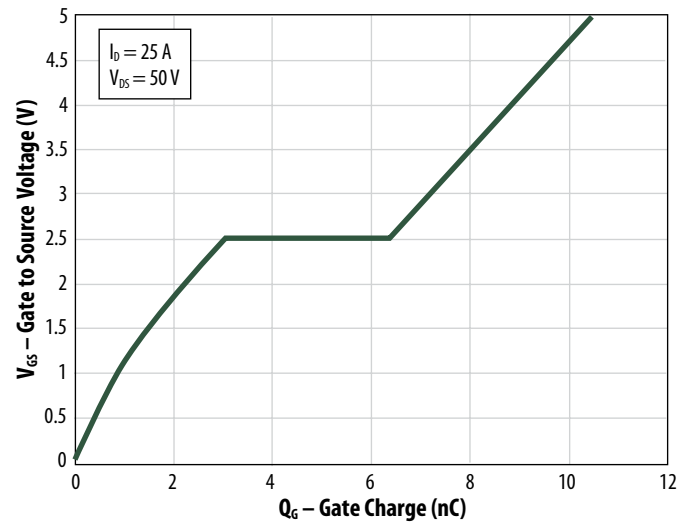


Figure 7: Reverse Drain-Source Characteristics

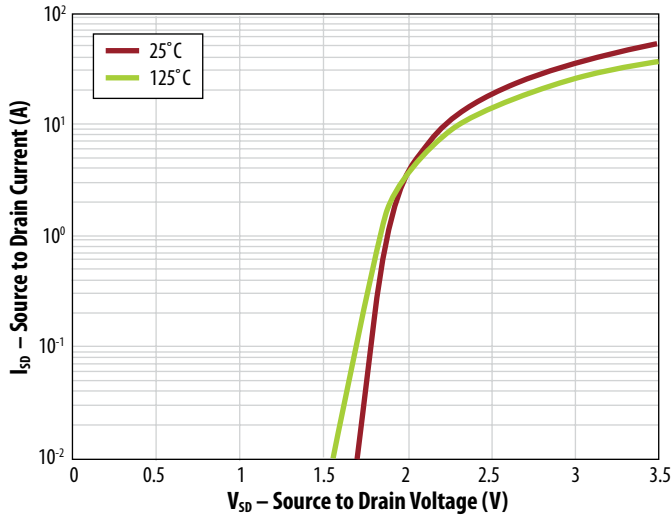


Figure 8: Normalized On Resistance Vs Temperature

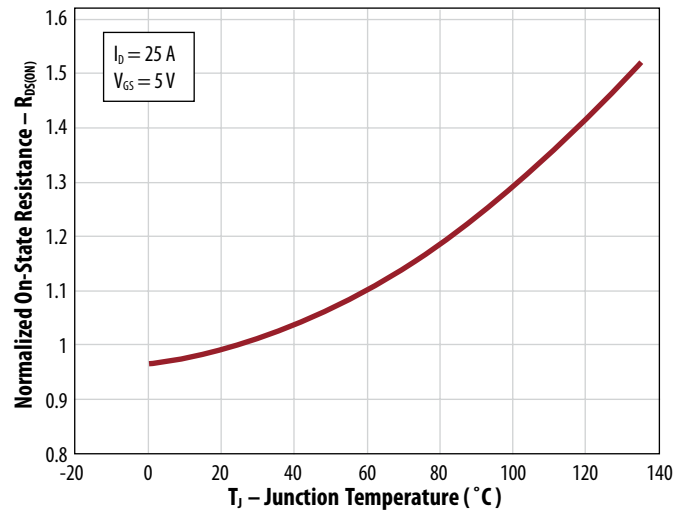


Figure 9: Normalized Threshold Voltage

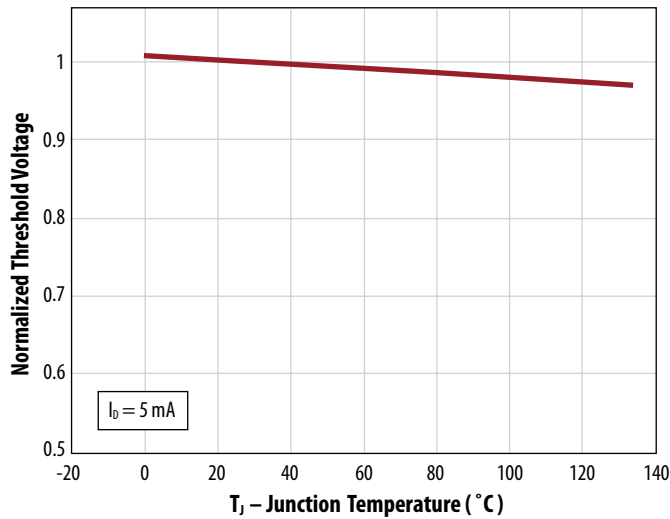
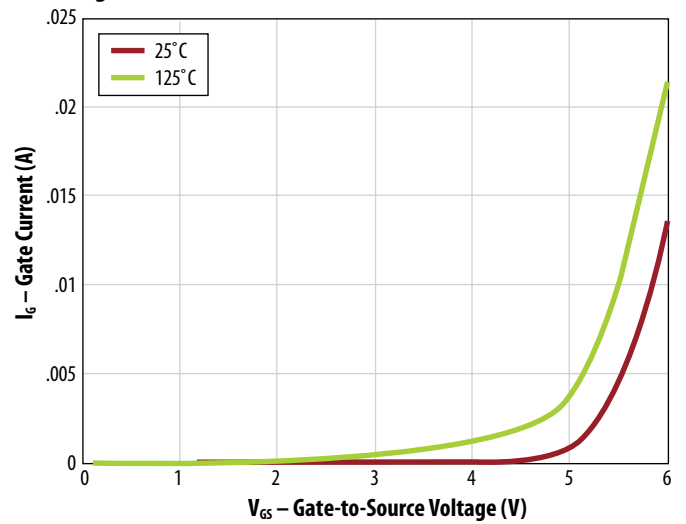
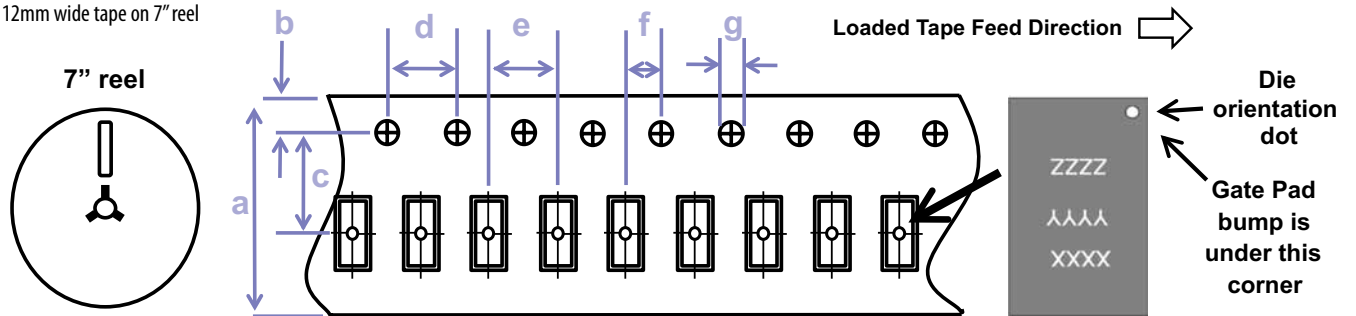


Figure 10: Gate Current



TAPE AND REEL CONFIGURATION

4mm pitch, 12mm wide tape on 7" reel

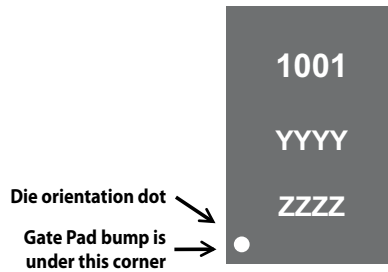


Die is placed into pocket bump side down (face side down)

| Dimension (mm) | EPC1001 | | |
|----------------|---------|------|------|
| | target | min | max |
| a | 12.0 | 11.7 | 12.3 |
| b | 1.75 | 1.65 | 1.85 |
| c (see note) | 5.50 | 5.45 | 5.55 |
| d | 4.00 | 3.90 | 4.10 |
| e | 4.00 | 3.90 | 4.10 |
| f (see note) | 2.00 | 1.95 | 2.05 |
| g | 1.5 | 1.5 | 1.6 |

Note: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole

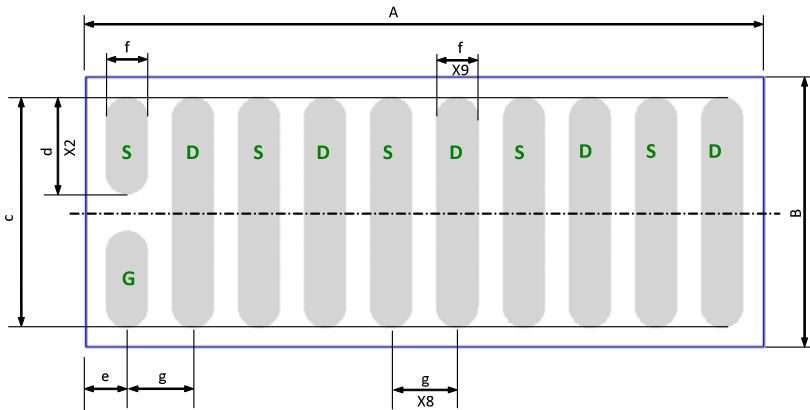
DIE MARKINGS



| Part Number | Laser Markings | | |
|-------------|-----------------------|------------------------------|------------------------------|
| | Part # Marking Line 1 | Lot_Date Code Marking line 2 | Lot_Date Code Marking Line 3 |
| EPC1001 | 1001 | YYYY | ZZZZ |

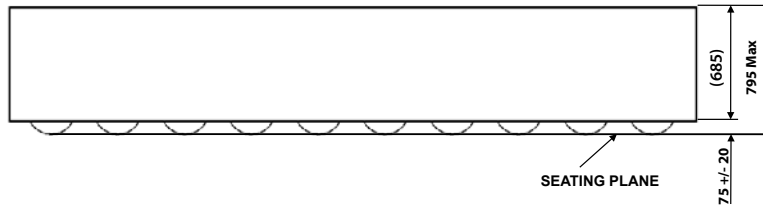
DIE OUTLINE

Bottom View



| DIM | MICROMETERS | | |
|-----|-------------|---------|-------|
| | MIN | Nominal | MAX |
| A | 4075 | 4105 | 4135 |
| B | 1602 | 1632 | 1662 |
| c | 1379 | 1.382 | 1.385 |
| d | 577 | 580 | 583 |
| e | 235 | 250 | 265 |
| f | 248 | 250 | 252 |
| g | 400 | 400 | 400 |

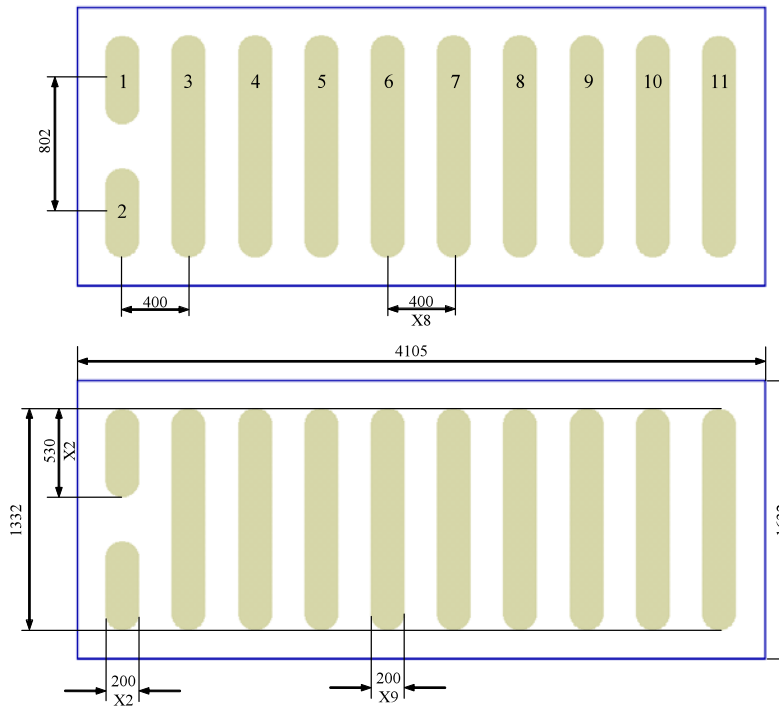
Side View



RECOMMENDED

LAND PATTERN

(measurements in μm)



Pad no. 1 is Gate;
 Pads no. 3, 5, 7, 9, 11 are Drain;
 Pads no. 4, 6, 8, 10 are Source;
 Pad no. 2 is source and is recommended to pin out as a source sense.