

N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
60	0.0055 at $V_{GS} = 10$ V	90 ^d	78.5

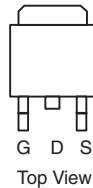
FEATURES

- TrenchFET[®] Power MOSFETS
- 175 °C Junction Temperature
- 100 % R_g and UIS Tested

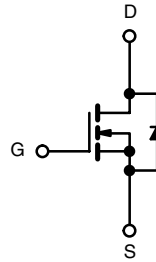

RoHS
COMPLIANT

APPLICATIONS

- Power Supply
 - Secondary Synchronous Rectification
- Industrial

TO-263


Ordering Information: SUM90N06-5m5P-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175$ °C)	I_D	$T_C = 25$ °C	90 ^d
		$T_C = 70$ °C	90 ^d
Pulsed Drain Current	I_{DM}	240	A
Avalanche Current	I_{AS}	50	
Single Avalanche Energy ^a	E_{AS}	125	mJ
Maximum Power Dissipation ^a	P_D	$T_C = 25$ °C	272 ^b
		$T_A = 25$ °C ^c	3.75
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) ^c	R_{thJA}	40	°C/W
Junction-to-Case (Drain)	R_{thJC}	0.55	

Notes:

- Duty cycle ≤ 1 %.
- See SOA curve for voltage derating.
- When Mounted on 1" square PCB (FR-4 material).
- Package limited.

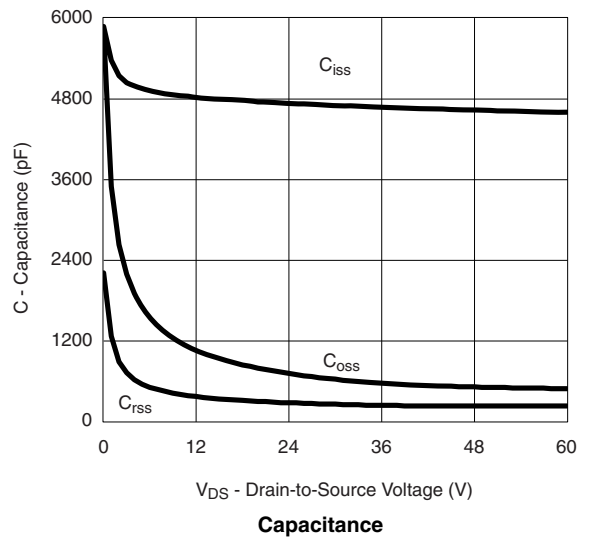
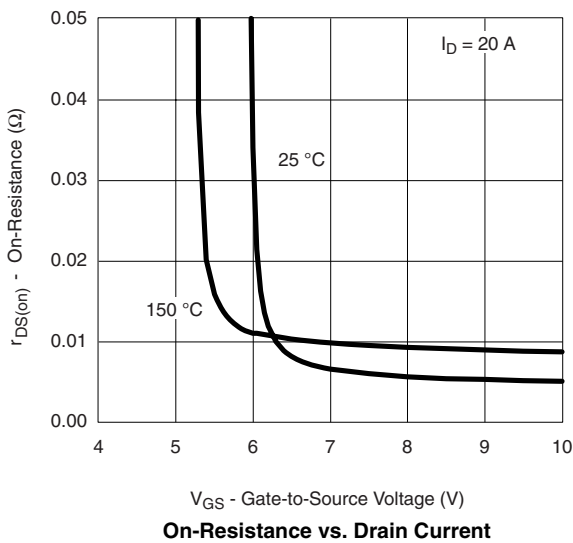
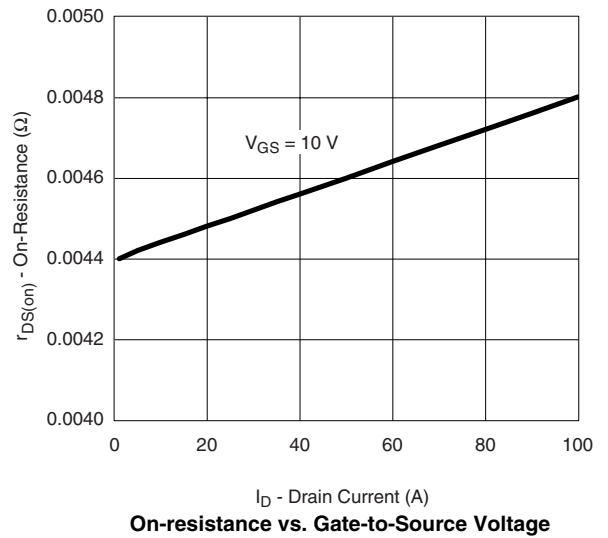
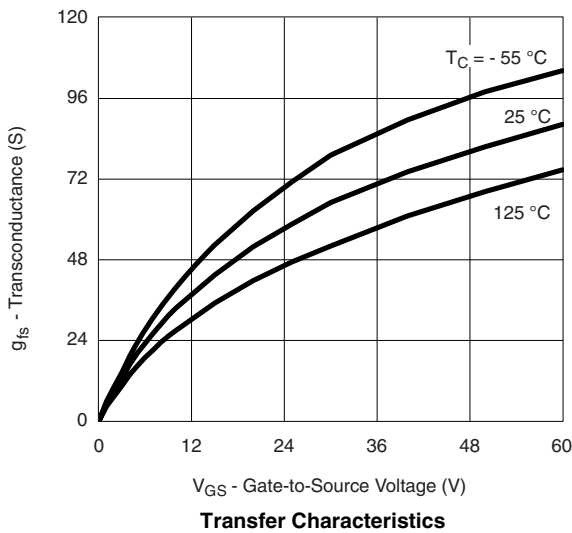
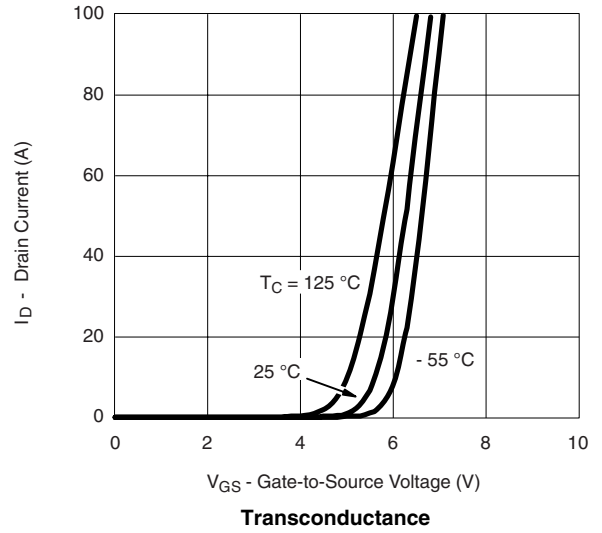
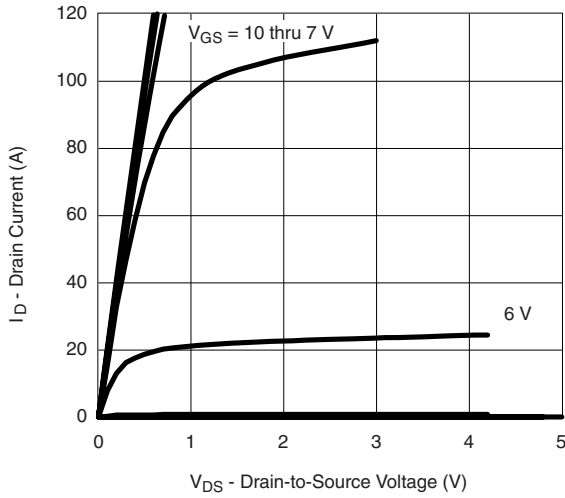
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{DS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.5		4.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			50	
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$			250	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 10\text{ V}, V_{GS} = 10\text{ V}$	70			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.0045	0.0055	Ω
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$		0.0072	0.009	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		58		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 30\text{ V}, f = 1\text{ MHz}$		4700		pF
Output Capacitance	C_{oss}			620		
Reverse Transfer Capacitance	C_{rss}			250		
Total Gate Charge ^c	Q_g	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		78.5	120	nC
Gate-Source Charge ^c	Q_{gs}			28		
Gate-Drain Charge ^c	Q_{gd}			20.6		
Gate Resistance	R_g	$f = 1\text{ MHz}$		1.2	2.4	Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 0.6\text{ }\Omega$ $I_D \cong 50\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		16	30	ns
Rise Time ^c	t_r			10	20	
Turn-Off Delay Time ^c	$t_{d(off)}$			25	40	
Fall Time ^c	t_f			8	15	
Source-Drain Diode Ratings and Characteristics $T_C = 25\text{ }^\circ\text{C}$ ^b						
Continuous Current	I_S				85	A
Pulsed Current	I_{SM}				240	
Forward Voltage ^a	V_{SD}	$I_F = 20\text{ A}, V_{GS} = 0\text{ V}$		0.83	1.5	V
Reverse Recovery Time	t_{rr}	$I_F = 75\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		62	100	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			3.8	5.7	A
Reverse Recovery Charge	Q_{rr}				118	180

Notes:

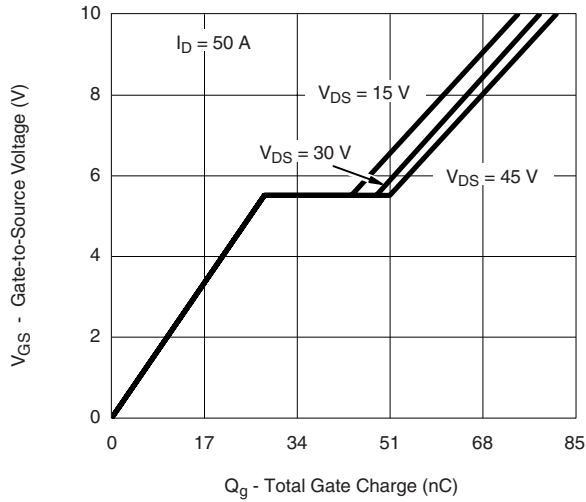
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

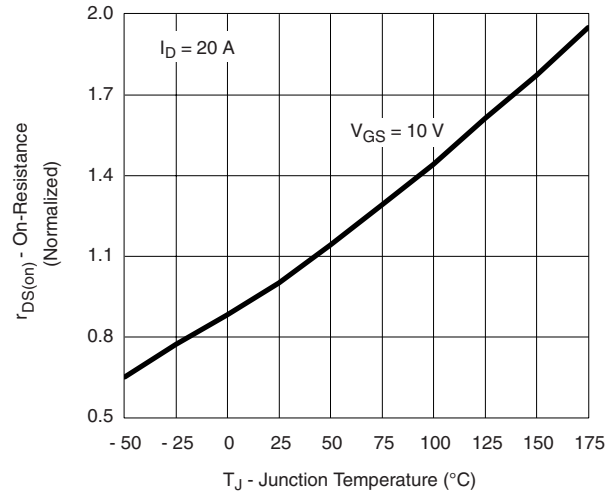
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



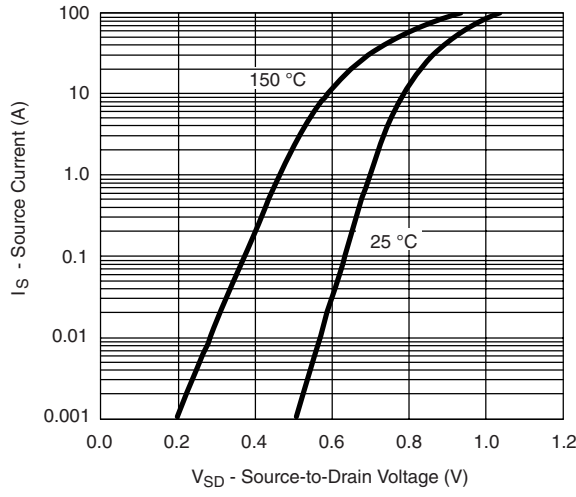
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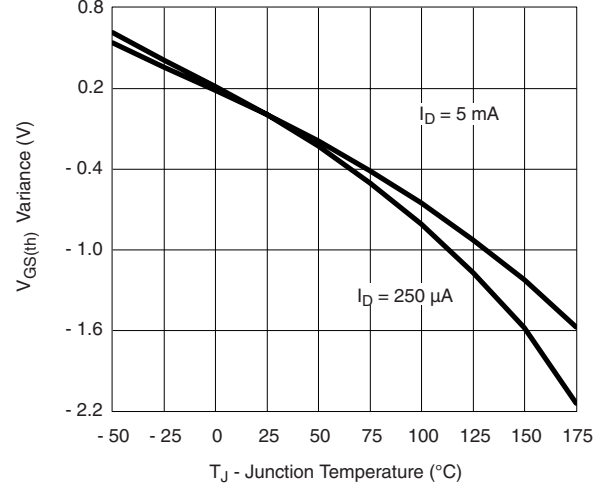
On-Resistance vs. Junction Temperature



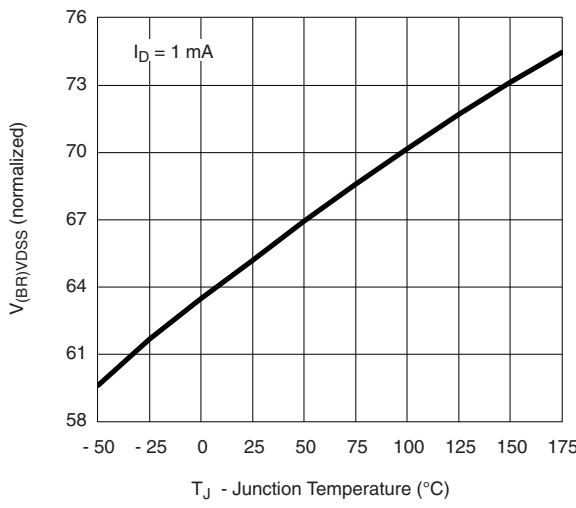
Threshold Voltage



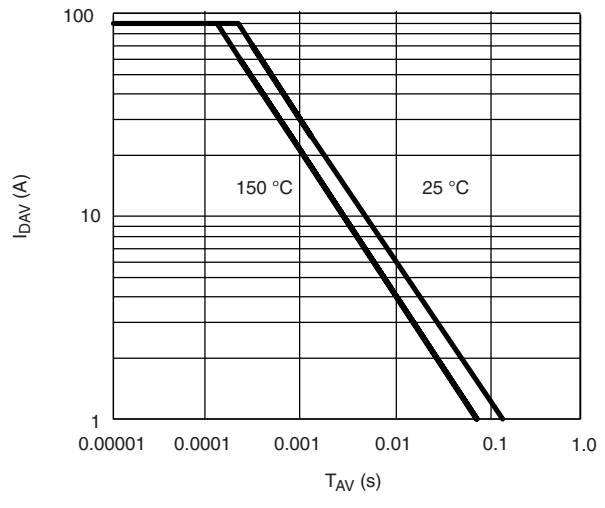
Gate Charge



On-Resistance vs. Junction Temperature

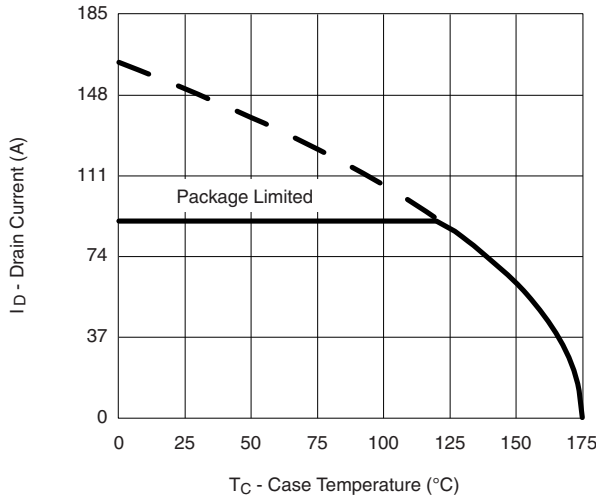


Source-Drain Diode Forward Voltage

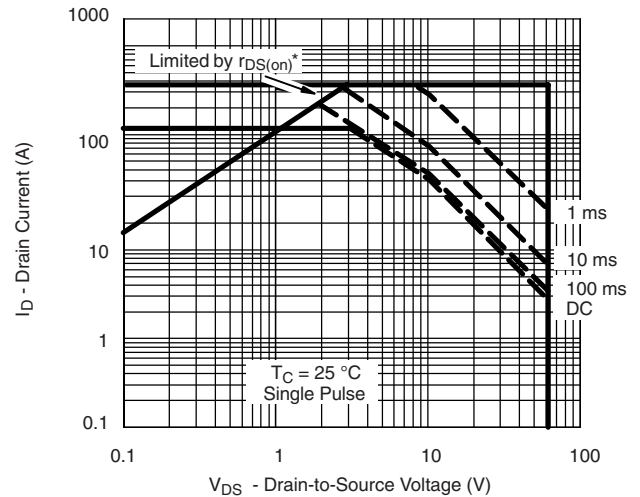


Maximum Drain Current vs. Case Temperature

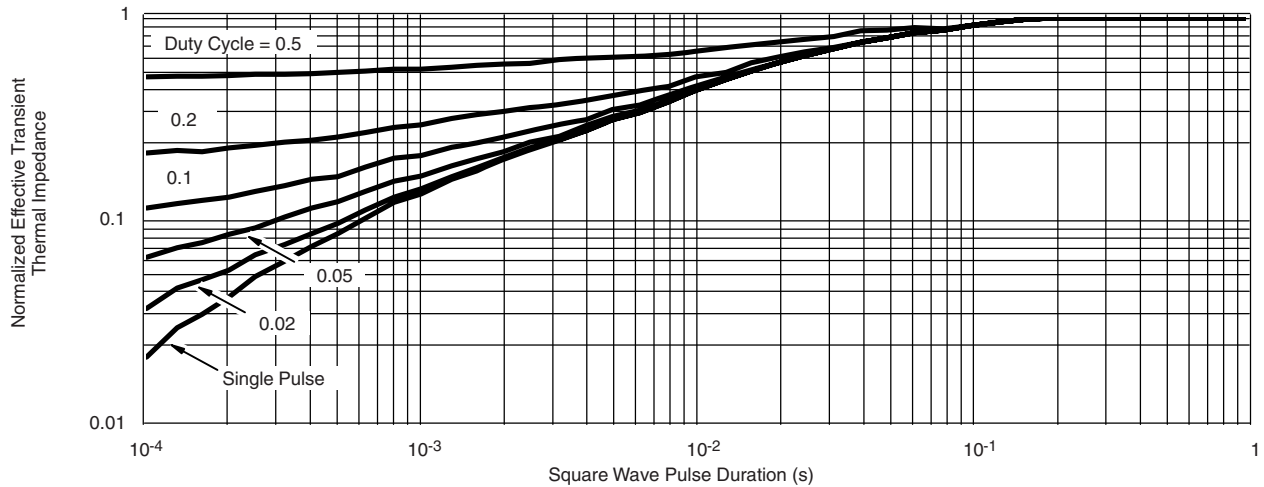
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Single Pulse Avalanche Current Capability vs. Time



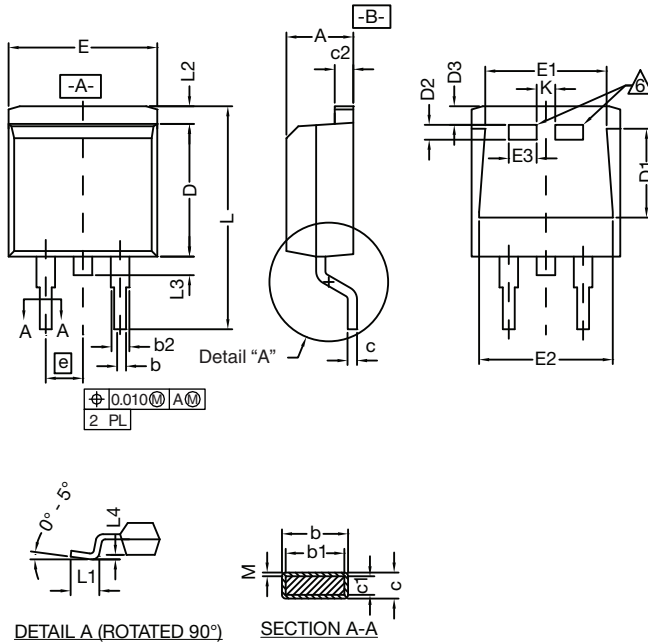
Safe Operating Area
* $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified



Normalized Thermal Transient Impedance, Junction-to-Case

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TO-263 (D²PAK): 3-LEAD



DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
E3	0.072	0.078	1.829	1.981	
[e]	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	
ECN: T10-0738-Rev. J, 03-Jan-11					
DWG: 5843					

Notes

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- *: Thin lead is for SUB, SYB.
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
- This feature is for thick lead.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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