



## P-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY			
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a</sup>	$Q_g$ (Typ.)
- 40	0.040 at $V_{GS} = - 10$ V	- 8	17 nC
	0.050 at $V_{GS} = - 4.5$ V	- 8	

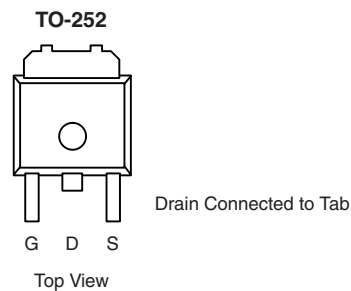
## FEATURES

- TrenchFET<sup>®</sup> Power MOSFET
- 100 % UIS Tested

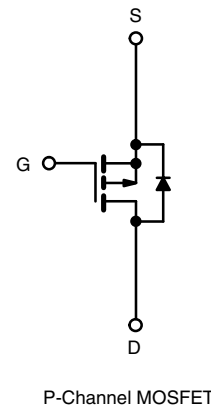
RoHS  
COMPLIANT

## APPLICATIONS

- Backlight Inverter for LCD Display
- Full Bridge DC/DC Converter



Ordering Information:  
SUD50P04-40P-E3 (Lead (Pb)-free)



ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	$V_{DS}$	- 40	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	- 8 <sup>a</sup>	A
		$T_C = 70$ °C	- 8 <sup>a</sup>	
		$T_A = 25$ °C	- 6 <sup>b</sup>	
		$T_A = 70$ °C	- 4.8 <sup>b</sup>	
Pulsed Drain Current	$I_{DM}$	- 30		
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25$ °C	- 8 <sup>a</sup>	
		$T_A = 25$ °C	- 2.0 <sup>b</sup>	
Single Pulse Avalanche Current	$I_{AS}$	15		
Avalanche Energy	$E_{AS}$	11.25	mJ	
Maximum Power Dissipation	$P_D$	$T_C = 25$ °C	24	W
		$T_C = 70$ °C	15.3	
		$T_A = 25$ °C	2.4 <sup>b</sup>	
		$T_A = 70$ °C	1.5 <sup>b</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b</sup>	$R_{thJA}$	43	52	°C/W	
Maximum Junction-to-Case					

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 40			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		- 41		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		4.3			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 1.4		- 2.7	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}$			- 1	$\mu\text{A}$
		$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}, T_J = 70\text{ }^\circ\text{C}$			- 20	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq -5\text{ V}, V_{GS} = -10\text{ V}$	- 10			A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -5\text{ A}$		0.030	0.040	$\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -4\text{ A}$		0.036	0.050	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -15\text{ V}, I_D = -5\text{ A}$		20		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1555		pF
Output Capacitance	$C_{oss}$		176			
Reverse Transfer Capacitance	$C_{rss}$		142			
Total Gate Charge	$Q_g$	$V_{DS} = -20\text{ V}, V_{GS} = -10\text{ V}, I_D = -5\text{ A}$		38.5	60	nC
				17	27	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -20\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -5\text{ A}$		4.2		nC
Gate-Drain Charge	$Q_{gd}$		7.0			
Gate Resistance	$R_g$		$f = 1\text{ MHz}$		3	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -20\text{ V}, R_L = 4\text{ }\Omega$ $I_D \cong -5\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		47	80	ns
Rise Time	$t_r$		60	110		
Turn-Off Delay Time	$t_{d(off)}$		35	60		
Fall Time	$t_f$		13	25		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -20\text{ V}, R_L = 4\text{ }\Omega$ $I_D \cong -5\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		10	20	ns
Rise Time	$t_r$		14	25		
Turn-Off Delay Time	$t_{d(off)}$		36	60		
Fall Time	$t_f$		10	20		
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			- 8	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				- 30	
Body Diode Voltage	$V_{SD}$	$I_S = -2\text{ A}$		- 0.76	- 1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		22	40	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		22	40	nC	
Reverse Recovery Fall Time	$t_a$		15		ns	
Reverse Recovery Rise Time	$t_b$		7			

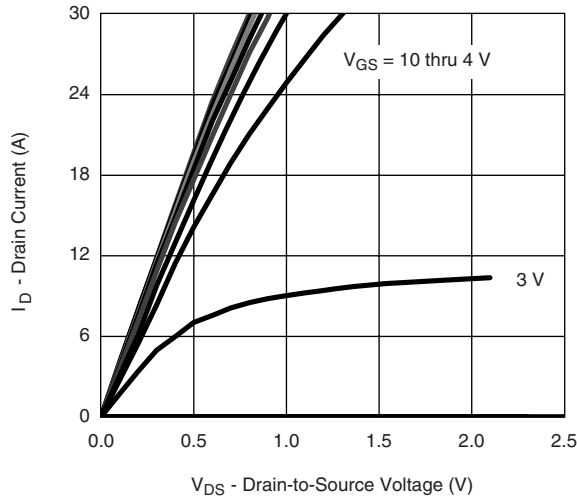
Notes:

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.

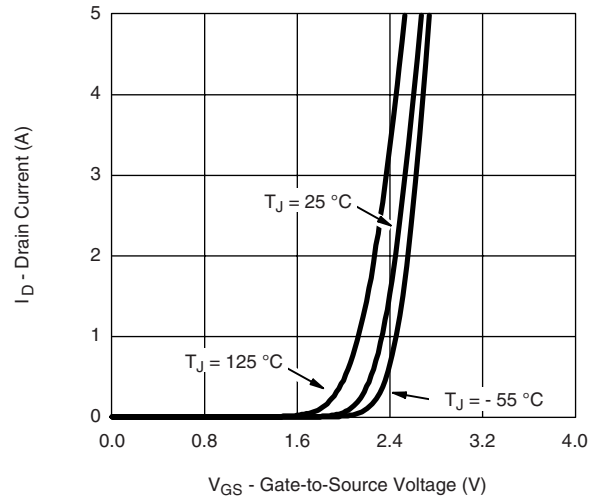
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



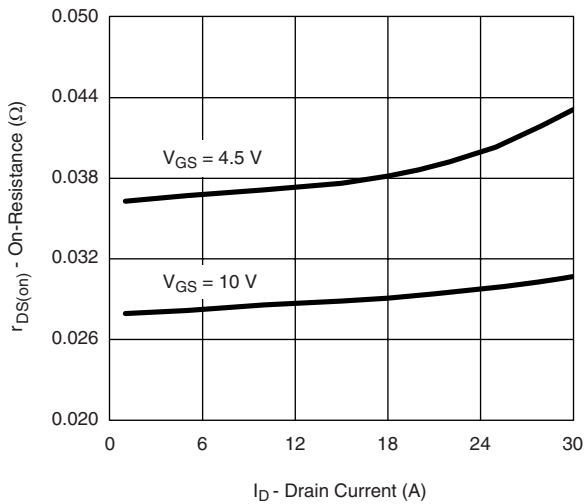
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



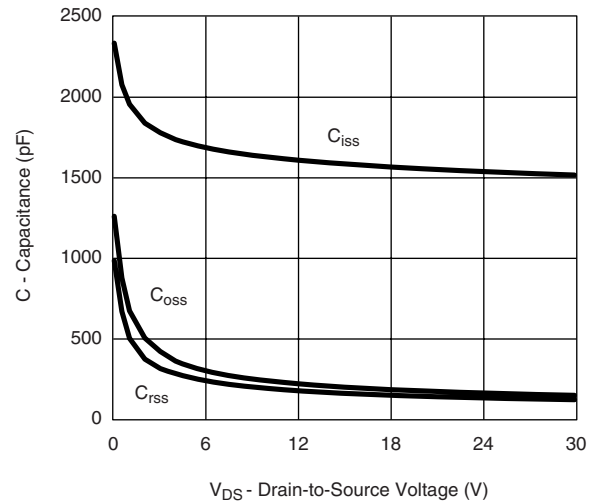
**Output Characteristics**



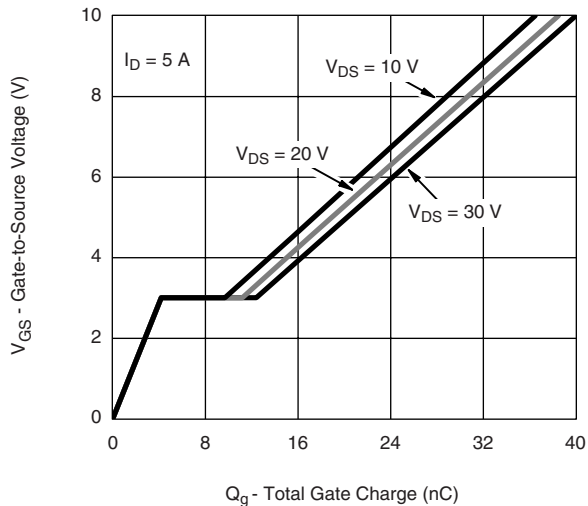
**Transfer Characteristics**



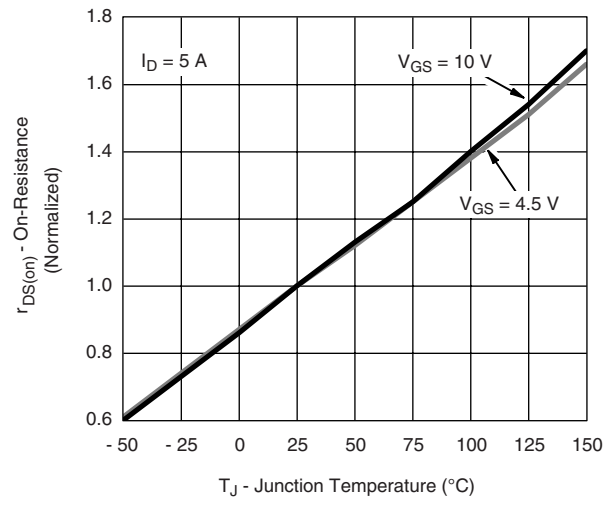
**On-Resistance vs. Drain Current**



**Capacitance**



**Gate Charge**



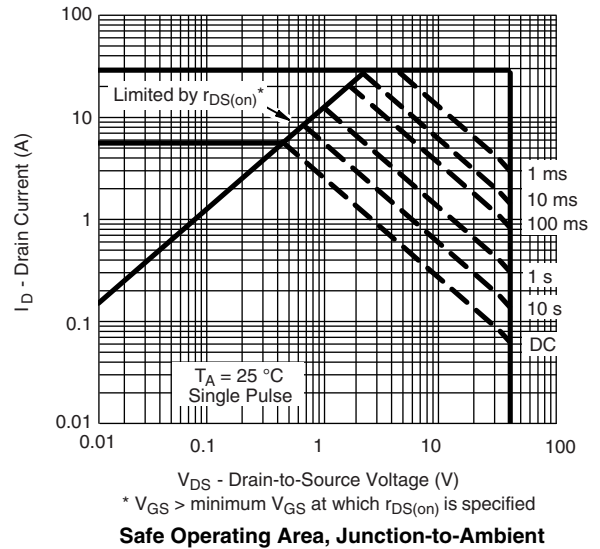
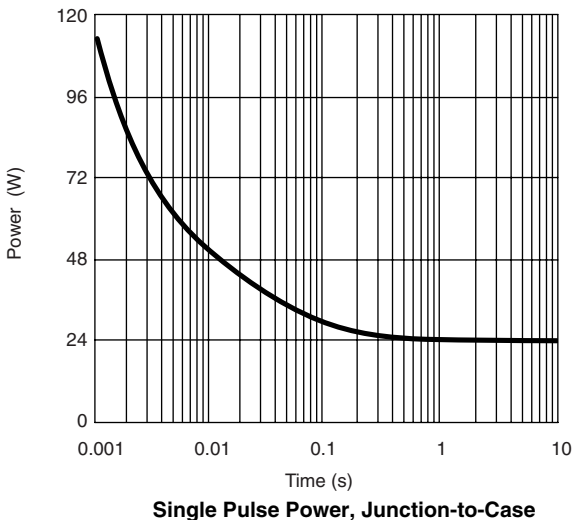
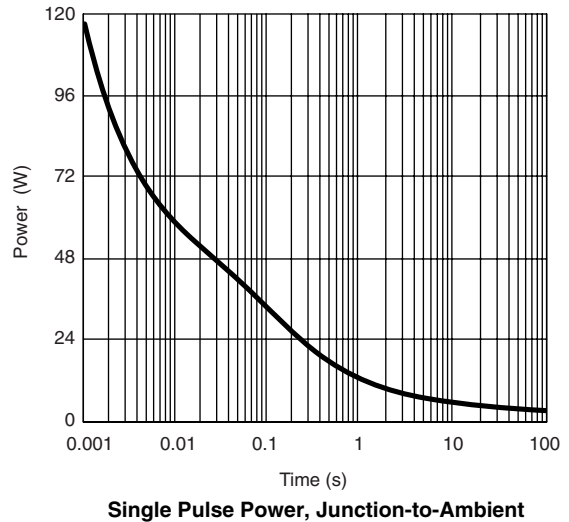
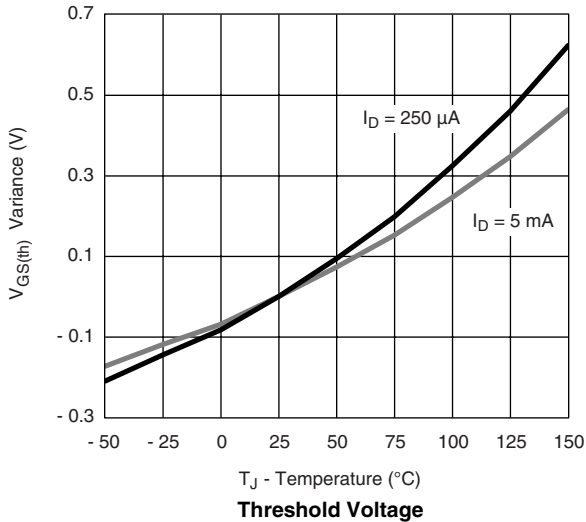
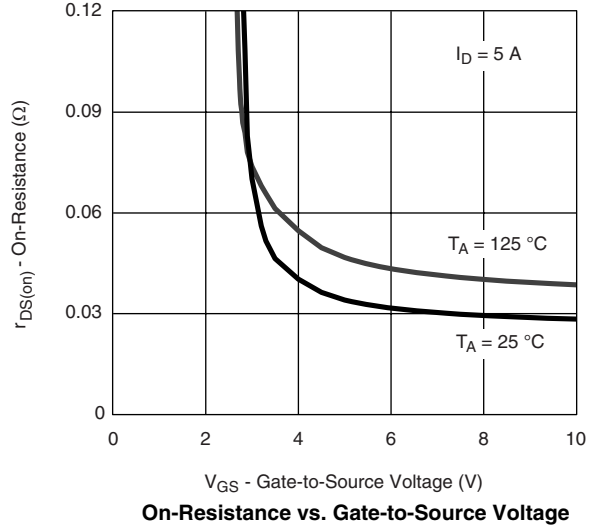
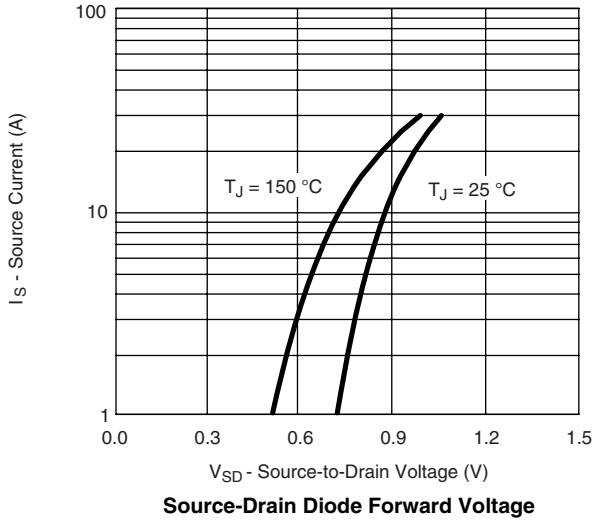
**On-Resistance vs. Junction Temperature**

# SUD50P04-40P



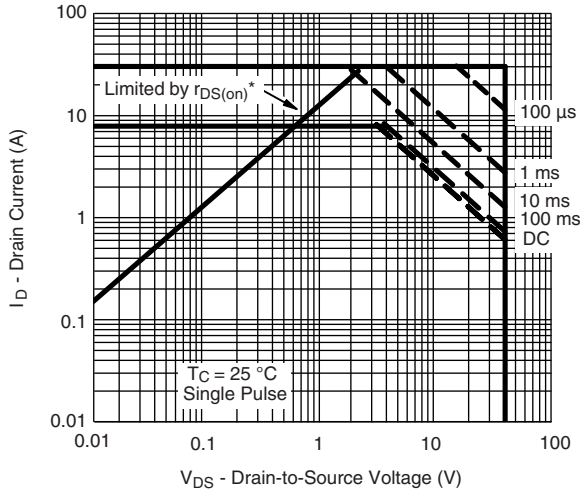
Vishay Siliconix

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

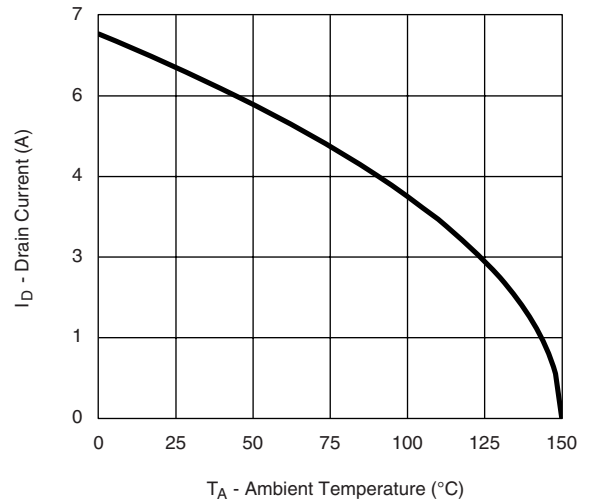




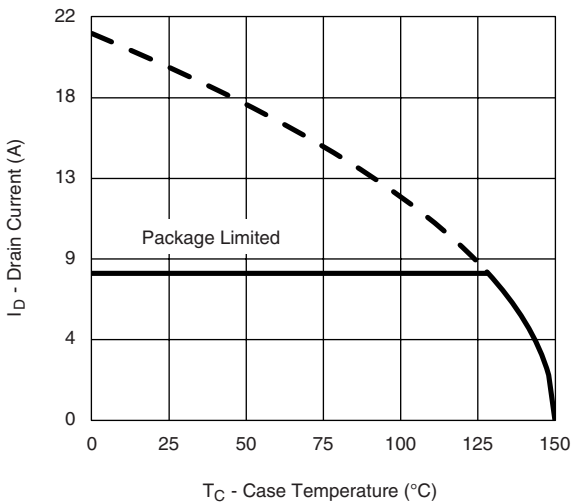
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



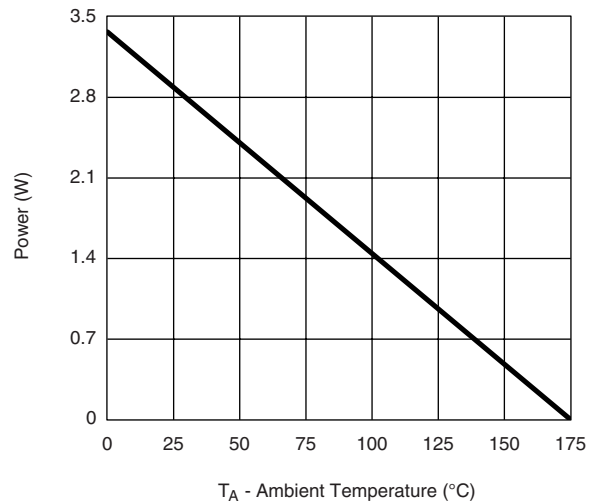
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $r_{DS(on)}$  is specified  
**Safe Operating Area, Junction-to-Case**



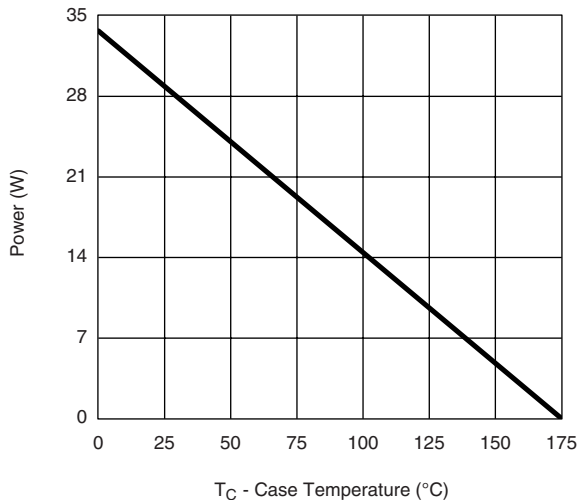
**Current Derating\*, Junction-to-Ambient**



**Current Derating\*, Junction-to-Case**



**Power Derating\*, Junction-to-Ambient**



**Power Derating\*, Junction-to-Case**

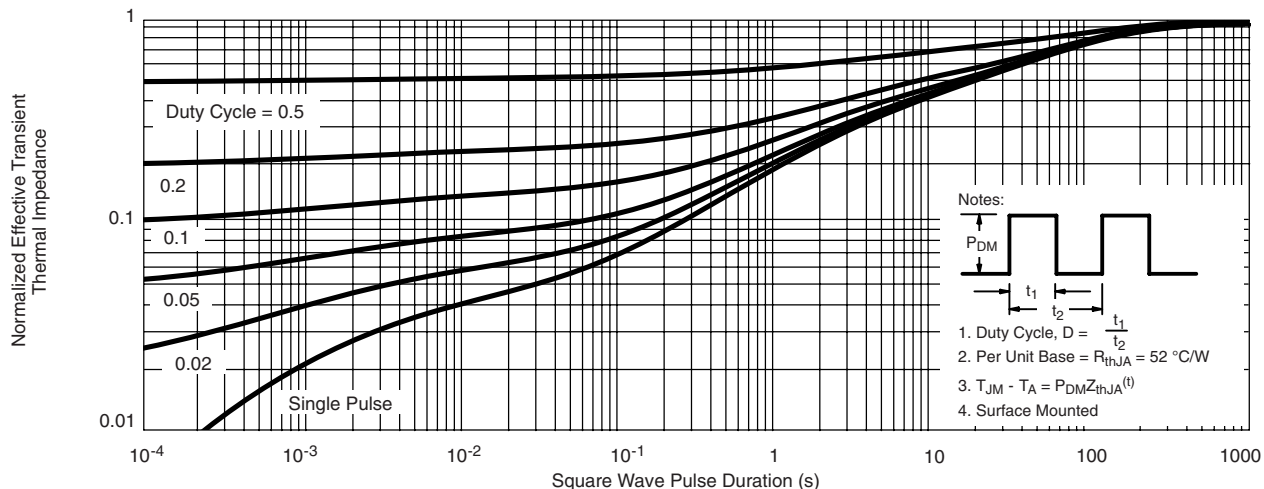
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 175\text{ }^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

# SUD50P04-40P

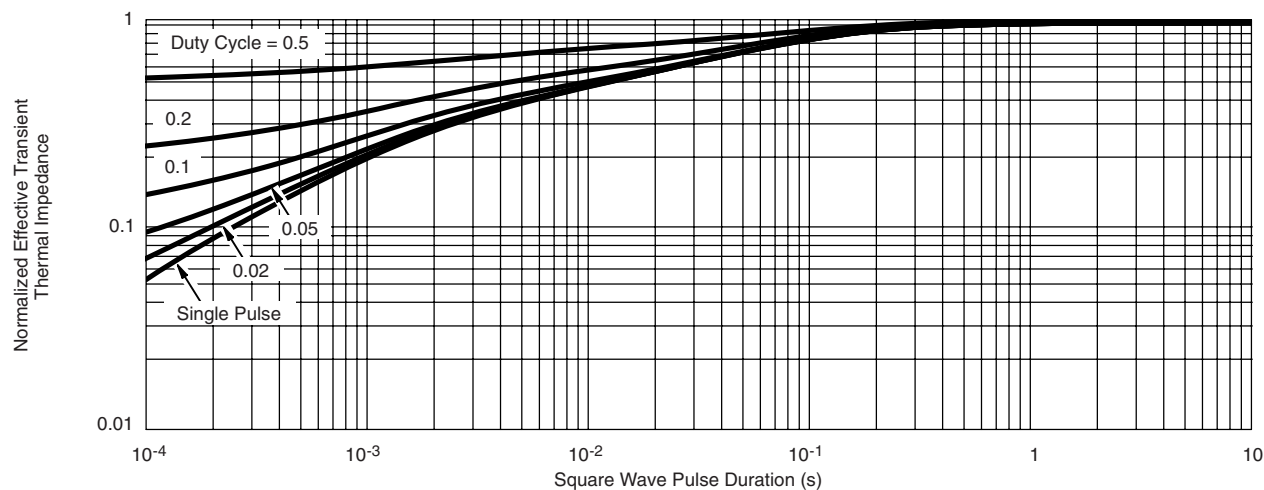
Vishay Siliconix



## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



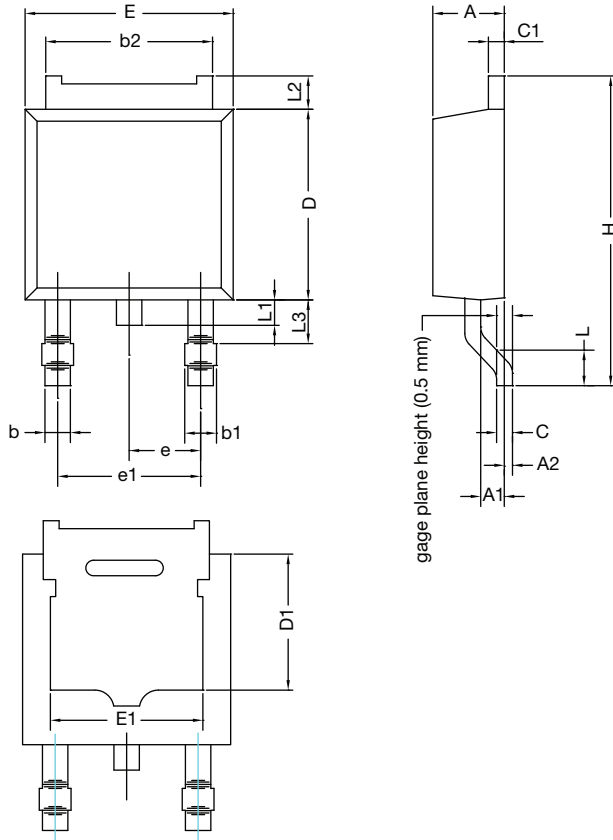
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?69731>.

## TO-252AA CASE OUTLINE



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.21	2.38	0.087	0.094
A1	0.89	1.14	0.035	0.045
A2	0.030	0.127	0.001	0.005
b	0.71	0.88	0.028	0.035
b1	0.76	1.14	0.030	0.045
b2	5.23	5.44	0.206	0.214
C	0.46	0.58	0.018	0.023
C1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
D1	4.10	4.45	0.161	0.175
E	6.48	6.73	0.255	0.265
E1	4.49	5.50	0.177	0.217
e	2.28 BSC		0.090 BSC	
e1	4.57 BSC		0.180 BSC	
H	9.65	10.41	0.380	0.410
L	1.40	1.78	0.055	0.070
L1	0.64	1.02	0.025	0.040
L2	0.89	1.27	0.035	0.050
L3	1.15	1.52	0.040	0.060
ECN: T11-0110-Rev. L, 18-Apr-11 DWG: 5347				

### Note

- Dimension L3 is for reference only.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)





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