

N-Channel 20-V (D-S) MOSFET with Schottky Diode

MOSFET PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
20	0.039 at V _{GS} = 4.5 V	6	6 nC
	0.045 at V _{GS} = 2.5 V	6	
	0.055 at V _{GS} = 1.8 V	6	

SCHOTTKY PRODUCT SUMMARY		
V _{KA} (V)	V _F (V) Diode Forward Voltage	I _F (A) ^a
20	0.375 at 1 A	1

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- LITTLE FOOT[®] Plus Power MOSFET
- New Thermally Enhanced PowerPAK[®] ChipFET[®] Package
 - Small Footprint Area
 - Low On-Resistance
 - Thin 0.8 mm Profile
- Compliant to RoHS Directive 2002/95/EC

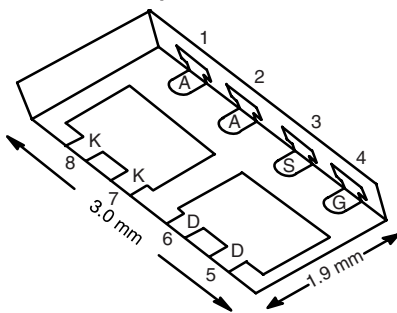


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

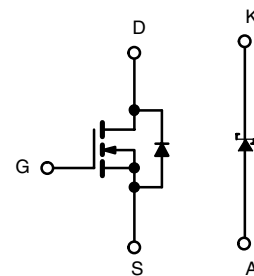
- Load Switch for Portable Applications
- Ideal for Boost Circuits

PowerPAK ChipFET Dual



Bottom View

Marking Code



N-Channel MOSFET

Ordering Information: Si5858DU-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage (MOSFET)	V _{DS}	20	V	
Reverse Voltage (Schottky)	V _{KA}	20		
Gate-Source Voltage (MOSFET)	V _{GS}	± 8		
Continuous Drain Current (T _J = 150 °C) (MOSFET)	I _D	T _C = 25 °C	6 ^a	A
		T _C = 70 °C	6 ^a	
		T _A = 25 °C	7.2 ^{b, c}	
		T _A = 70 °C	5.8 ^{b, c}	
Pulsed Drain Current (MOSFET)	I _{DM}	20	A	
Continuous Source Current (MOSFET Diode Conduction)	I _S	T _C = 25 °C		6.9
		T _A = 25 °C	1.9 ^{b, c}	
Average Forward Current (Schottky)	I _F	1 ^b	A	
Pulsed Forward Current (Schottky)	I _{FM}	7		
Maximum Power Dissipation (MOSFET)	P _D	T _C = 25 °C	8.3	W
		T _C = 70 °C	5.3	
		T _A = 25 °C	2.3 ^{b, c}	
		T _A = 70 °C	1.5 ^{b, c}	
Maximum Power Dissipation (Schottky)	P _D	T _C = 25 °C	7.8	W
		T _C = 70 °C	5	
		T _A = 25 °C	2.1 ^{b, c}	
		T _A = 70 °C	1.3 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET) ^{b, f}	$t \leq 5$ s	R_{thJA}	45	55	°C/W
Maximum Junction-to-Case (Drain) (MOSFET)		R_{thJC}	12	15	
Maximum Junction-to-Ambient (Schottky)	$t \leq 5$ s	R_{thJA}	49	61	
Maximum Junction-to-Case (Drain) (Schottky)		R_{thJC}	13	16	

Notes:

- Package limited.
- Surface Mounted on FR4 board.
- $t = 5$ s.
- See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions for MOSFETS is 105 °C/W.
- Maximum under Steady State conditions for Schottky is 110 °C/W.

SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = 250$ μ A	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS/TJ}$	$I_D = 250$ μ A		17.4		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)/TJ}$			- 2.6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ μ A	0.4		1.0	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 8$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20$ V, $V_{GS} = 0$ V			- 1	μ A
		$V_{DS} = 20$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			- 10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq 5$ V, $V_{GS} = 4.5$ V	- 20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5$ V, $I_D = 4.4$ A		0.032	0.039	Ω
		$V_{GS} = 2.5$ V, $I_D = 4.1$ A		0.037	0.045	
		$V_{GS} = 1.8$ V, $I_D = 1.8$ A		0.0455	0.055	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10$ V, $I_D = 4.4$ A		22		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 10$ V, $V_{GS} = 0$ V, $f = 1$ MHz		520		pF
Output Capacitance	C_{oss}			100		
Reverse Transfer Capacitance	C_{rss}			60		
Total Gate Charge	Q_g	$V_{DS} = 10$ V, $V_{GS} = 8$ V, $I_D = 4.4$ A		10.5	16	nC
		$V_{DS} = 10$ V, $V_{GS} = 4.5$ V, $I_D = 4.4$ A		6	9	
					0.91	
Gate-Source Charge	Q_{gs}			0.7		
Gate-Drain Charge	Q_{gd}					
Gate Resistance	R_g	$f = 1$ MHz		1.9		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10$ V, $R_L = 2.8$ Ω $I_D \cong 3.6$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ Ω		20	30	ns
Rise Time	t_r			65	100	
Turn-Off Delay Time	$t_{d(off)}$			40	60	
Fall Time	t_f			10	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10$ V, $R_L = 2.8$ Ω $I_D \cong 3.6$ A, $V_{GEN} = 8$ V, $R_g = 1$ Ω		5	10	
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			26	40	
Fall Time	t_f			8	15	



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			14.8	A
Pulse Diode Forward Current	I_{SM}				20	
Body Diode Voltage	V_{SD}	$I_S = 1.2\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -2\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		45	70	ns
Body Diode Reverse Recovery Charge	Q_{rr}			21	32	nC
Reverse Recovery Fall Time	t_a			29		ns
Reverse Recovery Rise Time	t_b			16		

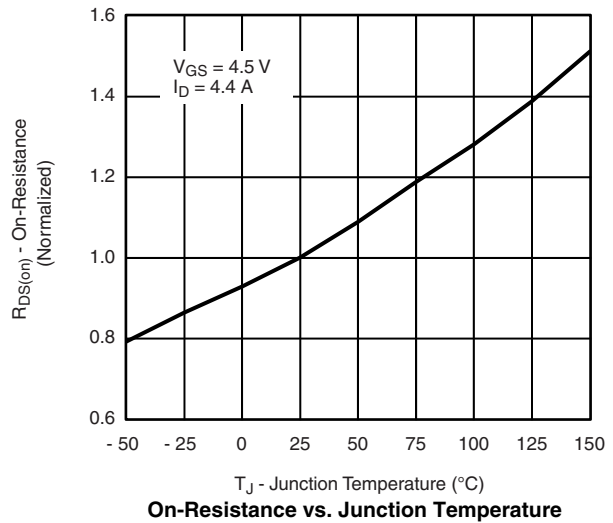
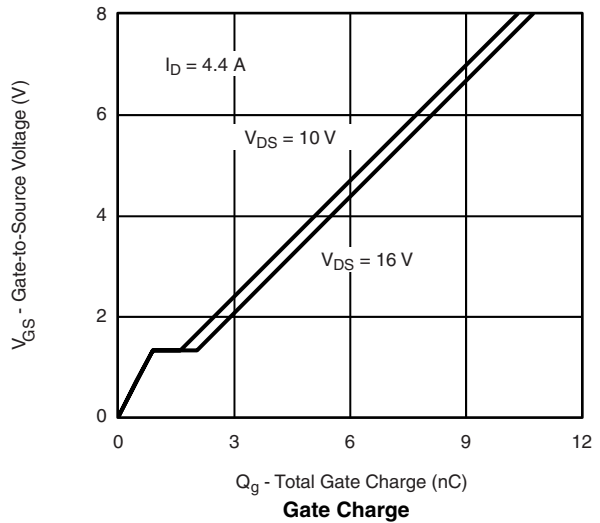
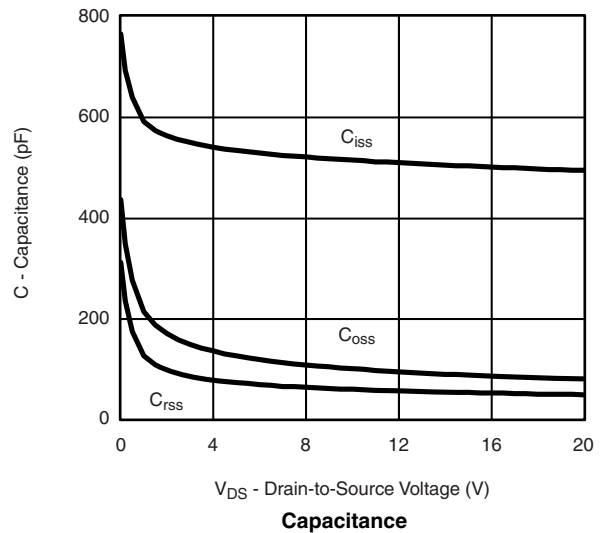
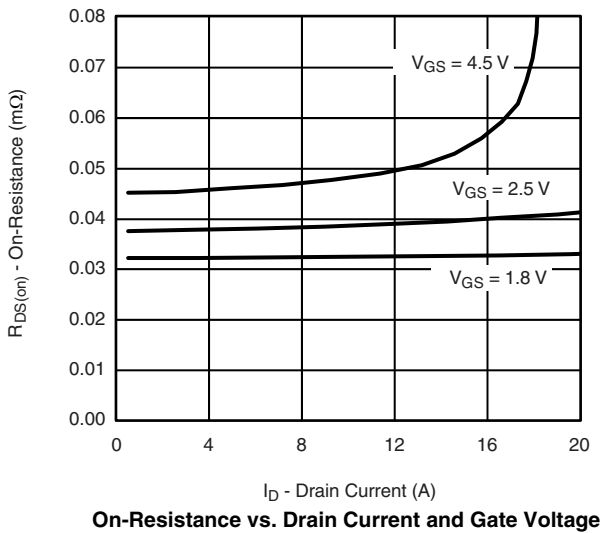
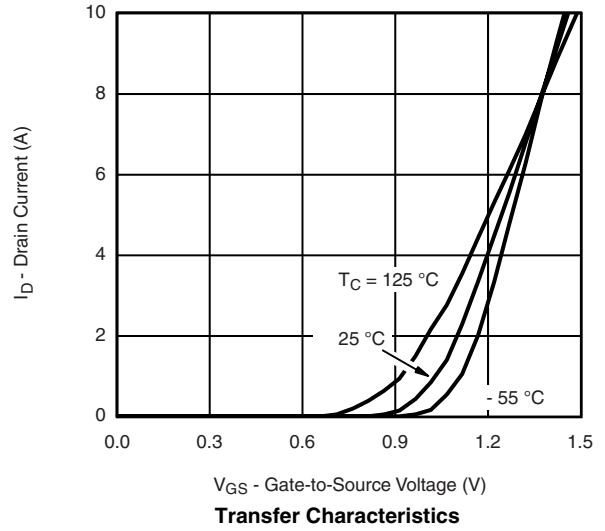
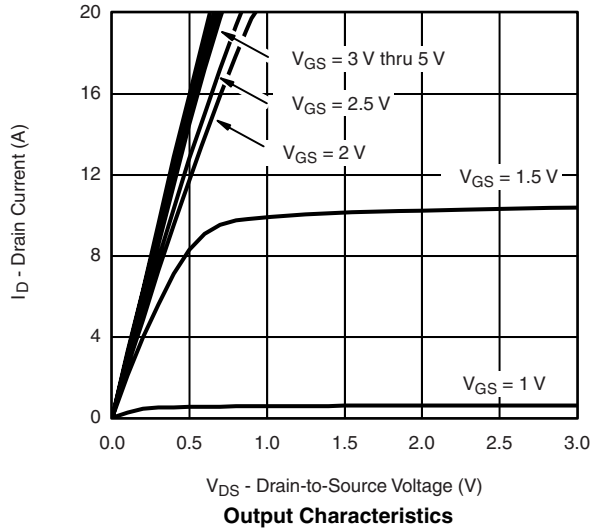
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

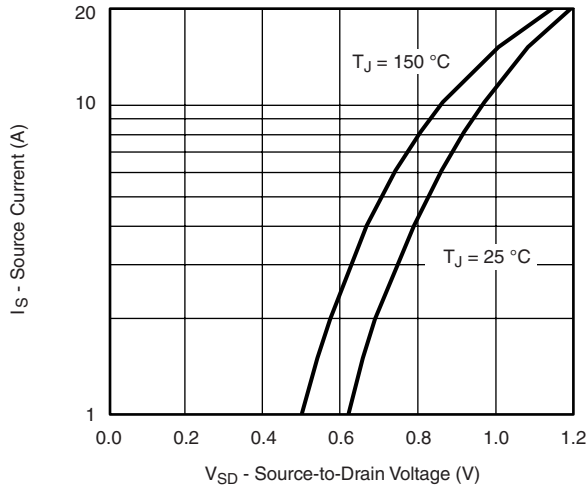
SCHOTTKY SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Forward Voltage Drop	V_F	$I_F = 1\text{ A}$		0.34	0.375	V
		$I_F = 1\text{ A}, T_J = 125\text{ }^\circ\text{C}$		0.255	0.290	
Maximum Reverse Leakage Current	I_{rm}	$V_R = 20\text{ V}$		0.05	0.500	mA
		$V_R = 20\text{ V}, T_J = 85\text{ }^\circ\text{C}$		2	20	
		$V_R = 20\text{ V}, T_J = 125\text{ }^\circ\text{C}$		10	100	
Junction Capacitance	C_T	$V_R = 10\text{ V}$		90		pF

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

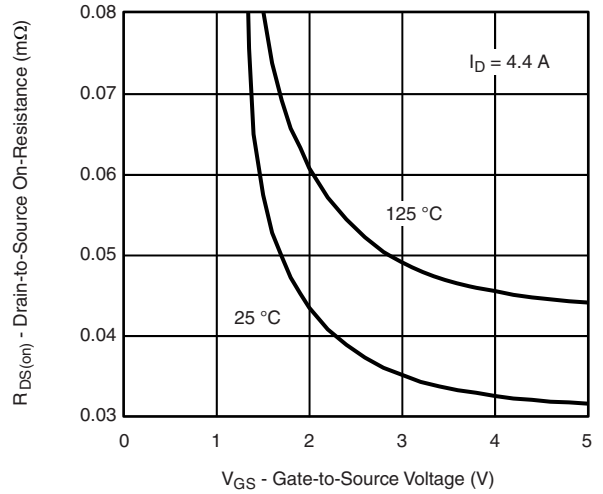
MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



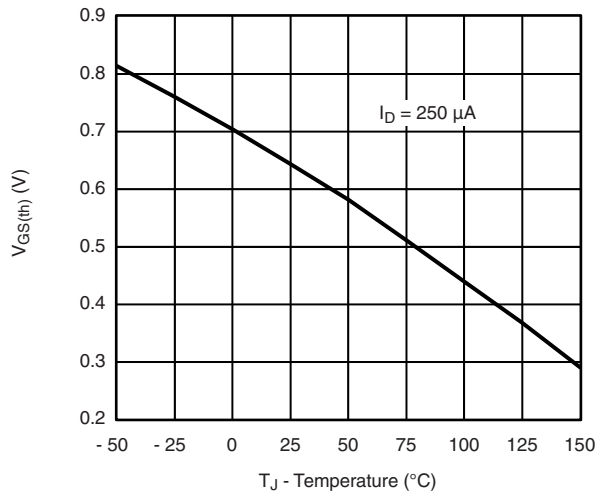
MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



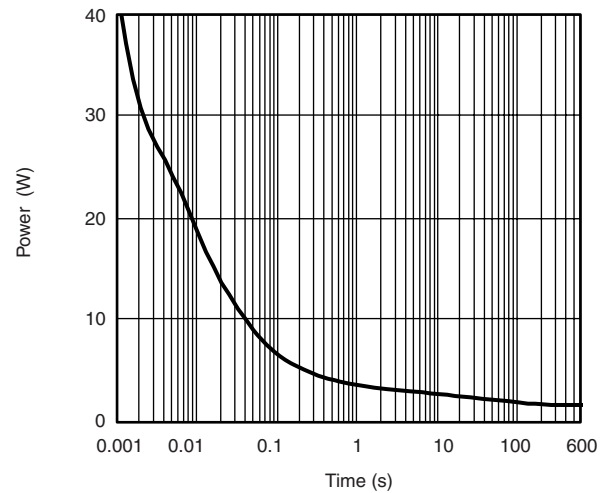
Source-Drain Diode Forward Voltage



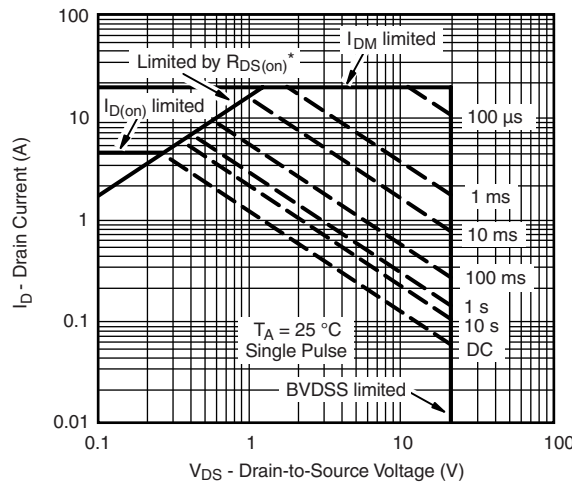
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



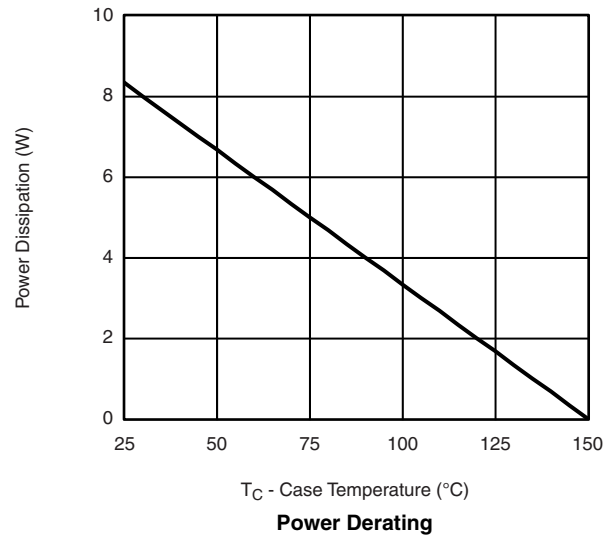
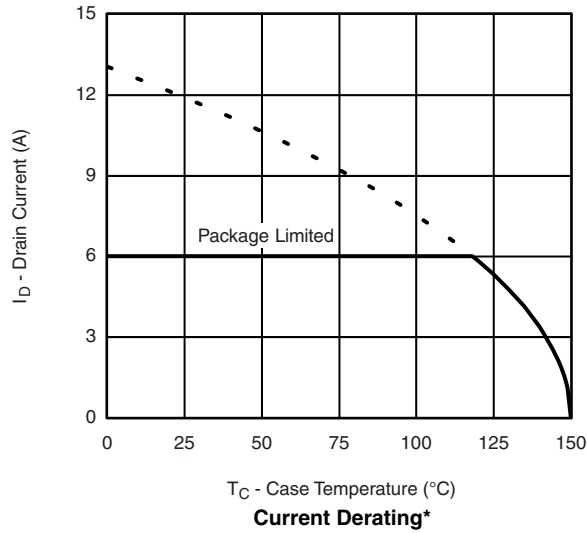
Single Pulse Power, Junction-to-Ambient



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

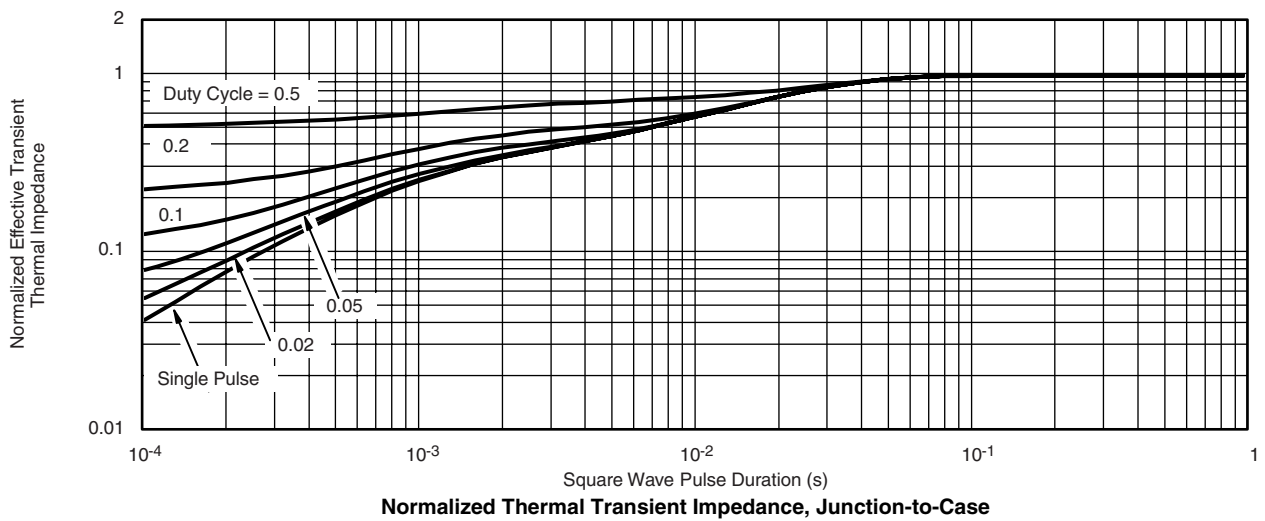
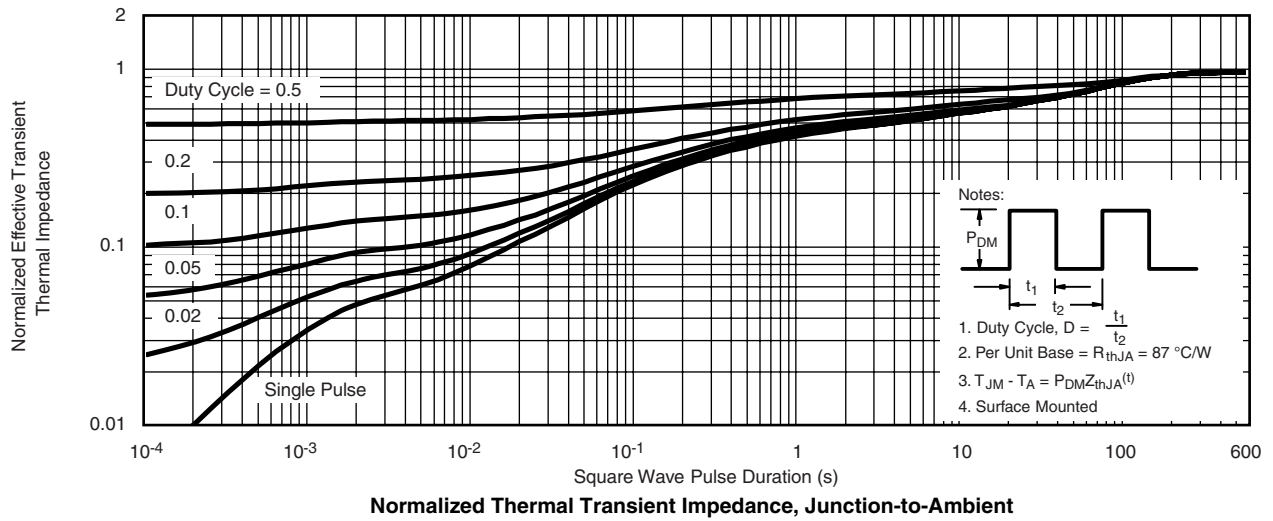
Safe Operating Area, Junction-to-Ambient

MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

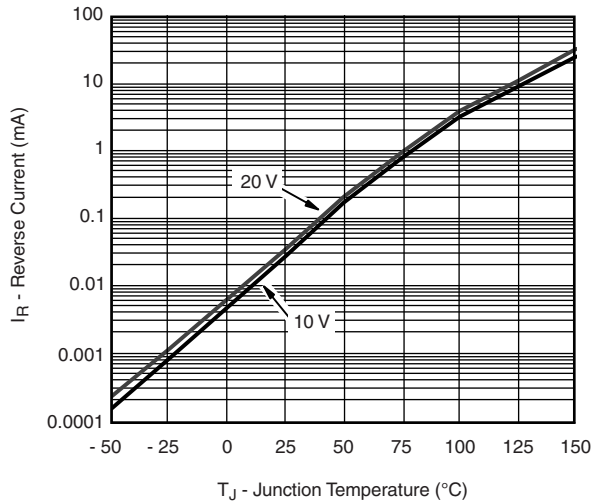


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

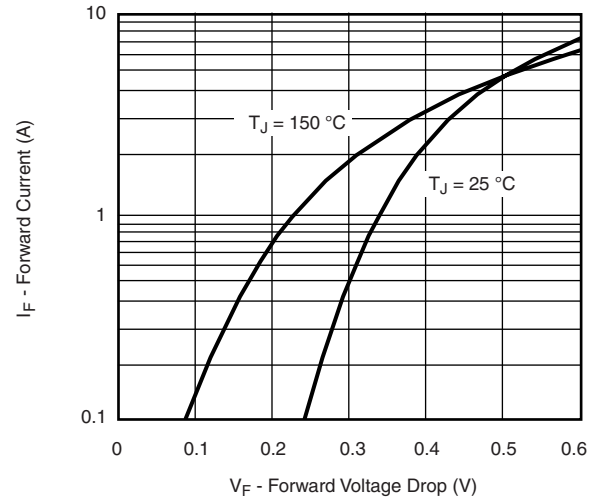
MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



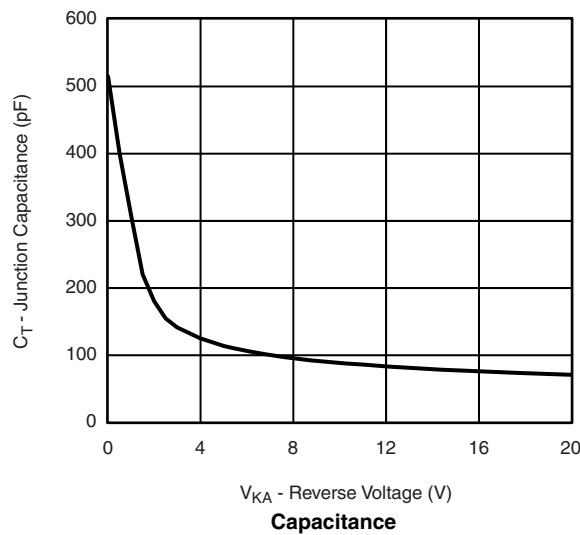
SCHOTTKY TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Reverse Current vs. Junction Temperature

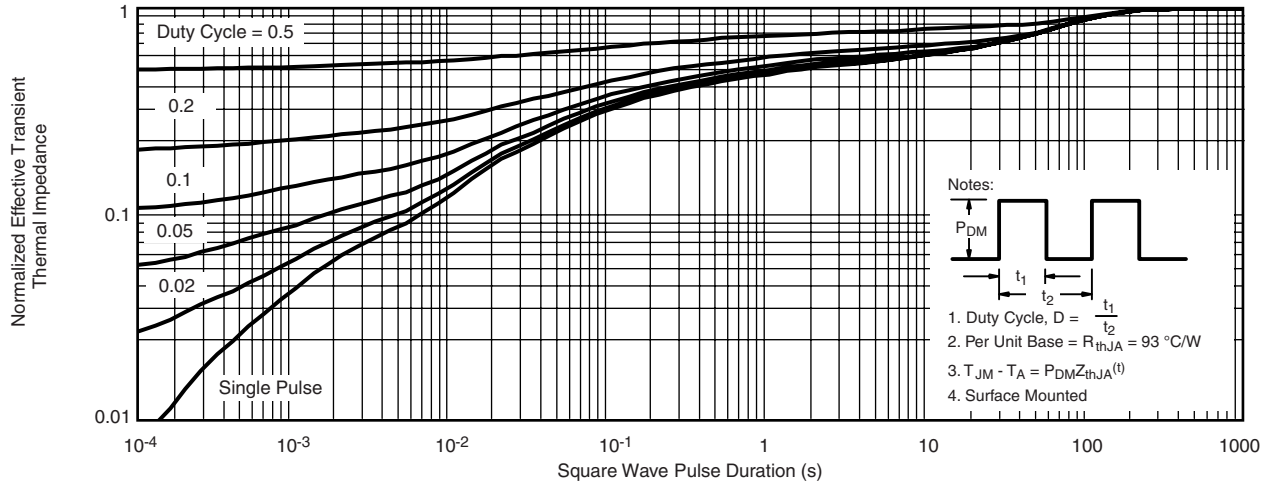


Forward Voltage Drop

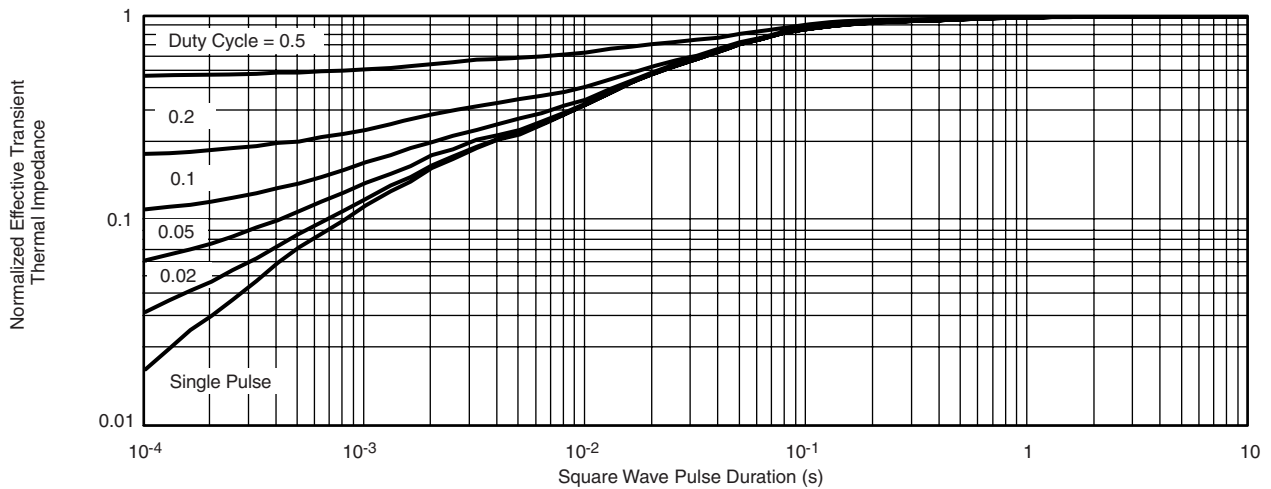


Capacitance

SCHOTTKY TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



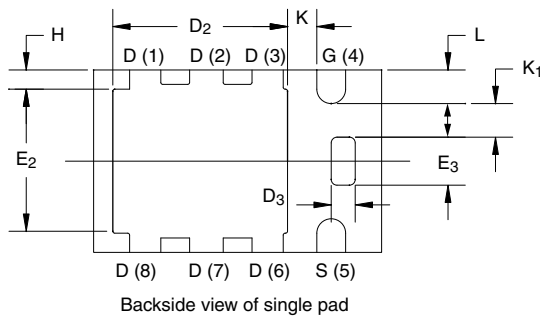
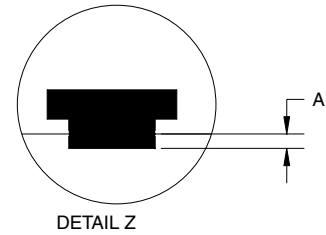
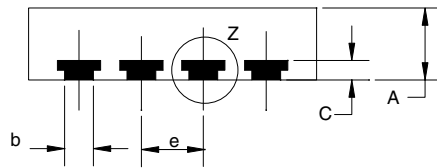
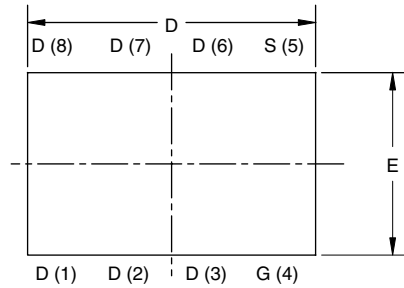
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

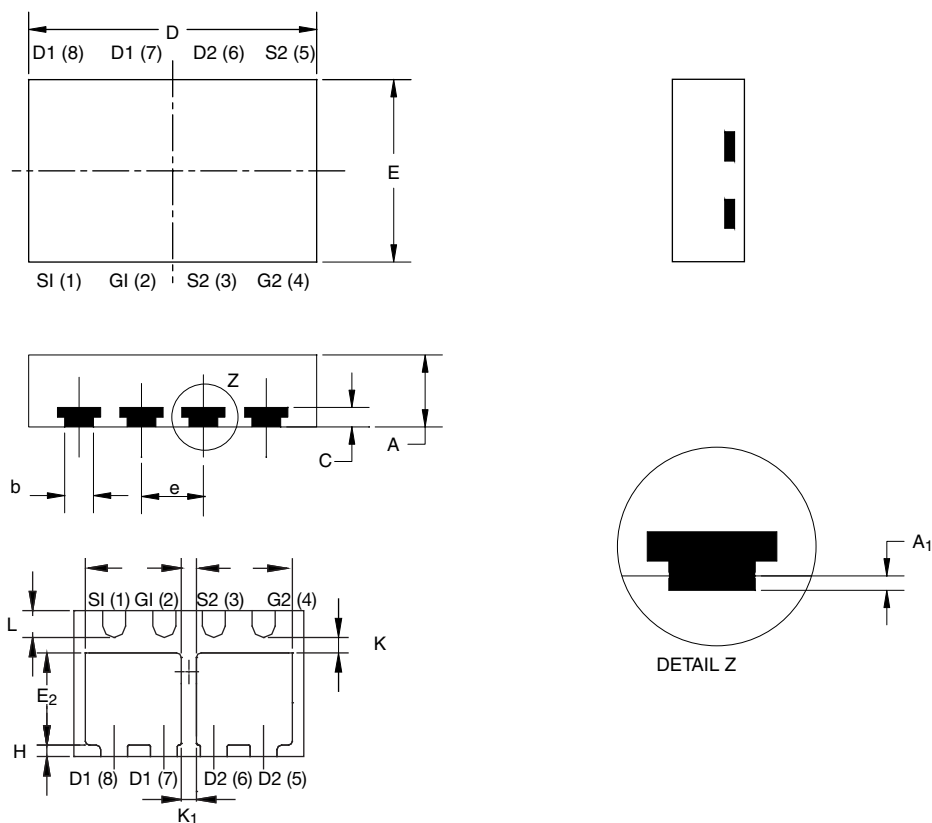
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PowerPAK® ChipFET® SINGLE PAD



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A ₁	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D ₂	1.75	1.87	2.00	0.069	0.074	0.079
D ₃	0.20	0.25	0.30	0.008	0.010	0.012
E	1.82	1.90	1.98	0.072	0.075	0.078
E ₂	1.38	1.50	1.63	0.054	0.059	0.064
E ₃	0.45	0.50	0.55	0.018	0.020	0.022
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.25	-	-	0.010	-	-
K ₁	0.30	-	-	0.012	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016

PowerPAK® ChipFET® DUAL PAD



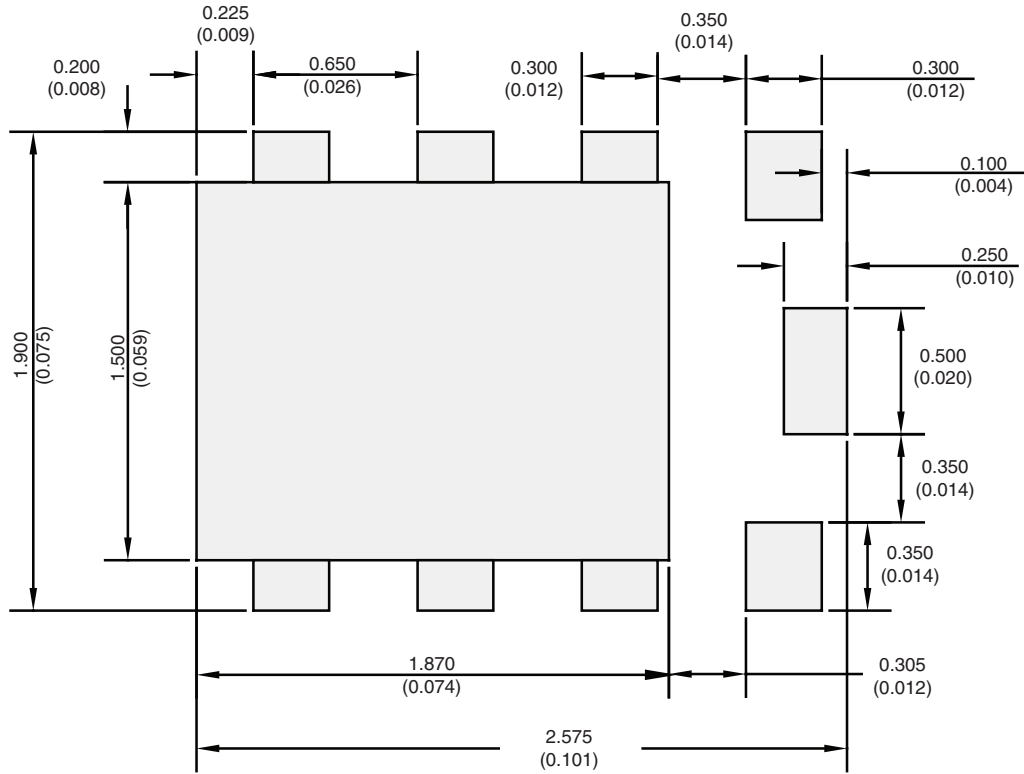
Backside view of dual pad

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A ₁	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D ₂	1.07	1.20	1.32	0.042	0.047	0.052
E	1.82	1.90	1.98	0.072	0.075	0.078
E ₂	0.92	1.05	1.17	0.036	0.041	0.046
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.20	-	-	0.008	-	-
K ₁	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016

ECN: C10-0618-Rev. C, 19-Jul-09

DWG: 5940

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Single



Recommended Minimum Pads
Dimensions in mm/(Inches)

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